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Developing a method for modeling, characterizing and mitigating parasitic light sensitivity in global shutter CMOS image sensors

Développement d'une méthode pour modéliser, caractériser et atténuer la sensibilité à la lumière parasite dans les imageurs CMOS à obturation globale

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Glossary of Abbreviations and Acronyms

ABD	Anti-Blooming Drain
ADC	Analog-to-Digital Conversion
APS	Active-Pixel Sensor
APT	Anti Punch-Through
AR	Anti-Reflection
BEOL	Back-End-Of-Line
BTE	Boltzmann Transport Equation
CCD	Charge-Coupled Device
CIS	CMOS Image Sensor
CG	Conversion Gain
CMOS	Complementary Metal-Oxide-Semiconductor
CDS	Correlated Double Sampling
CP	Collection Probability
CPD	Correction PhotoDiode
CTG	Correction Transfer Gate
CVF	Charge-to-Voltage Factor
DC	Dark Current
DCNU	Dark Current Non-Uniformity
DS	Double Sampling
DR	Dynamic Range
ESA	European Space Agency
EPI	Epitaxial Layer
FD	Floating Diffusion
FDTD	Finite-Difference Time-Domain

FEOL	Front-End-Of-Line
FPGA	Field Programmanble Gate Array
FPN	Fixed-Pattern Noise
GS	Global Shutter
GSE	Global Shutter Efficiency
ILD	Inter-Layer Dielectric
ITR	Integrate Then Read
IWR	Integrate While Read
JPL	Jet Propulsion Laboratory
LG	Light Guide
NIR	Near Infra-Red
MOS	Metal-Oxide-Semiconductor
NCDS	Non-Correlated Double Sampling
OGRD	Optical Generation Rate Density
PBC	Periodic Boundary Conditions
PD	PhotoDiode
PLS	Parasitic Light Sensitivity
PMD	Pre-Metal Dielectric
PML	Perfectly Matching Layer
PPD	Pinned PhotoDiode
PRNU	Photo-Response Non-Uniformity
PSA	Partial Spectral Averaging
PTC	Photon Transfer Curve
QE	Quantum Efficiency
RS	Rolling Shutter
SCR	Space Charge Region
SELY	Row Selector Transistor
SF	Source Follower

SHR Sample & Hold Reset

SHS Sample & Hold Signal

SL Straight Line

SN Storage Node

SNR Signal-to-Noise Ratio

STI Shallow Trench Isolation

TCAD Technology Computer Aided Design

TG Transfer Gate

TGAB Transfer Gate Anti-Blooming

TMM Transfer-Matrix-Method

RST Reset Transistor

VLSI Very Large Scale Integration

WBLS Tungsten Buried Light Shield

Introduction

Distortion-free imaging of fast-moving objects has become crucial for a wide spectrum of applications such as industrial machine vision, automotive, facial and motion recognition and Earth imaging from space [LMR13]; [Mey14]; [Vel+16]. Even though CMOS Image Sensors (CIS) performances have greatly increased throughout the years thanks to strong industrial and research efforts, achieving high Dynamic Range (DR), high sensitivity and low noise performances, the typical Rolling Shutter (RS) operation of this sensors restricts the image quality of fast-moving objects imaging: non-synchronous exposure of the entire array, in a Rolling Shutter fashion indeed, is the main cause of spatial distortions. Global Shutter CMOS Image Sensors have therefore been developed to tackle this problem. An in-pixel storing element has been added in order to allow separation between the exposure phase and the readout phase, allowing for synchronous global exposure of the array [Tak+07]. Distortion-free imaging can be therefore achieved, but the insertion of an in-pixel storage element causes new problems to be addressed; notably one highly limiting problem in Global Shutter CMOS Image Sensors is the non-negligible sensitivity of the storage element to parasitic light, especially in case a charge storing element is used. Poor performances in suppressing parasitic light though heavily limit the use of Global Shutter CMOS Image Sensors in high-speed and strong light environment.

Parasitic Light Sensitivity (PLS) has been defined as the figure of merit to evaluate the efficiency of Global Shutter CMOS Image Sensors in suppressing parasitic light to induce unwanted perturbation throughout the array. Various studies have been presented with the objective of reducing Parasitic Light Sensitivity and thus improving the Global Shutter CMOS Image Sensors performances through technological or circuital improvements. Nevertheless, few studies present a model for Parasitic Light Sensitivity, some of which only presenting simulated results without giving any details on the model exploited [Yok+18b] and some others developing a model only for a specific type of pixels [Roy+19]. Moreover, a general lack of specificity and modeling of the Parasitic Light Sensitivity as function the impinging wavelength has been noticed. This becomes of particular importance when realizing that applications like facial and motion recognition often require Near-InfraRed (NIR) detection (850 - 950 nm), while it is common practice on the market to only characterize Parasitic Light Sensitivity performances at a wavelength of 550 nm.

One of the scopes of this work is to develop a framework to allow improvement of the Global Shutter CMOS Image Sensors performances through a deep understanding of parasitic light collection by the Storage Node. Base of the framework is the development of a method for modeling Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors, wavelength and given pixel design parameters as input. Chapter 2 is focused on explanation of the phenomena causing non-negligible Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors and their modeling. A steady-state efficient method is presented, exploiting the Finite-Difference Time-Domain (FDTD) simulations to model the electromagnetic properties of light inside the pixel structures. The charge transport properties inside the silicon active region are modeled

via single-particle Boltzmann Transport Equation, implemented in MATLAB®, and with the drift-diffusion model using TCAD simulations for comparison.

In chapter 3 the developed model is exploited as a fast tool to improve Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors. Different pixel designs are modeled and compared, with the aim in giving guidelines for an efficient Global Shutter pixel design. Notably, an important part of the chapter focuses on the understanding of the light shielding properties of metallic interconnection layers and their optimal exploitation to shield the in-pixel storage element from direct impinging parasitic light. To prove simulation results, test structures have been developed and characterized in chapter 4.

Though being treated as a figure of merit, there is no standard metric for measuring Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors. Some measurement techniques have been presented in literature [Mey+11], though they may not apply for a general characterization of each pixel in the array. Chapter 4 presents a development of a standard metric for measuring Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors that can be applied to the large variety of Global Shutter CMOS Image Sensors on the market. The metric relies on Quantum Efficiency (QE) measurements, which are widely known in the image sensor community and well standardized. The metric allows per-pixel characterization at different wavelength and at different impinging angles, thus allowing a more complete characterization of the Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors.

An important effort has been put into the enhancement of Global Shutter CMOS Image Sensors performances via technological improvement. Conversely, few studies have been made on post-process correction methods to mitigate the problem of Parasitic Light Sensitivity [SJI19]; [Ge+19]. Though often limiting the operating frame rate, post-process correction methods may result in a cost-effective way to reduce Parasitic Light Sensitivity, especially when technological improvement is not a viable option. In chapter 4 different post-process correction methods are presented taking into account the different Global Shutter operating modes (triggered, also called Integrate Then Read (ITR) or pipeline, also called Integrate While Read (IWR)). Increasing the panel of post-process correction methods allows the user choose the one better suiting the required applications.

Chapter 1

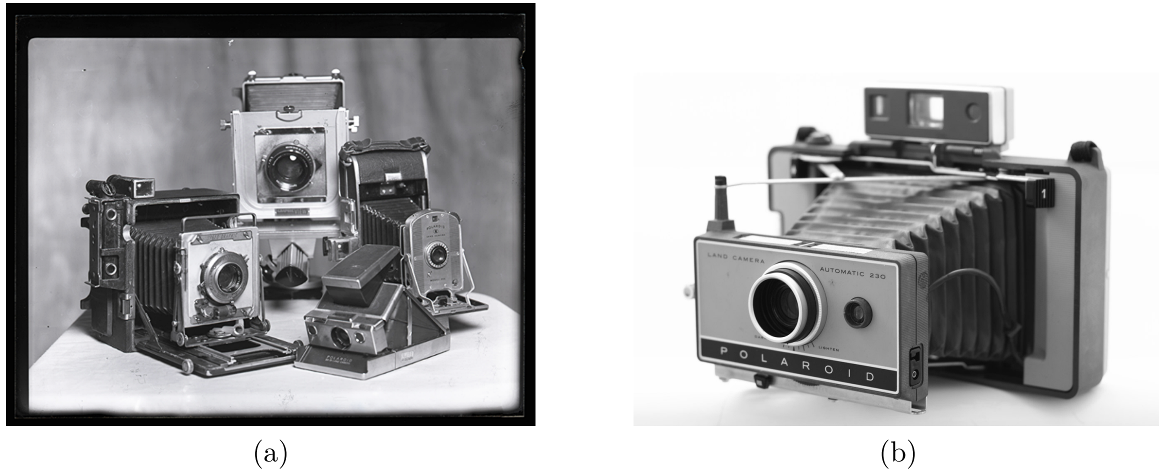
Global Shutter CMOS Image Sensors, working mode and applications

1.1 History of Image Sensing

1.1.1 Early days of photography

Niépce develops the first permanent images using a plate covered with bitumen dissolved in oil, which is photosensitive. Successive etching of the bitumen first and the plate afterwards created an etching plate for printing in press. *Heliographs* is the name given to these plates. Hours long exposure time was though an issue of this technique. Niépce began soon after a partnership with Louis Jacques Mandé Daguerre, a famous Parisian inventor, discovering a new technique to darken the exposed portions of heliographs through use of silver previously exposed to iodine fumes. After Niépce's death few time later, Daguerre discovered that silver iodide plate required only a fraction of the exposure time and that a latent image could be revealed by exposing the plate to mercury fumes. This marks the beginning of the *Daguerreotype image*. The latent image and use of silver combined with iodine became the basis of every major camera process of the 19th century. William Henry Fox Talbot, unaware of Niépce and Daguerre's works, developed the so-called *photogenic drawings* resulting in colorful positive images. However this technique, and other techniques developed soon after by Bayard, Ponton, and Herschel, resulted in lower sensitivity and resolution compared to the daguerreotypes. The latter was then made the process of choice for commercial use by the late 1840s.

The invention of Emulsion Plates marks the beginning of a new era. These plates, also called wet plates, used an emulsion process called the Collodion process making these plates more sensitive, few seconds of exposure were sufficient, and less expensive compared to daguerreotypes. Portrait photographs became the most common use of photography, moreover many photographs from the Civil War were produced on wet plates. The drawback associated to these plates is found in the need of carry chemistry to rapidly develop the pictures. In the 1870s this problem was solved thanks to the invention of Richard Maddox, creating dry gelatine plates that were nearly equal to wet plates in speed and quality. Dry plates could



(a) (b)

Figure 1.1: (a) Cameras for the use of dry plates. (b) First Polaroid instant camera.

be relied upon at any time and developed later at a more convenient location. As a plus, the process also allowed for smaller cameras that could be hand-held, grabbing the interest of amateurs and commercial photographers. Example of dry plate cameras can be seen in Fig. 1.1a.

Photography revolution started some years later, when George Eastman started a company called Kodak in the 1880s. His creation of a flexible roll film that did not require constant changing the solid plates allowed him to develop a self-contained box camera holding the film roll, making it accessible not only to professionals but also to the common consumer. A famous Kodak slogan said: "You press the button, we take care of the rest", leaving the consumer to just take care of the shot and allowing them to develop their pictures sending the camera back to the factory. With the beginning of the World War II many photographers started to use the newer 35mm film and cameras, giving way to capture decisive moments and shaping the face of photography forever. At the same time, Polaroid introduced a novel camera that used a secret chemical process to develop film in less than a minute; instant images caught the public's attention and camera prices dropped leading to a wide use. Example of the first Polaroid instant camera can be appreciated in Fig. 1.1b. Polaroid stopped the instant film production in 2008.

1.1.2 The digital camera: solid-state imagery

To understand the reason why Polaroid ended its instant film production, it is needed to jump to 1960s - 1970s, where solid-state imagery has its roots. At that time, vidicon tube was the main technology for electronically capturing video, being mature with more than 30 years of television development behind it. Vidicon technology, despite its excellent quality, had several drawbacks like size, weight and lag, being disadvantageous for many applications [Don99]. Requirements for a lighter and smaller technology drove the research towards solid-state image sensors.

Figure 1.2: Modern full-frame 24 mm × 36 mm CMOS Image Sensor embedded in a mirrorless camera consumer grade application.

The first attempt to operate a *p-n* junction as an integrator for photodetection was done by Weckler at Farchild in 1965 [Wec65]. He observed that leaving floating one terminal of an initially reverse biased *p-n* junction would produce a voltage drop at the terminal which is dependent on the capacitance of the junction and on the photocurrent flowing into the floating node. This study gave rise to the development of the first MOS passive pixel sensor (MOS PPS) [Ren+90]. This pixel was making use of a floating *p-n* junction, also called *PhotoDiode*, and a single transistor for column Bit Line access. No amplification of the in-pixel signal was foreseen until 1968 when Noble and Plessey proposed the first MOS Active Pixel Sensor (MOS APS), with the addition of a reset transistor to force a reset voltage onto the PhotoDiode and a buffer transistor for amplification.

Nevertheless, the first MOS PPS and Active Pixel Sensor were not able to compete against the newly developed *Charge-Coupled Device* (CCD), due to different noise issues that were not present on this latter. CCD was invented in 1969 by Boyle and Smith [BS70] at Bell Labs, initially called Charge Bubble Devices, in analogy with magnetic bubble memories since storage was the primary objective for which CCD has been created. Its application as an image sensor was evident and soon after reported by Tompsett, Amelio and Smith in 1970 [TAS70]. Throughout the 1970s and the 1980s CCDs dominated the image sensor market: nearly all commercial video cameras were starting to include CCD as detector, moreover more scientific applications were requiring the use of a solid-state detector. Most of all, two space imaging applications allowed for the improvement and the establishment of CCD as the main image sensing technology, being the U.S. National Aeronautics and Space Administration (NASA) Large Space Telescope (later called Hubble Space Telescope) and JPL unmanned space probes for solar system exploration.

When talking about technology and its improvements, changes are just around the corner. CMOS Image Sensors have been under sporadic investigation since the 1960s, as it has been said before, but it is since the 1990s that these image sensors have seen a resurgent interest and a consistent amount of studies. The major reasons for this grown interest can be found in the need to develop miniaturized and cost effective imaging systems. Integration of CCD

technology onto CMOS one was troublesome, while integration of VLSI electronics on the same chip would reduce component and packaging costs. The first version of what became known later as CMOS Active Pixel Sensor was developed in 1990 by Andoh et al. [The03]. Few years later, in 1993, a CMOS Active Pixel Sensor with intra-pixel charge transfer was developed at JPL and promoted by E. Fossum et al. [Fos93]. Implementation of the Pinned PhotoDiode (PPD), firstly developed for CCD, onto CMOS Image Sensor became possible in 1995 by a collaboration between JPL and Kodak [Lee+95]; this, together with other improvements in the following years, made the CMOS Image Sensor able to achieve similar, or even better, imaging performances in comparison with the CCDs starting from the 2000s, allowing the CMOS Image Sensor business to take off [The08]. Over the last decade, CMOS Image Sensor technology allowed the proliferation of various low power, high income margin applications requiring image sensing such as automotive, security, medical, professional photography (Fig. 1.2 shows a modern CMOS Image Sensor embedded in a high performing digital mirrorless camera) and smartphones. Notably, the steady growth of mobile phones sales has been one of the primary driver for CMOS Image Sensor market growth, allowing for higher research and development spending as well as an increased number of patent filling [Fon15]; [Fon19]. As a result of high research and development investments, various technological improvements have been introduced to enhance the performances of CMOS Image Sensors, also boosted by the ever-shrinking CMOS technology scaling. Small pixels of $\sim 1\,\mu m$ pitch or even less are nowadays available on the market [Wuu+10]. Backside illumination [NDF02], microlenses [ABT03], optical stack light guides [Vel+16] and pixel isolation by trenches [Kum+18] alongside with 3D multi-wafer integration [Kon+15] have strongly increased the sensitivity and performances of CMOS Image Sensors, allowing for the integration of new capabilities as for example the Global Shutter operation mode.

Even though not completely ruling out the CCDs out of business, the research extent leading technological improvements together with low power operation, ease of integration with CMOS circuitry, ease of development of smart sensing and reduced production and packaging costs have put CMOS Image Sensors in a strong position in nowadays market.

1.2 History of Earth Observation from Space

1.2.1 First aerial images

Aerial images trace back at the end of the 1850s, when a photographer and balloonist known as Nadar produced the first ever aerial photograph (in Fig. 1.3) from a tethered hot-air balloon 80 meters above the ground, using the Collodion process requiring a complete dark room to be carried inside the balloon basket. Unfortunately, his photographs haven't lasted until our days, but his achievements laid foundations for successive works. With the improvements of photographic technology resulting in smaller cameras exploiting dry-plates, various aerials images were taken exploiting flying objects like pigeons or kites.

During World War I, aerial photography from airplanes soon replaced sketching and draw-

Figure 1.3: View of Boston on the first ever aerial image on a Colloidon process [Hol].

ing by aerial observation. Maps were therefore produced starting from aerial photographs and proved their pivotal military worth; camera technology was being constantly improved (ad for example the invention of a mechanical shutter inside the lens to drastically improve camera stability and image quality) and by the end of the conflict both sides were photographing the entire front twice a day.

Following the end of the war, the aerial camera was turned to non-military purposes.A series of overlapping photographs of Manhattan Island were taken, that turned into an aerial map, which became a commercial success and was used by several New York City agencies and businesses. Deals with other cities followed, as it was found aerial surveys to be faster and cheaper than a ground survey. This started a successful commercial venture for aerial photographs, proving its civil uses [PAP].

The ever first photography of Earth's curvature was taken in 1935 by the Explorer II balloon, reaching a height of 20 kilometers above Earth's surface. Satellites were going to be invented soon after...

1.2.2 Observing satellites

The satellite era of remote sensing began in 1957 when Sputnik 1 was launched by the Soviet Union. This satellite was able to complete Earth's orbit every 96 minutes and transmit radio signals that could be received on Earth, though it was not designed for Earth Observation and did not carry any camera on it. The first satellite designed specifically for this task was

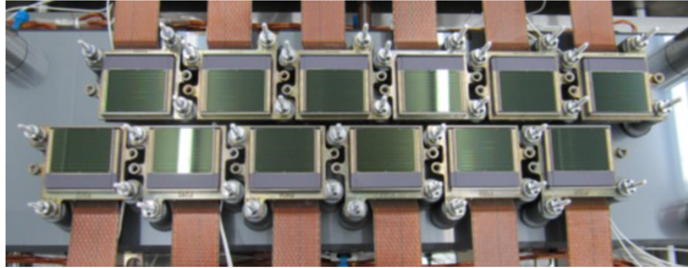


Figure 1.4: Focal plane part of the MultiSpectral Instrument for the ESA/EU Sentinel 2 mission.

Vanguard 2, even though some technological problems made his life short. Vanguard 2 was therefore replaced by TIROS-1 in 1960, which was able to produce the first television footage of weather patterns from space.

Monitoring of Earth's land areas started more or less in 1972 with the launch of the satellite Landsat-1, previously called *Earth Resources Technology Satellite* (ERTS), following pioneering research by the U.S. NASA. Landsat-1 was bringing a Vidcon sensor, which unfortunately failed, and a multispectral digital sensor that worked well. Following its success in multispectral remote sensing, a series of newer Landsat missions were eventually launched, establishing a reference for similar observation satellites and sensors of the following decades, such as the French *Système Pour l'Observation de la Terre* (SPOT).

Since the early 1990s, the national space organizations, such as the U.S. NASA and the European Space Agency (ESA), focused their Earth observation resources on the design and launch of large multisensor platforms. The European Remote-Sensing satellites (ERS-1 and ERS-2), launched by ESA in the mid-1990s, started the European Earth observation missions. The two satellites were carrying a number of six main sensors, each one designed to monitor a specific aspect of Earth system process.

The study of mechanisms controlling the global climate system and its change were to become heavily dependent on the use of satellite observation. At the beginning of the 2000s satellites for environmental observation were being built: NASA launched two satellites forming the Earth Observing System (EOS), while ESA sent in space the largest Earth observation satellite ever built, ENVISAT, carrying 10 different sensors. ENVISAT was indeed built to continuously monitor the main Earth environmental parameters as the atmosphere, the oceans, the ice sheets and lands. Collected data were to be used not only for climate modeling, but also for study of Earth's dynamic and structure and for resources monitoring [Eurb].

More recently, ESA launched a joint program with the European Environment Agency (EEA) called Copernicus (previously Global Monitoring for Environment and Security) with the aim in providing accurate, timely and easily accessible information to improve the management of the environment, understand and mitigate the effects of climate change and ensure civil security through an Earth observation program [Eura]. Each mission of the project,

called Sentinel, is based on a constellation of four satellites to provide a robust revisit and coverage of Earth. An example of space grade image sensors developed for the Sentinel 2 mission by EADS-ASTRIUM and ISAE-SUPAERO can be found in Fig. 1.4 [BLSP13]. Six Sentinel missions are already operational, while other missions are still under development. Copernicus and Sentinel missions represent the most ambitious Earth observation program to date.

1.3 CMOS process for Image Sensing

Light detection through solid-state technology relies on the capacity of the system to count the number of incoming photons and convert them to an intelligible signal. Using solid-state technology, detection follows two main steps:

1. creation of free carriers proportional to the incoming number of photons;
2. counting of photo-generated carriers.

Let us start with the first step: creation of free carriers. When light hits the semiconductor, the photons generates electron-hole pairs through photoelectric effect. The generation of electron-hole pairs has been found to be dependent on the incoming photon wavelength, thus on the incoming photon energy modeled as follows [SN06]:

$$E_{ph} = h \cdot \nu = \frac{h \cdot c}{\lambda} \tag{1.1}$$

where h is the Planck's constant, ν the photon frequency, c the speed of light in vacuum and λ the photon wavelength. Electron-hole pair generation consists in a valence band electron interacting with a photon and acquiring its energy to be excited and elevated to the conduction band. This effect is only possible if the energy of the photon is sufficiently high to cause an excitation, thus following Eq. (1.2).

$$E_{ph} \geq E_g \quad \Rightarrow \quad \lambda \leq \frac{h \cdot c}{E_g} \tag{1.2}$$

where E_g is the semiconductor bandgap, defined as the difference between the conduction band and the valence band energies. Remembering that in silicon $E_g \approx 1.12\,\text{eV}$, in a first approximation, the incoming photons wavelength, called upper cut-off wavelength λ_c, required to promote an electron from valence band to conduction band, thus creating an electron-hole pair must respect the following [KS01]:

$$\lambda_c \leq \frac{h \cdot c}{E_g} \approx 1.11\,\mu\text{m} \tag{1.3}$$

It is therefore interesting to point out that electron-hole pairs in silicon can be generated with visible light, remembering that its wavelength is comprised between 400 nm and 700 nm.

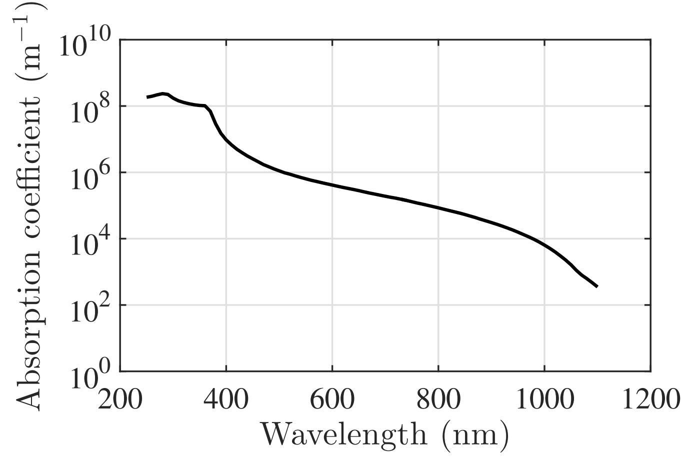


Figure 1.5: Absorption coefficient in silicon as function of wavelength [Ref].

Incident photons with wavelength shorter than λ_c become absorbed as they travel in the semiconductor and the light intensity, which is proportional to the number of photons, decays exponentially with the distance into the semiconductor. The light intensity I at a distance z from the semiconductor surface is given by the Beer-Lambert law:

$$I(z) = I_0 \cdot e^{-\alpha(\lambda) \cdot z} \tag{1.4}$$

where I_0 is the intensity of the incident radiation and α is the absorption coefficient, measured in m^{-1}. Absorption coefficient α is a property of the material and it is wavelength dependent.

Beer-Lambert law relates the attenuation of light with properties of the material, thus its absorption. Being the absorption coefficient α wavelength dependent as shown in Fig. 1.5, the ratio of light absorbed in silicon will be dependent on incoming wavelength, thus the number of electron-hole pairs generated at a certain depth will be dependent on the amount of photons at that depth. Integrating the Beer-Lambert law with respect to depth, it is possible to obtain the curves shown in Fig. 1.6. It is possible to appreciate that short wavelength incoming light is absorbed in a shallow depth, as the case of 400 nm and 500 nm, thus leading to electron-hole pairs generation closer to the silicon surface. Going to longer wavelengths, lights penetrates deeply in silicon, thus electron-hole pairs are generated more deeply. Exploiting the Beer-Lambert law it is therefore possible to retrieve the electron-hole pairs generation rate $G(z)$ at a given depth z. Knowing that it is possible to obtain the incoming photon rate Γ_0 through the equation $\Gamma_0 = I/E_{ph}$ and supposing that one incoming photon is able to generate one electron-hole pair, the electron-hole pairs generation rate will simply follow Eq. (1.5).

$$G(z) = \Gamma_0 \cdot e^{-\alpha(\lambda) \cdot z} \tag{1.5}$$

Similarly to what showed by Beer-Lambert law, it is easy to see that generation of electron-hole pairs rapidly decreases with depth when shorter wavelengths are taken into account,

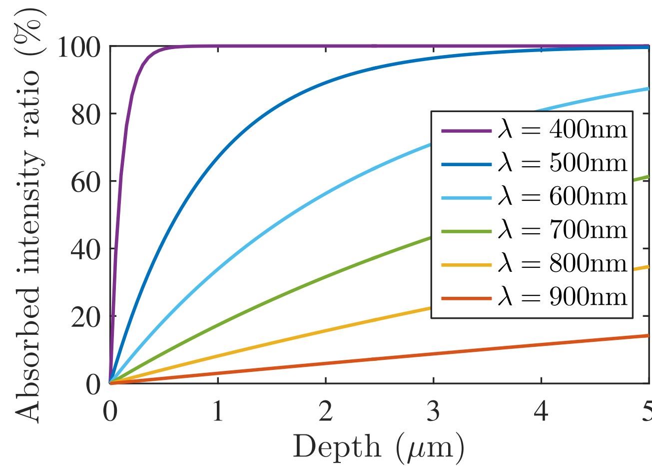


Figure 1.6: Light absorption in silicon as function of wavelength and depth, making use of the Beer-Lambert law.

differently from longer wavelengths where generation of electron-hole pairs close to the silicon surface is low.

We will now focus on the second step: counting of photo-generated carriers. It is mandatory to tell the reader that the following discussion will use the Drift-Diffusion model assumptions. Drift-Diffusion model describes free carriers in a semiconductor following two regimes of motion: the drift, responding to the local electric field, and the diffusion, depending on the local carriers concentration. Let us give the example of a p-doped semiconductor. Impinging photons will create electron-hole pairs, thus electrons will be promoted in the conduction band. Free electrons found in a p-doped region are designated as minority carriers. If no electric field is present, electrons will diffuse inside the p-doped semiconductor as free carriers and eventually recombining, if not reaching any boundaries (edges, metal contacts, ...); the time spent by the carrier in free roaming before recombination is called lifetime, τ. We will not enter into the details of carriers recombination, which is not the scope of our dissertation, but it is important to consider that free carriers must be counted or collected before they recombine, otherwise a part of the information on impinging light will be lost.

The first attempts of counting photo-generated electrons was done through polarization of a silicon slab, similarly to how photodetectors work. Polarization of the silicon slab would create an electric field inside the material that would drive the electrons towards the positive pole and holes towards the negative one, hopefully in a shorter time with respect to carriers lifetime. To count the amount of impinging photons in every instant it was sufficient to measure the resulting photocurrent. From simple calculations, it is easy to see that accurate current measurements would be hard and expensive to perform due to the low photocurrent value that could be retrieved. As briefly described in Sec. 1.1.2, the first attempt to store charges in a p-n junction and measuring the voltage drop instead of the current was done by Weckler at Farchild in 1965. The underlying idea was to create an electric field through the

use of a reverse biased p-n junction left floating, which could separate the electron-hole pairs generated inside the Space Charge Region (SCR), sweeping electrons to the n-doped zone and holes to the p-doped zone. Electrons swept in the n-zone would then have a much longer lifetime and at the same time would lower the junction potential. The amount of impinging photons could then be retrieved from the potential drop at the terminals of the p-n junction following Eq. (1.6),

$$\frac{dV}{dt} \approx \frac{J_{ph} \cdot A_d}{C_d} \tag{1.6}$$

where J_{ph} represents the photocurrent density, A_d the area of the detector and C_d the p-n junction capacitance.

Once understood that we desire to collect charges on a diode in order to count them through the voltage drop, let us try to mix the generation of electron-hole pairs as function of impinging wavelength with charge collection. Charges generated in the Space Charge Region are easily collected, being driven by the electric field towards the n region. On the other hand, collection of charges created in the quasi-neutral regions, i.e. where electric field is considered null, is more difficult. Notably, carriers created in the quasi-neutral regions will diffuse in a casual direction which could be different from the desired one, since the carrier will not be following any field lines. Free diffusing carriers will then roam around until either reaching an electric field or recombination.

If the free carrier reaches the Space Charge Region, the electric field will drive it towards the n-doped junction of the PhotoDiode and the carrier will be collected and participate to the potential lowering. If not reaching the PhotoDiode Space Charge Region, the carrier can continue its roam until recombination, for example when reaching a recombination center like the silicon surface. Other electric fields can also be present inside the silicon structure and drive the free carrier, as for example the ones generated by doping gradients. Given all these assumptions, it is easy to understand the difficulties of collecting carriers when electron-hole pairs are generated through longer wavelength impinging photons.

Modern image sensors use this concept of the floating p-n junction to create a PhotoDiode; the advancements compared to what has been developed by Weckler is given by the ways to readout the voltage drop across the PhotoDiode due to the photo-generated collected carriers. Let us imagine to use just one PhotoDiode to create an image sensor: it is easy to see that the single PhotoDiode would give us the result of the entire amount of light collected without having references on the region where this light has been collected. The passage to an array of PhotoDiodes is then straightforward. An image sensor is then constituted by a two-dimensional array of small repeating elements called pixels. One pixel will contain the photosensitive element used to collect the amount of light of a small region. The image is therefore reconstructed by a mosaic, where each tile contains the information of the amount of light captured by the corresponding pixel.

For the purposes of this thesis, we will just focus on CMOS Image Sensors. The advantage of integrating and image sensor on CMOS technology is the possibility to built the photosensitive and the readout elements on the same wafer using the same technology, reducing

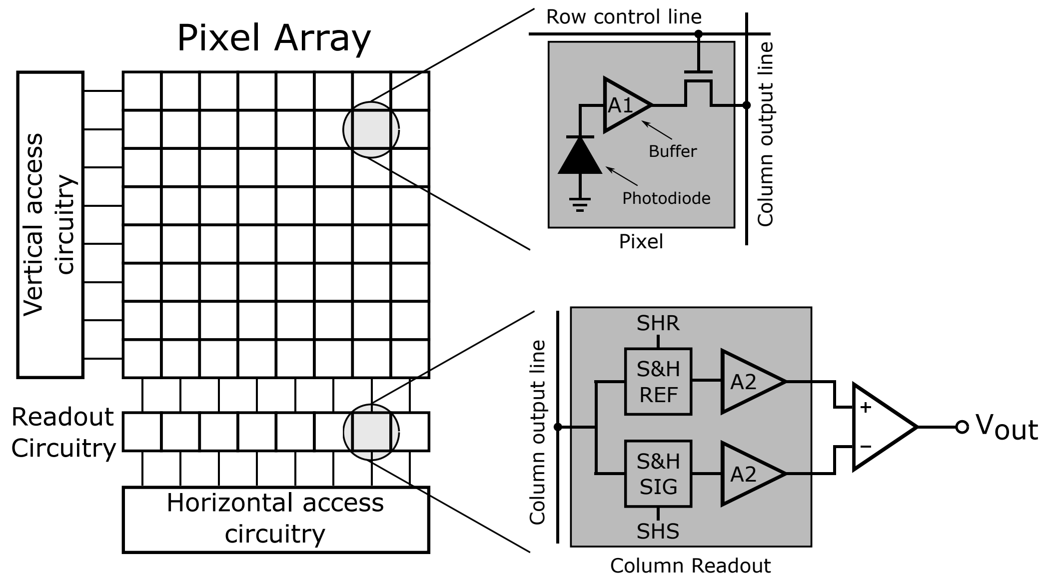
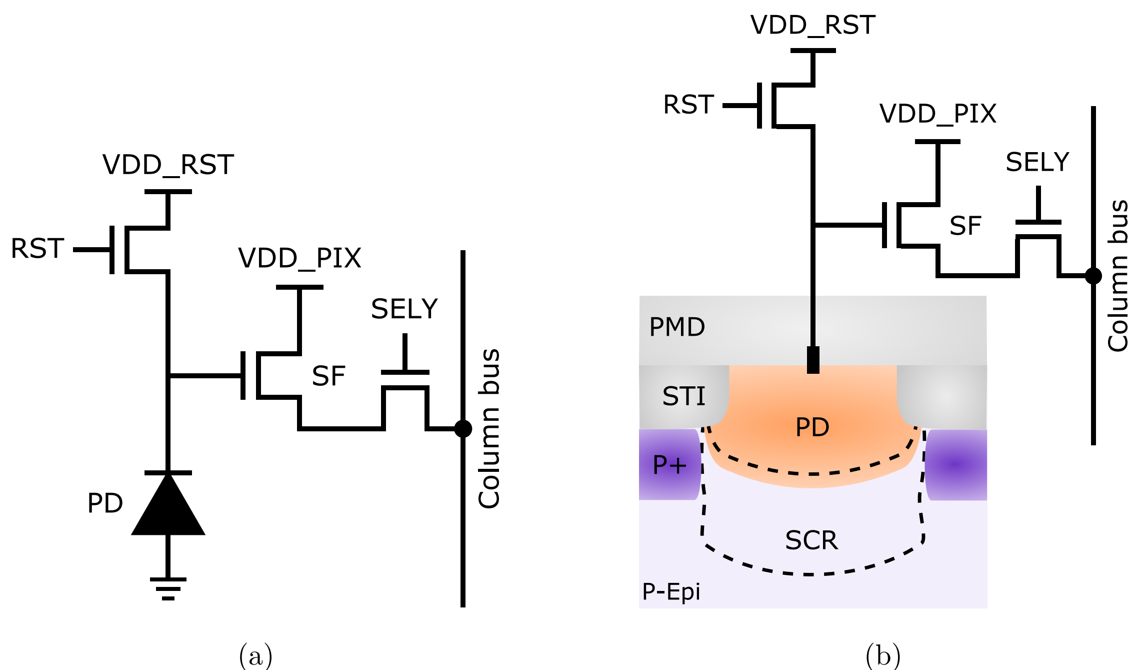


Figure 1.7: CMOS Image Sensor architecture containing an array of pixels, the vertical access circuitry to select the row, the horizontal access circuitry to select the column and the readout circuitry, generally consisting of amplifiers and Sample&Hold blocks, controlled by the signals Sample&Hold Reset (SHR) and Sample&Hold Signal (SHS), to store the information retrieved from the pixel array.

integration and development costs as well as power consumption. Pixel output is given as a voltage and each pixel can be randomly accessed through a combination of vertical and horizontal access circuits, just like Random Access Memories. This allows for the development of faster and smarter image sensors. In Fig. 1.7 it is possible to appreciate a typical CMOS Image Sensor architecture. The imaging area is a two-dimensional array of pixels, each pixel contains a photodetector and some transistors. This area is the heart of an image sensor and the imaging quality is largely determined by the performances of this area. Access circuitry is used to access a pixel and read the signal value in the pixel in a similar way of what happens in Random Access Memories, as previously said. A readout circuit is a one-dimensional array of switches and Sample&Hold (S&H) circuit, which is used to temporary collect, amplify and store a pixel output. Taking a closer look at the pixel schematic in Fig. 1.7 it is possible to notice that every pixel contains a photosensitive element, in this case a PhotoDiode, an amplifier and a line selector transistor. The PhotoDiode output is therefore buffered before being sent on the column output line, having the advantage in noise reduction and higher speed capabilities. Another name given to this type of CMOS Image Sensor is Active Pixel Sensor (APS), as briefly described in Sec. 1.1.2.

1.3.1 The Active Pixel Sensors

As previously mentioned, the critical area of an image sensor is the pixel array. Understanding of this area is therefore crucial to improve image sensor performances, so a strong knowledge



(a) (b)

Figure 1.8: (a) Schematic of a 3T pixel containing a PhotoDiode (PD), the reset transistor (RST), the Source Follower transistor (SF), the selector transistor (SELY). (b) Cross-section view of the 3T pixel including the same elements plus the p+ doping layer and the Shallow Trench Isolation (STI).

of the pixel schematic and structure is highly desired.

The schematic of the simplest active pixel, called 3T pixel, is shown in Fig. 1.8. It is easy to understand the reasons behind this name: “T” stands for transistor, and the pixel is composed of 3 transistors, plus one photosensitive element. The role of the line selector transistor is played by the SELY transistor, the role of the buffer is played by the Source Follower (SF) transistor and the role of the photosensitive element is played by the PhodoDiode (PD). The third transistor, hence the reset (RST) transistor, is used to pull the PhotoDiode to a reset level before each integration period. The information acquisition process in a 3T pixel works as follows: a reset operation through the RST is performed before each exposure period; once the RST is switched off the integration period starts, the PhotoDiode collects the free electrons generated by the incoming light; at the end of the integration period the voltage on the PhotoDiode is buffered by the SF and transferred to the column output line through SELY to be finally sampled in a Sample&Hold circuitry via the command Sample&Hold Signal (SHS). The reset value is stored as well (in a technique called Double Sampling that will be better explained further on) after the reset operation using the command Sample&Hold Reset (SHR). The time diagram of the integration and sampling process can be seen in Fig. 1.9.

As shown in Fig. 1.8a, the PhotoDiode consists in an *n*-diffusion on a *p*-substrate; after the reset operation, the n-diffusion is polarized at a positive potential while the p-substrate

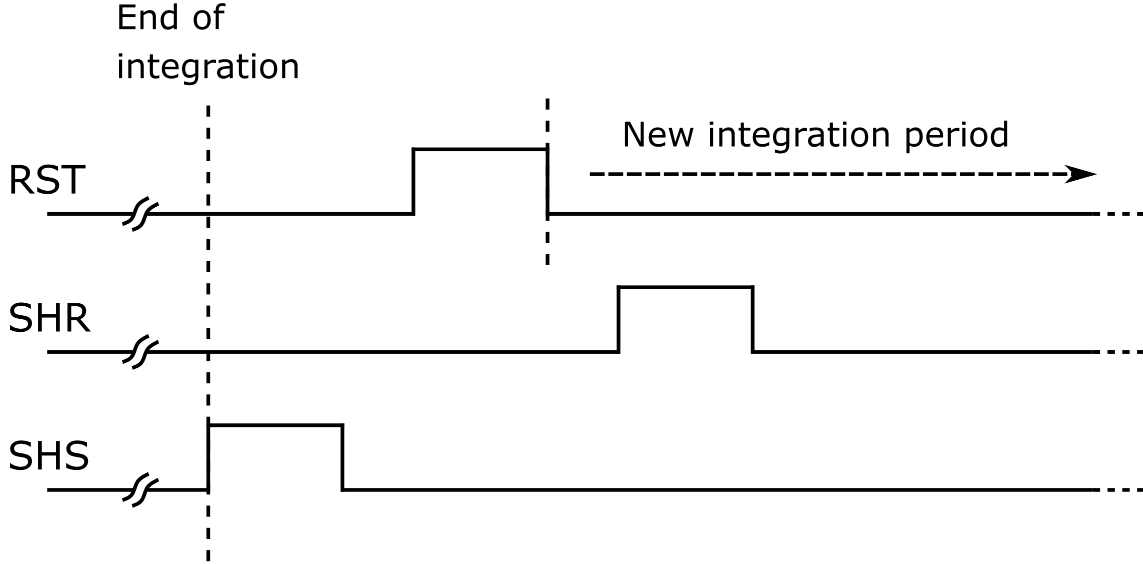


Figure 1.9: Time diagram exploited to operate the 3T Active Pixel Sensor in a dual sampling fashion. SHS samples the integrated signal voltage, RST is operated to reset the PhotoDiode and SHR samples the reset voltage.

is kept at ground potential, thus finding the diode in reverse polarization. A Space Charge Region (SCR) is therefore created which gives rise to an electric field pointing towards the *p*-substrate. It is important to accurately describe this region and its extension; as previously said, free electrons collection relies on the capability to direct them towards the n-diffusion of the PhotoDiode, thus collecting them, the electric field presence plays a fundamental role in guidance of free charges. In a first approximation, we will rely on diode equations considering abrupt junction, i.e. we will suppose a sharp transition between the two regions with different dopants, in order to describe the electric field direction and module as well as the SCR extension. Relying on Fermi statistics, it is possible to describe the junction built-voltage V_{bi} as follows:

$$V_{bi} = \frac{k_B T}{q} \log \left(\frac{N_D N_A}{n_i^2} \right) \tag{1.7}$$

where k_B is the Boltzmann constant, q is the electron charge, N_D is the donor concentration, N_A the acceptor concentration and n_i the intrinsic electron concentration at thermal equilibrium. Knowing the built-in voltage, it is possible to accurately describe the SCR region extension as function of an external applied voltage V as described in Eq. (1.8). For convention, the external applied voltage is considered positive when the p-region has a higher potential compared to the n-region. In consideration of a reversely biased diode, external applied voltage results negative, thus SCR region increases.

$$W = \sqrt{\frac{2\epsilon_s}{q} \left(\frac{N_A + N_D}{N_A N_D} \right) (V_{bi} - V)} \tag{1.8}$$

Finally, it is possible to give a one dimensional electric field description in the SCR, knowing

that W_n and W_p are respectively the SCR extension in the n and p region and that the junction is found at $x = 0$:

$$\begin{aligned} \mathscr{E}(x) &= -\frac{qN_A}{\epsilon_s}(x + W_p) \qquad \text{for } -W_p \leq x \leq 0 \\ \mathscr{E}(x) &= -\frac{qN_D}{\epsilon_s}(W_n - x) \qquad \text{for } 0 \leq x \leq W_n \end{aligned} \tag{1.9}$$

Due to the presence of an electric field between two "electrodes" (the n and p diffusions), the reverse biased PhotoDiode can be modeled as a capacitor. In a first approximation, supposing a parallel plate capacitor, the PhotoDiode capacitance can be expressed as:

$$C_{PD} = A \cdot \frac{\epsilon_s}{W} \tag{1.10}$$

where A is the PhotoDiode surface. As previously mentioned, the Active Pixel Sensor technology relies on measurement of voltage drop as function of the collected charge number. The charge-to-voltage conversion is performed in the PhotoDiode; the Conversion Gain (CG), also called Charge-to-Voltage Factor (CVF), is defined as the voltage shift resulting from the addition of one electron in the PhotoDiode. Its theoretical definition is given by Eq. (1.11) and is measured in Volt per number of electrons.

$$CG = \frac{q}{C_{PD}} \tag{1.11}$$

Estimation of the actual PhotoDiode capacitance is though not straightforward. Various methods have therefore been proposed in literature to solve this issue and accurately estimate this important factor [PH03]. In a first approximation it is though possible to say that the conversion gain is highly relying on the PhotoDiode area: the higher the PhotoDiode area, the smaller the conversion gain. But PhotoDiode area is a key parameter in Active Pixel Sensor: the ratio between PhotoDiode area and pixel area determines the Fill Factor (FF), which gives an idea of the amount of photons that can be retrieved and collected by the PhotoDiode compared to the number of incoming photons on the pixel. A fast analysis shows a trade-off between these two factors: higher conversion gain would imply smaller collection area, thus smaller FF.

Fig. 1.10 shows the schematic (a) and the cross-section (b) of 4T pixel implementing Pinned PhotoDiode. It is therefore possible to appreciate how carriers collection and charge-to-voltage conversion is anymore performed on the same node: the Pinned PhotoDiode is devoted only to charge collection and the so-called Floating Diffusion (FD) is devoted to charge-to-voltage conversion. This role separation allows to accurately select the conversion gain without having an impact on the collection area, thus the FF.

Fig. 1.10b shows the cross-section of a 4T pixel, highlighting the Pinned PhotoDiode, the Floating Diffusion and and a new transistor called Transfer Gate (TG). The primary use of TG is to impede or allow charge transfer between the Pinned PhotoDiode and the Floating Diffusion; notably, when the TG is pulsed to the *off* state, the charge transfer between the two nodes is blocked, allowing for charge integration in the Pinned PhotoDiode

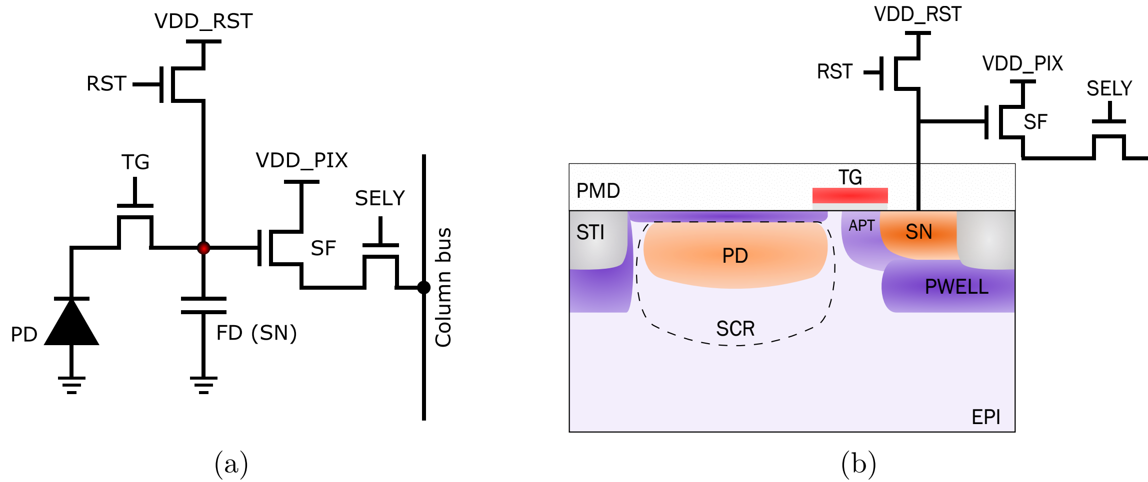


Figure 1.10: (a) Schematic of a 4T pixel containing a pinned PhotoDiode (PD), a Floating Diffusion (FD), the reset transistor (RST), the Source Follower transistor (SF), the selector transistor (SELY) and the Transfer Gate (TG). (b) Cross-section view of the 4T pixel including the same elements plus the PWELL and Anti Punch-Through (APT) doping layers and the Shallow Trench Isolation (STI).

during exposure period; when the TG is pulsed to the *on* state, charges flow from the Pinned PhotoDiode to the Floating Diffusion, determining the end of the exposure period. Once the charges have been transferred, similarly to what is done in 3T pixels, the potential on Floating Diffusion is sampled and buffered through the SF and sent to the line output column through SELY. Another important thing that must be observed is the presence of a so-called “pinning” layer between the PhotoDiode and the Silicon/Oxide interface: this highly doped p-layer is used to separate the n-diffusion from the Silicon/Oxide interface (allowing for an important noise reduction that will be described in Sec. 1.3.3) and to “pin” the maximum PhotoDiode potential to a value referred as V_{pin}. This voltage pinning means that, if the Pinned PhotoDiode is suddenly connected to a deeper well potential ($V_{well} > V_{pin}$), the Pinned PhotoDiode potential increases as charges are being transferred to the neighboring potential until reaching V_{pin}. Once the Pinned PhotoDiode reaches the pinning potential, no electrons are left inside its n-region; this total clearance of free electrons becomes feasible thanks to the scarce presence of electrons inside the Pinned PhotoDiode caused by the double-sided junction. Thanks to this effect, true charge transfer from the Pinned PhotoDiode to a neighboring drain is therefore possible.

1.3.2 Light Sensitivity and Quantum Efficiency

Light Sensitivity can be defined as the image sensor transfer function, relating the output (the output voltage) with the input (incoming photons), generally defined in $\text{mV} \cdot \text{lux}^{-1}$. It is possible to subdivide the transfer function into three main building blocks, in order to give a better understanding of how detection works. Definitions of the three blocks are given

hereafter:

- **Optical Quantum Efficiency (η_o):** We refer to optical quantum efficiency as the ratio of per pixel penetrating photons into the silicon over the number of per pixel incoming photons. Optical quantum efficiency only depends on the pixel structure and technology, as it relates the amount of light that is able to penetrate into the silicon to the total incoming light. Technology plays therefore a fundamental role: optimization of anti-reflection coatings between air and oxide as well as anti-reflection coatings between oxide and silicon are of primary importance to reduce the reflectance of the pixel and thus increase the number of penetrating photons. It has to be kept in mind that pixel architecture also plays a role in the optical quantum efficiency: light gets reflected by metallic interconnections, thus reducing the number of photons reaching the silicon; again this problem can be solved by improving the technological node, some examples have been given in literature using micro-lenses [ABT03], light guides or even double-micro-lenses [Yok+18b].
- **Internal Quantum Efficiency (η_i):** We refer to internal quantum efficiency as the ratio of collected free electrons over the photo-generated electron-hole pairs. Referring to the ability of the pixel to efficiently collect the photo-generated electrons, the internal quantum efficiency is the harder parameter to model because of its dependence on a great number of factors. Technology and pixel design play a main role for this parameter, but surprisingly an important role is also played by the incoming light: as previously seen, light wavelength strongly determines the depth at which electron-hole pairs are generated. As we will see further on in our discussion, the locations at which the incoming light crosses the Silicon/Oxide interface can play an important role on internal quantum efficiency.
- **Charge-to-Voltage conversion:** Though extensively discussed in previous sections, we remind that Charge-to-Voltage conversion models the capability of the system to variate the voltage output as function of the collected electrons. Technology and design can help improving this parameter.

Even though Light Sensitivity can be extensively used to relate the image sensor output voltage to the incoming light illuminance, it does not give us a perception of the system efficiency to absorb and collect the incoming photons. A parameter, named external or overall Quantum Efficiency (QE), has therefore been created to this purpose. Quantum Efficiency models the number of collected electrons per number of incoming photons. Given what said previously, it can be easily seen that:

$$QE = \eta_o \times \eta_i \tag{1.12}$$

We expect Quantum Efficiency to be wavelength dependent for what it has been previously said. It is possible to appreciate the measured Quantum Efficiency as function of wavelength for a commercial CMOS Active Pixel Sensor in Fig. 1.11. In panchromatic Active Pixel Sensor, Quantum Efficiency is generally at its highest value around 500 - 550 nm. It is easy

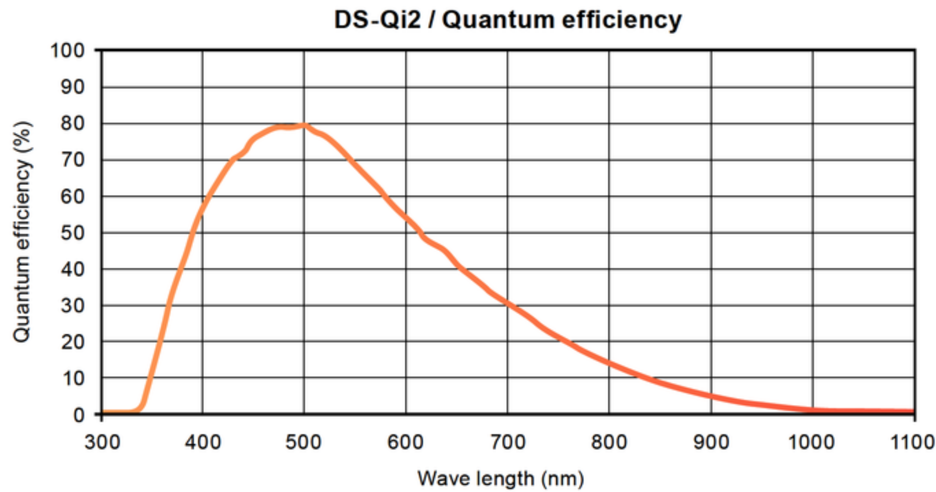


Figure 1.11: Example of panchromatic Quantum Efficiency curve, courtesy of Nikon.

Figure 1.12: Comparison of (a) the standard test image "Lena" and (b) its noisy version, when Gaussian noise has been added in post-process. Definition of image noise is then possible, as the statistical variation of pixel brightness in the image.

to see that Quantum Efficiency decreases with longer wavelength; this is mainly caused by a deeper generation of electron-hole pairs as often pointed out before.

1.3.3 Noise in the Active Pixel Sensor

Noise in an electronic system can be defined as random fluctuations in the information processed by the electronic system itself. In an image sensor, noise could be defined as the

statistical variation in the output signal of each pixel, often seen as a statistical variation of the brightness of each pixel. In order to visually understand the concept of noise, Fig. 1.12 shows a comparison between the standard test image “Lena” and the same image with added Gaussian noise.

With the following, we aim in giving a brief description of some types of noise that are found in the operation of a Active Pixel Sensor. For a more complete vision on noise modeling in Active Pixel Sensor, please refer to [TFEG99]; [Tia00]; [MG10].

1.3.3.1 Photon shot noise

Photon shot noise is the only noise related to the image sensor illumination. It can be defined as the statistical fluctuation of the number of photons impinging onto the image sensor surface. Supposing a uniform illumination of the sensor, the photon arrival onto the sensor surface obeys to the Poisson's statistics; the variance of a Poisson's statistics is represented the square root of its mean, therefore the noise in the image sensor can be directly related to the statistical variation of impinging photons, thus the statistical variation of collected photo-generated electrons. Knowing that incoming photons and collected electrons are related by the Quantum Efficiency, it is possible to define shot noise as following

$$\sigma_{ph} \propto \sqrt{N_{ph} \cdot QE}. \tag{1.13}$$

where N_{ph} is the mean number of impinging photons onto one pixel surface.

1.3.3.2 Reset noise

Reset noise is the thermal noise associated with the reset operation of a capacitor. Reset noise is generated by random thermally induced motion of electrons in resistive regions through which the capacitor is charged, thus leading to statistical fluctuations of the potential on the capacitance. In a linear RC circuit analysis, it can be demonstrated that the noise associated to the charge operation of a capacitor is modeled as follows:

$$\sigma_{kTC} = \sqrt{\frac{k_B \cdot T}{C}}, \tag{1.14}$$

where k_B is the Boltzmann constant, T is the temperature and C is the capacitance.

In the Active Pixel Sensor previously presented, the reset operation is performed onto the Floating Diffusion through the RST transistor. Modeling the Floating Diffusion as a capacitance and the RST transistor as a resistance (under given operation conditions, i.e. soft reset [MG10]) can easily be related to Eq. (1.14).

1.3.3.3 Dark Current shot noise

It is supposed that leaving an image sensor in the dark would result in a null output signal, since no photons are being collected. This happens not to be real, since charges can be generated through thermal activation and collected by the PhotoDiode (or other capacities, like the Floating Diffusion) and contribute to the output signal. This signal, often called Dark Current (DC) is strongly dependent on the temperature as well as on the crystalline structure of the silicon, the quality of the interfaces with the oxide layers, the pixel layout and the presence of electric fields [Goi+12]. Further details on the Dark Current phenomenology, analysis and improvements can be found in [Jan+01]; [Goi+12]; [Mar+17]; [Riz+18].

Dark Current in itself cannot be defined as a noise, since it is not represented by a statistical fluctuation, but rather as a constant base signal (at a given structure, temperature and operating conditions). Nevertheless, statistical fluctuations of the Dark Current are present, since the thermal generation of charges obeys to the Poisson's statistics. In a similar manner to what shown for the photon shot noise in sec. 1.3.3.1, it is possible to define a Dark Current shot noise as the square-root of the mean number of charges N_{DC} contributing to the Dark Current at a given structure, temperature and operating conditions:

$$\sigma_{DC} \propto \sqrt{N_{DC}}. \tag{1.15}$$

1.3.3.4 Spatial noise

Differently from what previously seen, spatial noise represents the pixel-to-pixel output variation across the whole sensor under uniform illumination. Spatial noise is mainly due to device and interconnect parameter variations across the sensor, thus being highly related to process mismatch across the sensor. Spatial noise is "fixed" for a given sensor, but varies from sensor to sensor. Contributions to spatial noise are briefly listed in the following.

- Fixed Pattern noise (FPN) can be defined as the spatial variation in the pixel output values under uniform illumination. FPN main contributions in an Active Pixel Sensor are given by column and in-pixel amplification, the root cause being in the transistors threshold voltage mismatch. FPN is independent of illumination conditions.

- Dark Current Non-Uniformity (DCNU) can be defined as the pixel-to-pixel mean Dark Current mismatch. This is mainly due to fabrication process, pixel design and the neighboring elements (as for example for pixel at the edge of the array).

- Photo Response Non-Uniformity (PRNU) can be defined as the spatial variation of pixel-to-pixel response to incoming light. This includes QE and conversion gain spatial mismatch as well as column readout gain mismatch.

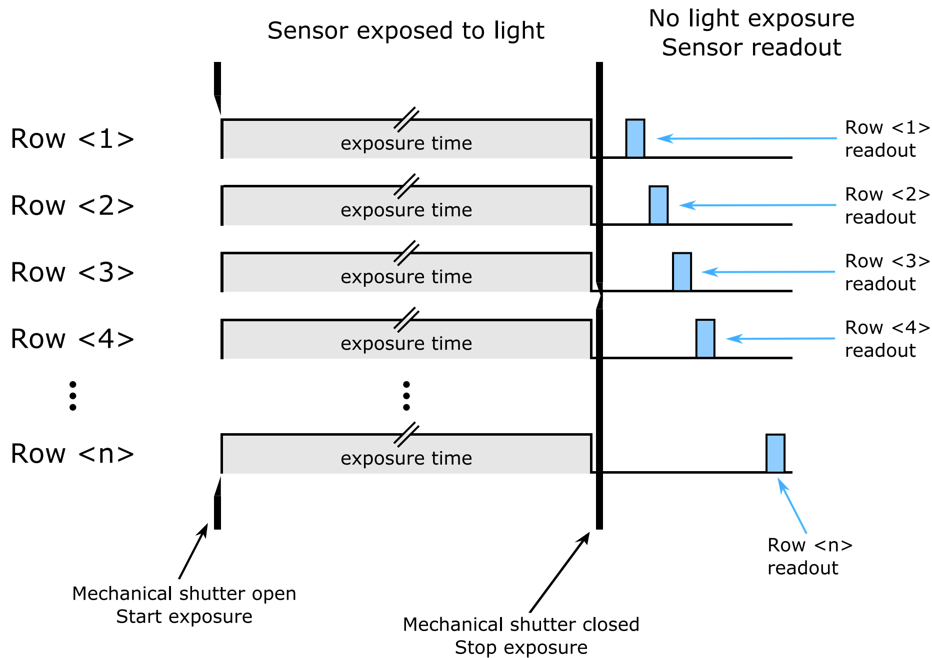


Figure 1.13: Example of mechanical shutter frame capture operation. The exposition starts via the aperture of the mechanical shutter and ends with its closure. After closing the shutter, no light is allowed onto the sensor and readout can start.

1.4 The Electronic Shutter

« Who does not want to shoot some nice pictures on a nice sunny summer day? We grab our last model camera and we're ready to shoot some pictures. The first one here it comes, we choose the lens aperture, the point onto which to focus and we press that button: "ka-chick", that is the sound we here. But wait, what is that sound? »

It is common to hear a click when shooting pictures: this is due to a curtain that opens up, allowing sensor exposure to light, and closes after the selected exposure time to impede any more light to come in. This curtain represents a *Mechanical Shutter*. The operation scheme of the mechanical shutter is presented in Fig. 1.13; the shutter opens up allowing for a global array exposure, then the shutter closes ending the exposure period, once the shutter is closed, no light reaches the image sensor though allowing for a row-by-row readout. The mechanical shutter has served generation of photographers, allowing for highly synchronized exposure times, high reliability and reduced spatial distortions. Though, for some applications, an electronic shutter would be preferred in order to avoid any moving part.

1.4.1 Rolling and Global Shutter operating modes

The electronic shutter defines the capability of the image sensor to set the exposure time without the use of any mechanical part, thus turning *on* and *off* the image sensor. The global

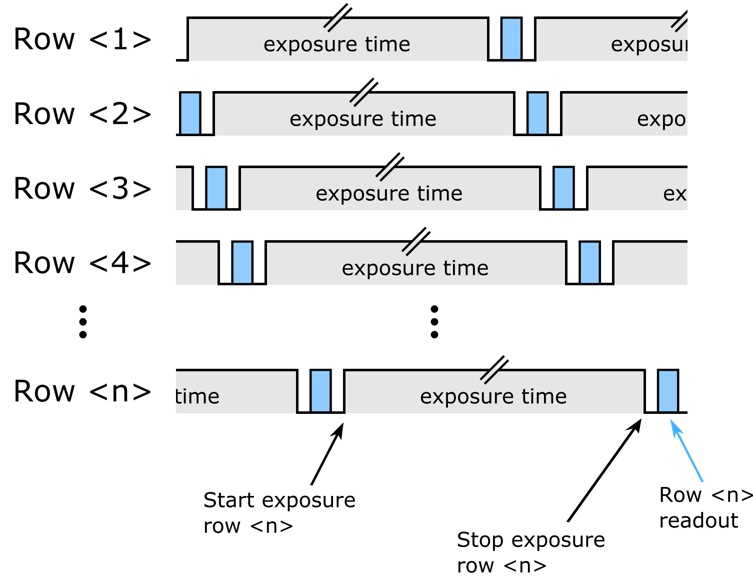


Figure 1.14: Example of Rolling Shutter operation mode. The integration period does not start synchronously in the entire array, but it is row-by-row shifted. At the end of its integration period, the row can be readout and restart its integration, triggering the end of the successive row integration and its read out and so on. In this way, each row has the same integration time.

array exposure followed by a row-by-row readout, as with the mechanical shutter, becomes impossible: the sensor is still kept under illumination conditions while doing the readout, thus causing an exposure imbalance between the different rows. Moreover, direct readout of the entire matrix proves to be impossible, due to the high number of pixels in the array and the excessive number of interconnections that would be required. One way to solve this issue is to operate the whole sensor on a row-by-row basis, using sequential exposure and readout; one row at a time can be efficiently readout, keeping a good trade-off between complexity and speed. This new operating mode is better defined as Rolling Shutter (RS). A visual explanation of the Rolling Shutter mechanisms is presented in Fig. 1.14; sequential row exposure is performed thus allowing for sequential row readout and same exposure time throughout the whole array. Even though Rolling Shutter mode proves its efficiency, spatial distortions may be caused by the non-synchronous exposure of the array, especially when imaging fast-moving objects.

In order to improve the Rolling Shutter mode, thus allowing for a global synchronous exposure of the matrix, the acquired information should be stored somewhere before being accessed for readout. Global synchronous transfer and storage of information allows for the same exposure time throughout the entire array. This operating mode is called Global Shutter (GS) and allows for usage of the electronic shutter releasing the problem of spatial distortions caused by the rolling operation. The work operation of Global Shutter can be appreciated in Fig. 1.15. The array is globally exposed for a certain amount of time, the acquired information is then globally transferred to storage, readout is finally performed in a row-by-row fashion

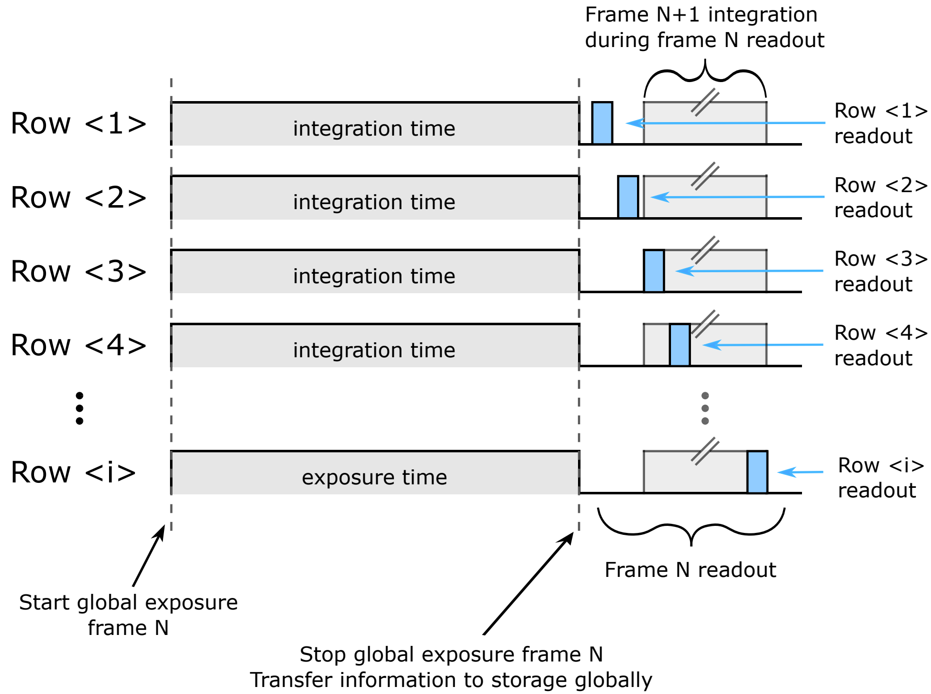


Figure 1.15: Example of Global Shutter operation mode. The integration start synchronously on the whole array. At the end of integration, a global transfer is performed, the information stored and readout row by row. Given the separation between the exposure phase and the storage/readout phase, a second integration can be started during the previous frame readout.

because the same constraints for the Rolling Shutter mode still stand.

1.4.2 Correlated Double Sampling

Double Sampling (DS) is a technique often used to accurately measure sensors output suppressing undesired offset. In the case of image sensors, Double Sampling is exploited to suppress offset noise as the in-pixel FPN, being one of the main disadvantages of Active Pixel Sensor imagers in comparison with CCD imagers, and reset noise. Double Sampling requires sampling of two values, one at known conditions and one at unknown conditions. The two values are then held and subtracted in order to retrieve the pixel output. The value at known condition is found to be the voltage level of the Floating Diffusion right after the reset operation; once sampled and held, we refer to it as V_{REF}. The value at unknown condition is the voltage level of the Floating Diffusion once the integration is terminated (and charges are transferred from the PhotoDiode to the Storage Node in the case of 4T or 5T pixels); once sampled and held, we refer to it as V_{SIG}. The pixel output is then retrieved as the subtraction of V_{REF} and V_{SIG}, defined then as the voltage drop from the reference level as function of the collected charges.

Double Sampling operation is defined *correlated* if V_{SIG} is sampled after V_{REF}, while is

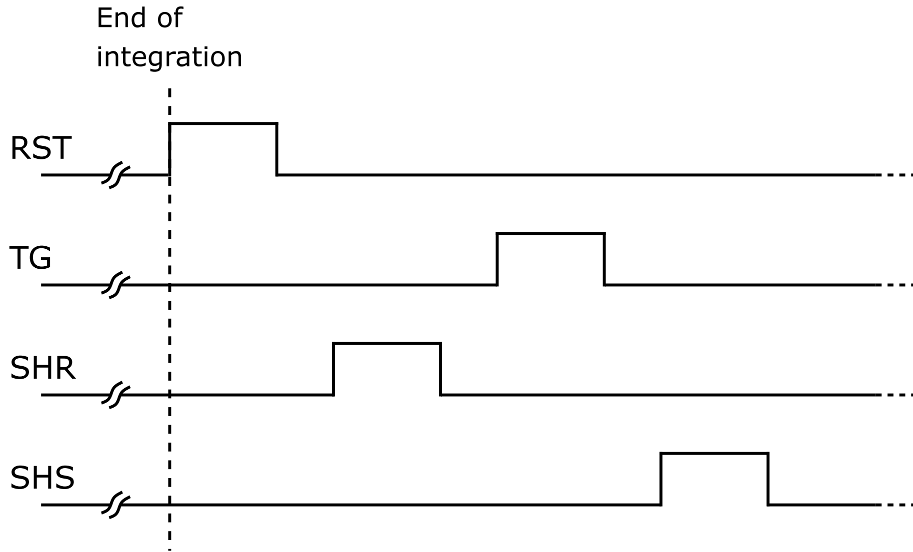


Figure 1.16: Time diagram of Correlated Double Sampling (CDS) readout scheme in a 4T pixel. Right before the end of the integration, the Floating Diffusion is reset via the RST command and the reset level sampled via the SHR command. End of integration is then determined through the TG command that transfers all integrated charges onto the Floating Diffusion. Finally, the signal level is sampled via the SHS command.

defined *non-correlated* if V_{SIG} is sampled before V_{REF}. Definition of correlation in Double Sampling is crucial for understanding which type of noise is being suppressed. Taking the example of Non-Correlated Double Sampling (NCDS) the sampled V_{REF} is the result of a reset operation performed after the sampling operation of V_{SIG}, thus the two being non-correlated; correlation is unimportant for time-constant noise suppression, thus spatial noise (in this case in-pixel FPN) is suppressed by Non-Correlated Double Sampling; on the other hand temporal noise, as reset noise, is not suppressed by Non-Correlated Double Sampling, due to temporal variability indeed, thus Correlated Double Sampling (CDS) is required.

The time diagram of command signals exploited to integrate and readout a 3T pixel Active Pixel Sensor has been previously shown in Fig. 1.9. SHR and SHS command signals are exploited to sample and hold the voltage level of the Floating Diffusion respectively after the reset operation (V_{REF}) and at the end of the integration (V_{SIG}). Due to the obliged sequential readout operations, reset operation of the Floating Diffusion and V_{REF} sampling are performed after sampling of V_{SIG}, thus leading to Non-Correlated Double Sampling operation. Non-Correlated Double Sampling operation in 3T pixels Active Pixel Sensor suppresses in-pixel FPN, though increasing the reset noise by $\sqrt{2}$ (both V_{REF} and V_{SIG} samples carry their distinct reset noise, thus subtraction of the two voltages results in noise summation).

In order to allow Correlated Double Sampling operation on Active Pixel Sensor, a separation of the integration and readout phases is required. It has been previously shown that this has been achieved through integration of a Pinned PhotoDiode and a TG; readout operations will still be performed on the Floating Diffusion while integration is happening on the Pinned

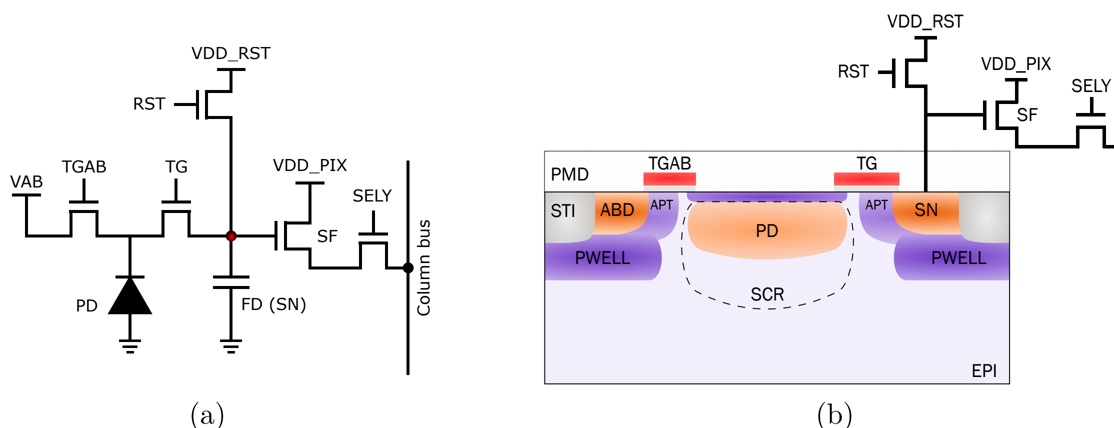


Figure 1.17: (a) Schematic of a 5T pixel containing a pinned PhotoDiode (PD), a Floating Diffusion (FD) which is used as a Storage Node (SN), the reset transistor (RST), the Source Follower transistor (SF), the selector transistor (SELY), the Transfer Gate (TG) and AntiBlooming Gate (TGAB) with its drain (ABD). (b) Cross-section view of the 5T pixel including the same elements plus the PWELL and the Anti Punch-Through (APT) doping layers and the Shallow Trench Isolation (STI).

PhotoDiode. Fig. 1.16 shows the time diagram of command signals exploited to integrate and readout a 4T pixel Active Pixel Sensor. It is now evident that reset operation and V_{REF} sampling can be performed just before the end of integration, operated by TG; V_{SIG} sampling happens soon after.

As a summary, it is possible to measure the voltage drop due to charge integration on a Floating Diffusion exploiting a Non-Correlated Double Sampling scheme. The resulting output will carry temporal noise, but the in-pixel spatial noise can be suppressed. It is nevertheless possible to measure the voltage drop due to charge integrated on the Pinned PhotoDiode and transferred to the Floating Diffusion exploiting a Correlated Double Sampling scheme. Correlated Double Sampling allows for reduction of temporal noise, notably suppression of reset noise, and suppression of in-pixel spatial noise.

1.4.3 Global Shutter Active Pixel Sensor: a concept

Transferring this operation mode to the pixel structure, the need for a Storage Node (SN) is evident. In a 4T pixel, the simplest solution would be to exploit the Floating Diffusion as the Storage Node; the TG would therefore become globally commanded allowing for a global transfer of charges from all the Pinned PhotoDiodes in the array to their respective Storage Nodes. Unfortunately, under strong light conditions the Pinned PhotoDiode could saturate while the Storage Node is queued to be readout, thus spilling the overflowing electrons towards the Storage Node; this would cause inefficiency in the electronic shutter *off* operation, where it has been supposed that the image sensor would not respond to incoming light. In order to solve this issue, a fifth transistor can be added to the pixel structure, consisting in a transfer

gate called TGAB and its associated drain ABD, as shown in Fig. 1.17. Even though the new transistor is called "AntiBlooming", it does not only serves the purpose of an overflow preferred path when weakly polarized to avoid the blooming effect [And+91], but also as the "start integration" command for Global Shutter operation when integration of frame N begins during readout of frame N+1 (otherwise called *Pipelined Global Shutter* or *Integrate While Read*). Moreover, in order to perform global operations, the TG, RST and TGAB are globally activated.

The Global Shutter Active Pixel Sensor is operated as follows: a global reset of the array through RST and TG is performed, starting the exposure; after the exposure time, the acquired charges are globally transferred activating the TG; readout is then performed in a row-by-row fashion through the SF and the SELY.

In Rolling Shutter mode, the Pinned PhotoDiode Active Pixel Sensor allows Correlated Double Sampling operation. When exploiting the Global Shutter mode on 4T/5T pixel Active Pixel Sensor, the Correlated Double Sampling sequence is no more applicable; it is impossible to acquire and store the reference voltage V_{REF} of the entire array before global charge transfer is performed, this would require a massive storage site of the same size of the array, which is, if not unfeasible, at least very impractical. Non-Correlated Double Sampling is though still available at least to perform FPN suppression. One straight way to perform Correlated Double Sampling on a Global Shutter Active Pixel Sensor, similarly to what has been first done in the passage from 3T to 4T, would be to give the Floating Diffusion the solely purpose of charge-to-voltage conversion. Adding an alternative Storage Node between the photosensitive element and the Floating Diffusion, with transfer gates commanding the passage from Pinned PhotoDiode to Storage Node and from Storage Node to Floating Diffusion, would free the Floating Diffusion from storage duties. This and many other solutions have been undertaken, as shown in literature, in order to develop one pixel allowing for Correlated Double Sampling operation. A closer analysis to improvements on Global Shutter pixel will be performed in the following chapter.

1.4.3.1 Global Shutter operating modes

Given its intrinsic nature of separating integration from storage/readout phase, a Global Shutter CMOS Image Sensor can be operated in two different modes.

ITR The Integrate Then Read (ITR) mode, also called Triggered Mode, allows separation of the integration and readout phases. Generally, an external trigger starts the integration, the ending of which is followed by array readout; continuous imaging is generally not exploited. This mode of operation is generally preferred in industrial inspection tasks [Wit+03].

IWR The Integrate While Read (IWR) mode, also called Pipelined Mode, allows integration of the entire array meanwhile the readout operations are being performed. This mode is exploited in case of a short array integration time required (high illumination of the

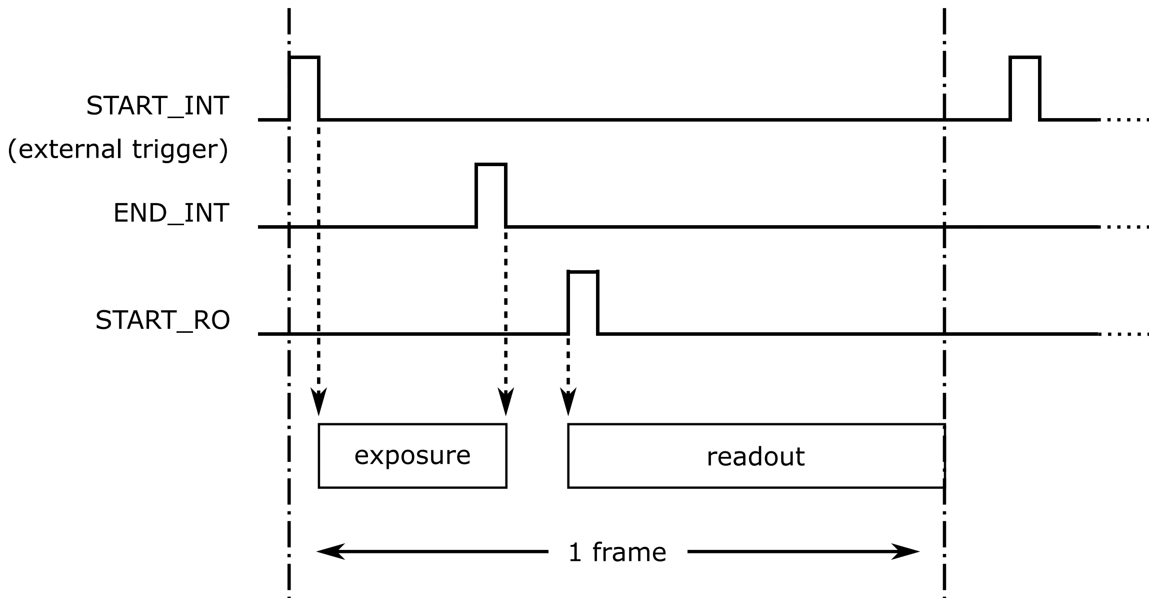


Figure 1.18: Time diagram of a Global Shutter CMOS Image Sensor operated in Integrate Then Read (ITR) mode. START_INT command (often an external trigger) determines the beginning of the array integration phase, its end is set by command END_INT. At the end of the integration of frame N, frame readout phase starts following the command START_RO. The frame length is determined by the length of readout phase plus the length of the integration phase.

scene) as well as high frame rate, the readout operation being generally longer than the array integration time. Such mode of operation is needed for continuous high speed imaging, in applications of motion analysis [Wit+03].

Fig. 1.18 shows an example of the time diagram to operate Global Shutter CMOS Image Sensors in the Integrate Then Read mode; a trigger, generally an external signal, gives the start of frame N integration. At the end of its integration, the frame is readout and the sensor can restart its operation at the next trigger signal. The minimum frame rate is set by the sum of the readout period plus the integration period. Fig. 1.19 shows an example of the time diagram to operate Global Shutter CMOS Image Sensors in the Integrate While Read mode; the integration of frame N+1 starts during frame N readout and ends correspondingly. Frame N+1 readout starts soon after. The minimum frame rate is set by the frame readout time.

Global Shutter CMOS Image Sensor are often operated in high speed imaging at strong light conditions. This requires a fast operation of the sensor, which translates in a high frame rate and thus a reduced frame time. The Integrate While Read mode allows the highest frame rate, given that the maximum time between one frame and the other is just the readout time. Therefore, the most common Global Shutter CMOS Image Sensors on the market are operated in the Integrate While Read mode.

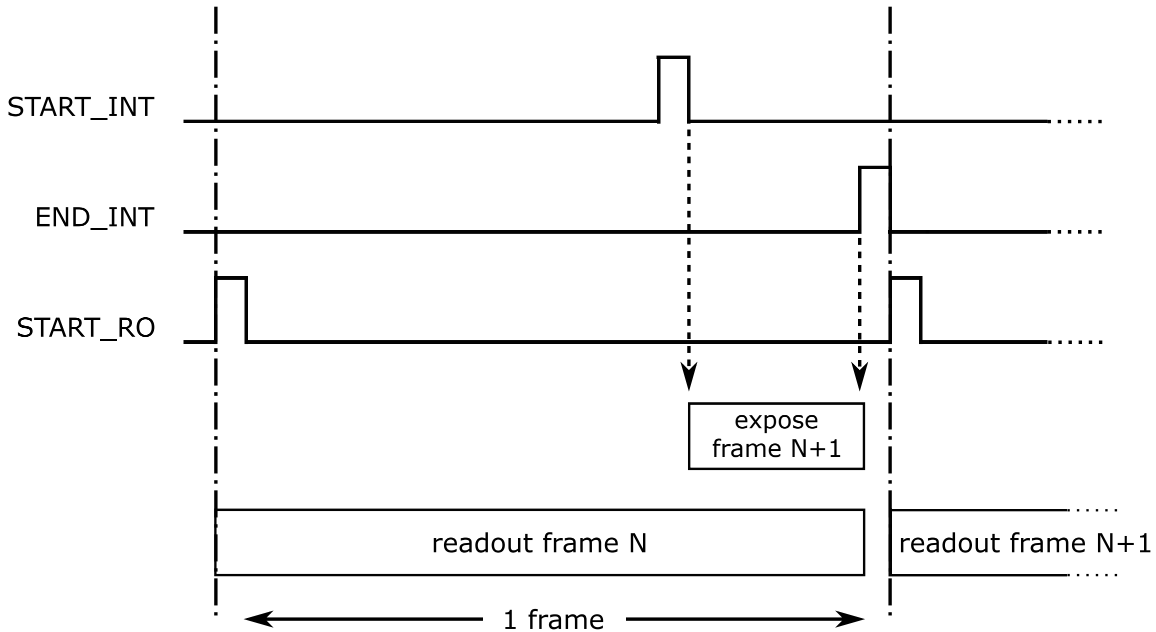


Figure 1.19: Time diagram of a Global Shutter CMOS Image Sensor operated in Integrate While Read (IWR) mode. START_INT command determines the beginning of the array integration phase, its end is set by command END_INT. Exposure of frame N is performed during readout of frame N+1. Readout phase starts with the help of the START_RO command. The frame length is determined by the length of readout phase.

1.5 A figure of merit: Parasitic Light Sensitivity

Once global exposure and Correlated Double Sampling operation problems are solved, one has to model all issues relatives to the presence of an in-pixel storage element. Notably, as previously seen in Sec. 1.4.3, the storage element is sensitive to light and, even if it might look negligible because its light sensitivity is generally smaller compared to the main photosensitive element, its impact on the output frame can be of some importance, notably during the storage and readout phase.

It is possible therefore to make a comparison between the mechanical shutter and the Global Shutter operation modes: as it has been shown in Fig. 1.13 and 1.15, the two operating modes have the same exposure plus readout pattern, though they differ by the presence (or absence) of a mechanical element used to impede sensor illumination during the storage and readout phase. In Global Shutter mode, no mechanical curtains are used to block the incoming light, but the solely operation of the pixel should be sufficient to efficiently reduce the influence of the incoming light during the storage and readout phase. In other words, to simply turn down the photosensitivity while the current frame is being readout. Non-negligible light sensitivity of the storage element though lowers the efficiency of the switch-off mechanism in Global Shutter CMOS Image Sensors. It is possible to define a parameter called

Global Shutter Efficiency (GSE) which determines the capability of the sensor to reproduce the behavior of the mechanical shutter, or better to switch-off its light sensitivity during storage and readout. Global Shutter Efficiency is defined in Eq. (1.16), where PLS is defined as Parasitic Light Sensitivity.

$$GSE = 1 - PLS \tag{1.16}$$

Parasitic Light Sensitivity (PLS) defines the sensor sensitivity during *off-state* in comparison to the sensor sensitivity during the *on-state*. In other words Parasitic Light Sensitivity defined the amount of light, defined as parasitic light, that the sensor "sees" during the *off-state* in comparison to the amount of light that the sensor "sees" during the *on-state*. It should be therefore clear that the parasitic light shows up during the storage and readout phase, thus it represents the amount of light being collected by the storage element; conversely, during the *on-state*, light is being collected on the main photosensitive element. One can therefore model the Parasitic Light Sensitivity as follows:

$$PLS = \frac{\mathscr{S}_{SN}}{\mathscr{S}_{PD}} = \frac{QE_{SN}}{QE_{PD}} \tag{1.17}$$

where $\mathscr{S}_{SN}$ and $\mathscr{S}_{PD}$ are respectively the light sensitivity of the Storage Node and the PhotoDiode. As explained in Sec. 1.3.2, the light sensitivity and the Quantum Efficiency are related between each other by a multiplicative constant, thus the two ways of defining the Parasitic Light Sensitivity are equivalent.

It is important to notice that the simple Storage Node sensitivity would not be useful for image sensor comparison: we could take two pixels, same dimensions and the Storage Node has the same sensitivity, but the two pixels differ in the PhotoDiode dimensions, thus PhotoDiode sensitivity; one PhotoDiode would be bigger, allowing fo a bigger sensitivity, and the other one would be smaller. In principle, if we compare the two pixels just by the Storage Node sensitivity, we could say that the two pixels capability to mimic the mechanical shutter is equal. Though, we think of Parasitic Light Sensitivity as a perturbation to the external picture due to the presence of light. It is evident that if perturbation has lower impact on the output, the Global Shutter Efficiency of that image sensor is higher. Therefore, if at identical light conditions, the two Storage Node would collect the same number of charges, while the two PhotoDiode would collect a different number of charges, as function of their sensitivities. It is straightforward to analyze that the same number of charges parasitically collected by the Storage Node would have lower impact on the total number of charges collected by the big PhotoDiode, compared to the small one. Therefore, Storage Node sensitivity alone would not be the best parameter to understand how much the sensor is able to mimic the mechanical shutter functions, but a ratio with PhotoDiode sensitivity is therefore required. Parasitic Light Sensitivity, as defined by Eq. (1.17) would be the best shot we have to compare two different image sensors and deduce which of the two is better at mimicking mechanical shutter functions. The equation make us also understand that there are two parameters with which to play if we want to increase the Global Shutter Efficiency, thus reducing the Parasitic Light Sensitivity: either we reduce the Storage Node sensitivity or we increase the PhotoDiode one.

It is of interest to spend few words on the different definitions of Global Shutter Efficiency

that can be found. At the very beginning, the definition of Global Shutter Efficiency was the one given by Eq. (1.16) [Mey+11]; [Kry13]; [Yas+11]. With the increase of performances in the Global Shutter Efficiency, the percentage notation became outdated and people started using more the ratio definition of Parasitic Light Sensitivity [DWG11]; [Kon+15]; [Oik+16], especially in the form of dB, for an easier appreciation of very low Parasitic Light Sensitivity ratios. Given that Parasitic Light Sensitivity is smaller than one, the dB value would result negative; therefore, some started exploiting the Parasitic Light Hardness (1/PLS) definition, thus showing a positive value and easier to directly grasp the performances [Yok+18a]. Nevertheless, some paper report their Global Shutter Efficiency value as a ratio, thus leading to confusion with the Parasitic Light Hardness (1/PLS) parameter [Vel+13]; [Geu+15]. *This manuscript will exploit Parasitic Light Hardness (1/PLS)* as the reference parameter for determining the performances of a Global Shutter CMOS Image Sensor.

1.6 State-of-the-Art Global Shutter CMOS Image Sensor

The need for a high speed CMOS Image Sensor that could replace the Interleaved CCD drove the research to find a solution to create a “snapshot” CMOS Image Sensor, also defined as Global Shutter, at the end of the 90s [Ste+99]. From that moment, the community had started developing these new types of CMOS Image Sensor and soon realized that a parasitic signal (or even called “a blur tail”) started to appear in relation with this new shutter type [Wit+03]; [ITK04]; [Don+05]; [Kry07]. The first Global Shutter CMOS Image Sensors were based on the 5T Pinned PhotoDiode pixel architecture, thus impeding the implementation of Correlated Double Sampling to reduce noise floor. Reduction of kTC noise was nevertheless of major importance to reduce the total noise floor and thus increasing the SNR to reach 4T Rolling Shutter performances that had a better SNR given the implementation of Correlated Double Sampling. Some different architectures begun to appear, allowing charge storage in a separate node from the Floating Diffusion at the cost of increasing the transistor count [Lau+07].

The information integrated in the PhotoDiode had therefore to be stored. Two storage method appeared:

1. **Charge storage.** Storing charges under a Storage Gate (SG) was one of the implemented solution [Sol+11]; [Sak+12]; [Kry13], given that this type of charge transfer has been frequently done in the CCD era. Low Global Shutter Efficiency were though limiting their success. On the other hand, Storage Diodes (SD) were exploited as well, though they were posing some technological difficulties, as the efficient transfer between the PhotoDiode and the SD [Yas+09]; [YIK11]; [Vel+13].
2. **Voltage storage.** In order to find an alternative to the limitations of charge storage, voltage sampling on in-pixel capacitances was foreseen. In this case, charges were classically transferred to the Floating Diffusion, its voltage sampled by the SF transistor and transferred to an in-pixel capacitance. A supplementary in-pixel capacitance was exploited to store the reset signal, thus allowing for the implementation of the Correlated

Double Sampling technique [Wan+10]; [Mey+11]; [Mey14]; [Sta+18]. In other cases, two capacitances were exploited as a clamp on which the Correlated Double Sampling operation was implicitly performed [DWG11]; [DWI11]; [Toc+13].

As Global Shutter Efficiency performances were limiting the exploitation of charge storage based Global Shutter CMOS Image Sensors, voltage based Global Shutter CMOS Image Sensors had taken a large footprint on the market. Nevertheless, their limitations soon show up, as the integration of additional capacitances were adding more kTC noise to the noise floor (readout noise could go from 10 e^- upwards). In order to keep the noise floor low, large capacitances had to be exploited, thus limiting the pixel shrinking capabilities. Some techniques were exploited to circumvent the issue, as the shared readout electronics (two pixels sharing one readout circuitry) [WBM13], though adding supplementary issues as the non-seamless shutter operation that had to be divided due to the shared readout. On the other hand, MOS and especially MIM capacitances were a great solution to improve the Global Shutter Efficiency performances, given their relatively low sensitivity to parasitic light[1].

Improvements in the technological processes allowed for the development of both voltage and charge storage Global Shutter with enhanced performances. 3D integration allowed to integrate the storage capacitances on a second wafer sandwiched on top of the first wafer containing the pixel array; the second wafer allows for the integration of larger capacitances thus improving the noise floor as well as resulting in exceptional Global Shutter Efficiency performances (up to 180 dB!!) [Aok+13]; [Kon+15]; [Kon+16a]. An example of a two wafers 3D integration for Global Shutter CMOS Image Sensors is shown in Fig. 1.20. 3D integration currently represents the State-of-the-Art for voltage storage Global Shutter CMOS Image Sensors.

At the same time, development of improved light convergence and confinement through micro-lens, light pipes and light shielding structures, as for example the Tungsten Buried Light Shield (WBLS) consisting in a layer of tungsten close to the Si/SiO_2interface, allowed for the rediscover of charge storage Global Shutter CMOS Image Sensors with improved Global Shutter Efficiency performances (thanks to a better handling of impinging light) [Kaw+16]; [Vel+16]; [Sek+17]; [Kob+18]; [Lah+17]; [Kum+18], drawing the advantage of low noise performances. Examples of light guide, WBLS and double micro-lens are shown in Fig. 1.21.

Some other enhanced solutions include the vertical PhotoDiode voltage domain architecture [Sta+18] and its derivation onto the Capacitive Deep Trench Isolation (CDTI) allowing the integration of vertical fully depleted PhotoDiode and Storage Node (SN) [Tou+18]; [Roy+19]

The current State-of-the-Art for charge storage Global Shutter CMOS Image Sensors is represented by the implementation of a double stacked micro-lenses, light pipe and WBLS, allowing an enhanced confinement of the impinging light towards the PhotoDiode [Yok+18b]; [Miz+20].

[1]For sake of clarity, MIM capacitances are insensitive to parasitic light. Nevertheless, they are connected to a transistor diffusion which is instead sensitive to parasitic light. MOS capacitances are sensitive to parasitic

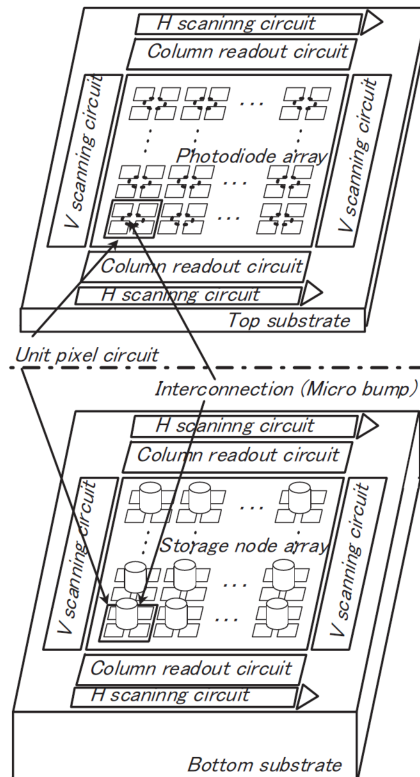


Figure 1.20: 3D integration on two wafers to improve Global Shutter Efficiency (GSE) for a voltage storage Global Shutter CMOS Image Sensors [Kon+16b]. The two wafers are bonded via micro-bumps. Due to 3D integration, the array wafer must be back-thinned to allow impinging light from the backside, also called BackSide Illumination (BSI).

A resume of the performances in terms of Parasitic Light Hardness (1/PLS), temporal noise and pixel pitch is shown in Fig. 1.22. The group in blue represents the charge storage based pixels, the group in red represents the voltage storage based pixels and the group in yellow represents the voltage storage based pixel exploiting 3D integration. It is possible to notice from Fig. 1.22a that charge storage based pixels generally have a smaller pitch with respect to their voltage storage based counterparts as well as a lower noise floor, as shown in Fig. 1.22b. On the other hands, voltage storage based pixels show better Parasitic Light Hardness (1/PLS) performances, especially in the case of 3D integration.

1.7 Challenges and motivations

This chapter has presented an historical development of image sensing, from film to solid state cameras, from CCD to CMOS technology. One of the multiple applications of image sensing has been presented as well from its historical point of view and has set the background for

light, though the subtraction operation of the capacitance pair is efficient in suppressing parasitic light.

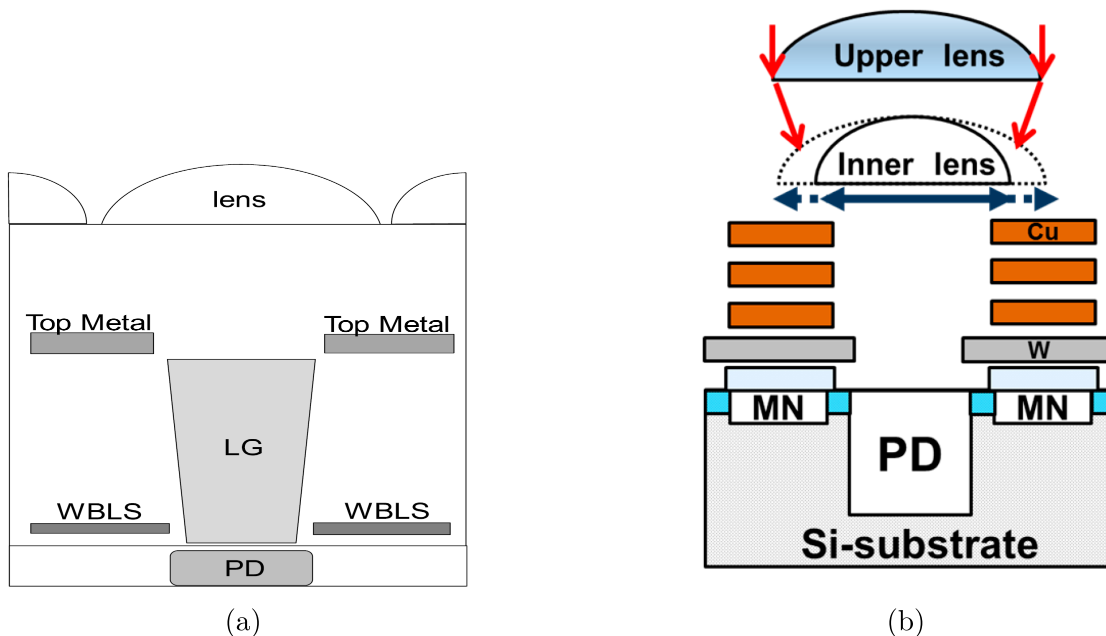


Figure 1.21: Various techniques to improve Global Shutter Efficiency (GSE) in charge storage Global Shutter CMOS Image Sensors. (a) Light Guide (LG) and Tungsten Buried Light Shield (WBLS) [Vel+16]. (b) Double micro-lens [Yok+18b] where PD represents the PhotoDiode and MN represents the Memory Node, or Storage Node.

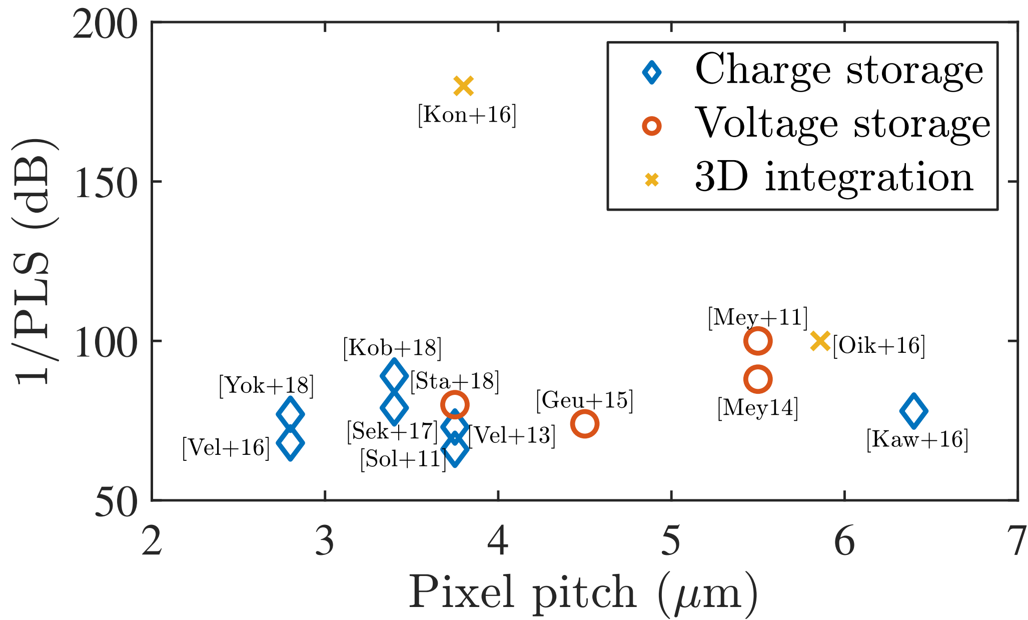
this thesis work.

Further on, the discussion has been centered on the development of image sensors exploiting the CMOS process, giving an explanation of the physical mechanisms behind solid-state photo-detection. Following an historical point of view, different active pixel sensor architectures have been presented, from the 3T to 4T, 5T and more, giving an insight on the reasons that have brought to these types of pixel enhancement. The different figures of merit that characterize the active pixel sensors have been presented and detailed, with the intention in laying the foundation for the upcoming work.

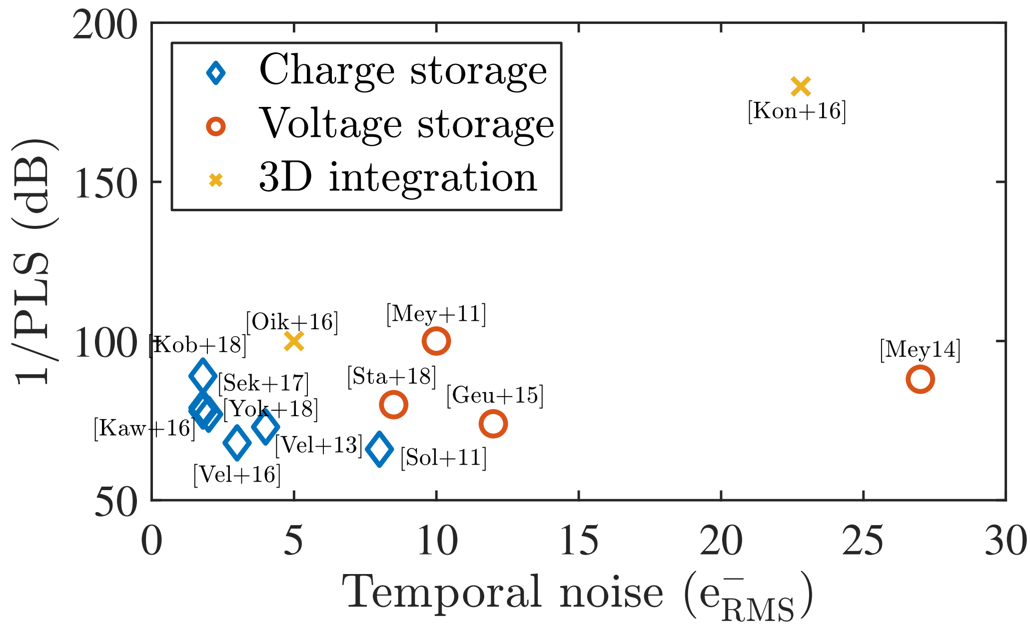
An important part of this chapter has been focused on the explanation of the electronic shutter, in comparison with the mechanical one. This has brought to the description of the motivations behind the development of Global Shutter CMOS Image Sensors and the description of one of its main figures of merit, the Parasitic Light Sensitivity. Finally, an historical development of Global Shutter CMOS Image Sensors has been presented, describing the different technological improvements that have led to the actual State-of-the-Art.

The upcoming work is inserted in the mainframe of Global Shutter CMOS Image Sensors. Various solutions to the Parasitic Light Sensitivity problem have been presented in literature, though lacking of a general model to describe the phenomenon. Aim of this work is to develop a method for modeling Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors,

that would allow for performance improvement in a cost-effective way as well as describing the main phenomena that are related to this non-ideal performance. Moreover, this work aims to define and develop a general characterization method for Parasitic Light Sensitivity that is applicable to the vast majority of Global Shutter CMOS Image Sensors, thus allowing for a better comparison between the different products. Finally, this work aims to analyze the feasibility of post-process Parasitic Light Sensitivity mitigation methods, exploring a cost-effective alternative approach to process enhancement to improve the sensor performances.



(a)



(b)

Figure 1.22: Overview of the main Global Shutter pixels presented in literature, classified per (a) pixel pitch and (b) temporal noise as function of their Parasitic Light Hardness (1/PLS). The blue group represents the charge storage based pixels, the red group represents the voltage storage based pixels and the yellow group represents the voltage storage based pixel exploiting 3D integration.

Chapter 2

Developing a method for modeling Parasitic Light Sensitivity

As previously discussed in Chapter 1, the usage of CMOS Image Senors (CIS) establishes constraints in detection of fast moving object without any spatial distortion; accurate detection relies on the capability of the sensor to acquire the scene in a global and synchronous way throughout the entire array, paying careful attention to the impinging stray light during image readout. In some specific cases, as for example commercial photography, the issue can be tackled through use of a mechanical shutter, allowing synchronous exposure of the entire array when open and a stray-light-less readout phase when closed. Some other applications, as for example film making, automotive sensing or Earth observation from space, require the use of an electronically-controlled shutter; Rolling Shutter (RS) mode cannot be exploited, posing a problem when imaging fast-moving objects or when the camera itself moves fast due to its non-synchronous array exposure, so Global Shutter CMOS Image Sensors have therefore been developed. Nevertheless, constant sensor exposure to light, notably during frame readout, can cause uncontrolled perturbation throughout the entire array; this perturbation is unknown a priori being dependent on the light conditions during frame readout. Global Shutter CMOS Image Sensors performances strongly depend on their capability in reducing sensitivity to the parasitic light.

The constant race to shrink pixel dimensions brings the issue of the Parasitic Light Sensitivity (PLS) in Global Shutter CMOS Image Sensors to another level; improving charge collection by the PhotoDiode (PD) has become more and more difficult as well as guiding the photon flux towards specific locations, especially in small dimensions pixels. Moreover, even if the Parasitic Light Sensitivity issue is widely known in the scientific and industrial image sensor community, its behavior regarding incoming light parameters remains mostly fuzzy; understanding and modeling of Parasitic Light Sensitivity are therefore highly required, providing guidelines towards an efficient and cost-effective improvement of Global Shutter CMOS Image Sensors.

This chapter aims to give an understanding on the phenomena that are responsible for the degradation of the sensor output caused by its Parasitic Light Sensitivity. In particular, knowledge of this phenomena will lead to the development of methods for modeling Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors through optical and transport simulations. Notably, two methods have been developed within this scope; results are then compared to TCAD simulations and, in view of a successive usage of the method for real

pixel modeling, advantages and drawbacks of the 2D method are presented.

2.1 Phenomenological analysis of Parasitic Light Sensitivity

As discussed in Chapter 1, the signal degradation in Global Shutter CMOS Image Sensors is caused by the non-negligible capacity of the Storage Node (SN) to collect optical-generated free charges during frame readout. In an ideal case, as for example it would be when a mechanical shutter is used for shooting pictures, the Storage Node does not "sense" any light, meaning that no light is allowed to enter during the readout phase, thus no charges can be photo-generated and collected by the Storage Node. In case an electronic shutter is being used, no mechanical moving parts can shield the image sensor from light during its readout phase; light is continuously impinging onto the image sensor, thus continuously generating charges. The image sensor must therefore be able to "drain", away from the Storage Node, the highest number of photo-generated charges as possible, in order to make the electronic shutter as efficient as possible, thus increasing the Global Shutter Efficiency (GSE). An electronic shutter aims therefore to mimic the mechanical shutter impeding photo-generated charges to reach the Storage Node during readout phase.

We have previously seen that the image sensor Parasitic Light Sensitivity can be described as the ratio between the PhotoDiode and Storage Node sensitivities or, in other words, the ratio between the PhotoDiode and Storage Node Quantum Efficiency (QE). Remembering that sensitivity and Quantum Efficiency differ from just one multiplicative constant that is common to both PhotoDiode and Storage Node sensitivities, represented by the conversion gain as explained in Sec. 1.3.2, it is clear that the two nodes' Quantum Efficiencies play a fundamental role in the explanation of the parasitic light phenomena and interpretation. Following this last statement, analysis on Quantum Efficiency will be sufficient to guide us through the understanding of the Parasitic Light Sensitivity phenomena.

We know that the Quantum Efficiency defines the number of collected electrons on the considered node over the number of impinging photons onto the pixel. This parameter can be split in two parameter: η_o, being the Optical Quantum Efficiency, representing the number of charges photo-generated in the semiconductor active zone, i.e. the epitaxial layer onto which the pixel is fabricated, over the total number of incoming photons (when considering that one photon is able to generate one electron-hole pair); η_i, being the Internal Quantum Efficiency, representing the number of charges collected over the number of photo-generated charges.

There are two main mechanisms underlying the parasitic light issue:

- light directly impinging onto the Storage Node, thus generating a number of electron-hole pairs right inside the Storage Node which is function of the impinging light wavelength;
- charges that are photo-generated elsewhere but having the possibility and capability to reach the Storage Node.

A detailed analysis of these two mechanisms will follow shortly.

2.1.1 Direct collection of photons

Let us first give some modeling of incoming light, as it will be crucial for our discussion. For our scopes, we will just focus on monochromatic light, thus light having just one frequency. Light can be modeled as a wave, with its own frequency, or corresponding wavelength, and its own phase. In some cases, when the light wavelength is order of magnitudes smaller compared to the feature sizes with which it interacts, light can be modeled by straight-line streams, called "*rays*"; a ray is a line drawn in space corresponding to the direction of flow of radiant energy. Rays are therefore a visual artifact to understand and follow the energy flow. Nevertheless, this simple way of modeling is useful to describe the behavior of light when reaching surfaces: notably, a basic notion of *reflection* and *refraction* can be given thanks to ray theory.

Before getting into details of Reflection and Refraction laws, velocity at which light propagates inside a medium has to be modeled and understood. Notably, it is well known that photons, thus light, propagate in the free space at a constant speed, defined as the speed of light c and given by Eq. (2.1).

$$c = 299\,792\,458\ m \cdot s^{-1} \tag{2.1}$$

When light penetrates inside a medium, its apparent velocity, alternatively called *group velocity*, changes as function of the medium *refractive index*. Refractive index is a property of the material. We can therefore define the refractive index as follows:

$$n = \frac{c}{v_g} \tag{2.2}$$

where c is the speed of light in vacuum, as previously stated, and v_g is the group velocity.

When a beam of light strikes an interface between two media, meaning that light strikes an area where there is a discontinuity between the refractive index of the two media, some light is transmitted to the new medium and some is scattered backwards; let us just concentrate on the back-scattered light: this phenomenon is called *reflection*. Notably, it can be proven that if we consider the incidence angle θ_i as the angle between the incoming light ray direction and the normal to the interface, the reflected ray direction angle θ_r will follow the identity:

$$|\theta_r| = |\theta_i|, \qquad \theta_r = -\theta_i \tag{2.3}$$

As it can be understood from Eq. (2.3) and from Fig. 2.1, the reflection angle will have the same numerical value as the incidence angle, though the reflected ray will travel in opposite direction compared to the incidence one. When the incident ray is impinging perpendicularly to the interface (also called *normal incidence*), the reflected ray will travel in the backward direction.

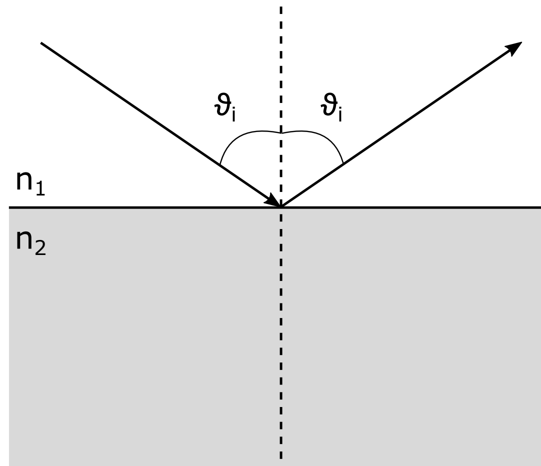


Figure 2.1: Illustration of light reflection at the interface between two media.

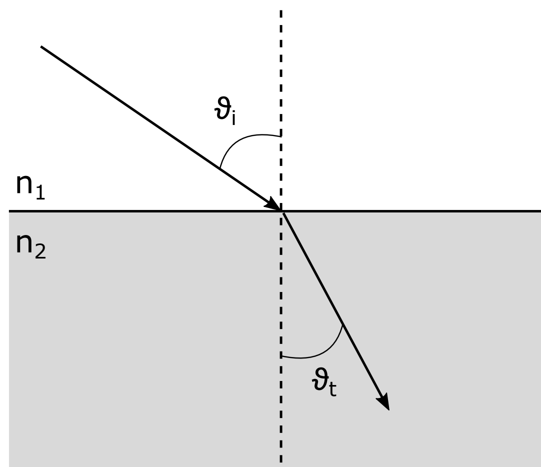


Figure 2.2: Illustration of light refraction at the interface between two media.

When encountering a discontinuity, some light is transmitted to the medium; this phenomenon is called *refraction*. It is possible to relate the incidence ray and the transmitted ray angles through the Snell's Law:

$$n_i \, sin\theta_i = n_t \, sin\theta_t \tag{2.4}$$

where n_i is the refractive index of the medium in which light is found before reaching the discontinuity, n_t is the refractive index of the medium in which light is transmitted and θ_i, θ_o are respectively the incidence and transmittance angles. Refraction phenomenon can be appreciated in Fig. 2.2; light enters in the second medium and is transmitted with an angle depending on the two media refractive index. The plane in which the incoming, reflected and transmitted ray lie is called *incidence plane*, which is always perpendicular to the plane on which the interface discontinuity lies.

Reflection and refraction are rather important when dealing with light; there is one phenomena which can be withdrawn from the previous equations and it is always important to take into account when light enters in medium with high refractive index: the *Total Internal Reflection*. Exploiting Snell's Law and supposing that a light ray lies inside a medium with high refractive index and heads towards an discontinuity interface with a medium having a lower refractive index, thus $n_i > n_t$, with an incidence angle θ_i, it is evident that $\theta_t > \theta_i$; there is one critical incidence angle at which the transmission angle becomes 90°:

$$\theta_c = \sin^{-1}\left(\frac{n_t}{n_i}\right). \tag{2.5}$$

When the incidence angle is equal or higher than the critical angle, the light that is transmitted to the low refractive index medium enters with an angle of 90° or more, being a mathematical artifact to say that light penetration in the low refractive index medium is not possible in this case; the incident light is therefore totally reflected and will not penetrate the medium.

It is clear by know that simple ray theory is able to describe reflection and refraction of light through direction angles, though some more physical theory is needed to describe the amount of light that is reflected or transmitted. An electromagnetic approach comes in handy, where light ray is modeled as an electromagnetic wave. We will not get into de details of the derivation of an electromagnetic wave, but we will focus on considering the electromagnetic lightwave as a *Plane Wave*. A plane wave is the simplest example of a three-dimensional wave; it exists at a given time and the electric and magnetic field vectors lie on a plane which is perpendicular to the direction of motion. An electromagnetic plane wave has the form

$$\vec{E} = \vec{E}_0\, e^{i\,(\vec{k}\cdot\vec{r}-\omega t)} \tag{2.6}$$

or, using the Euler's formula

$$\vec{E} = \vec{E}_0\, cos(\vec{k}\cdot\vec{r}-\omega t) \tag{2.7}$$

where the vector $\vec{E}$ represents the electric field of the monochromatic planar lightwave as function of time t, pulsation ω, the propagation vector $\vec{k}$, direction $\vec{r}$ and initial field $\vec{E}_0$. We have described the wave by it's electric field; it is possible to retrieve the magnetic field $\vec{H}$ using Maxwell's equations, that will be perpendicular to both electric field and propagation direction [Hec15].

With the knowledge of electric and magnetic field, it is possible to retrieve the energy density brought by the electromagnetic wave; the *Poynting vector* describes this energy flow as

$$\vec{S} = \vec{E} \times \vec{H}. \tag{2.8}$$

Since we are dealing with plane waves, it can be shown that energy density flows in the same direction of the wave propagation, being perpendicular to both electric and magnetic field.

It has to be reminded that, when light is modeled as an electromagnetic wave, polarization has to be taken into account. Polarization states the direction of the electric field vector with respect to the incidence plane; dealing with plane waves has the advantage in treating the

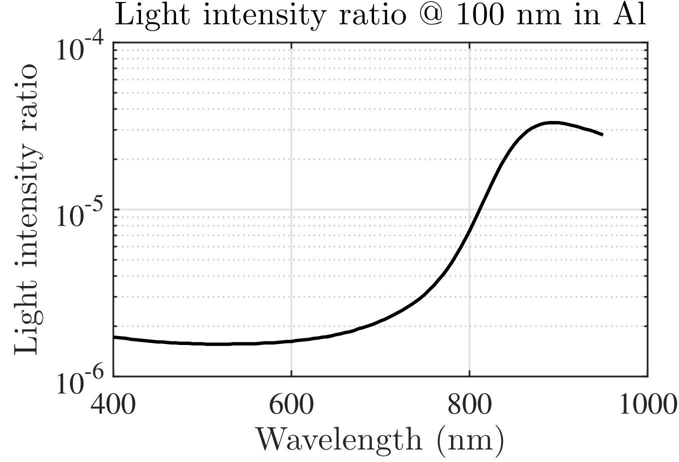


Figure 2.3: Light intensity in Aluminum after 100 nm.

wave polarization as constant, since the electric field direction is not changing with time while the wave propagates. If the electric field vector lies on the incidence plane, we define the electromagnetic wave as *parallel polarized*; if the electric field vector lies on a perpendicular plane compared to the incidence plane, we define the electromagnetic wave as *perpendicularly polarized*.

This description of lights allows to calculate the amplitude coefficient for reflection and transmission of an incident electromagnetic wave at the interface of two different media; the coefficients are described by the Fresnel equations given in Eqs. (2.9)-(2.12), where $r_\perp$ and $r_\parallel$ define the reflection coefficients of an impinging plane wave having respectively perpendicular and parallel polarization with respect to the incidence plane, and $t_\perp$ and $t_\parallel$ define the transmission coefficient of an impinging plane wave having respectively perpendicular and parallel polarization with respect to the incidence plane [Hec15].

$$r_\perp = -\frac{\sin(\theta_i - \theta_t)}{\sin(\theta_i + \theta_t)} \tag{2.9}$$

$$r_\parallel = +\frac{\tan(\theta_i - \theta_t)}{\tan(\theta_i + \theta_t)} \tag{2.10}$$

$$t_\perp = +\frac{2\sin\theta_t\, \cos\theta_i}{\sin(\theta_i + \theta_t)} \tag{2.11}$$

$$t_\parallel = +\frac{2\sin\theta_t\, \cos\theta_i}{\sin(\theta_i + \theta_t)\cos(\theta_i + \theta_t)} \tag{2.12}$$

The Fresnel equations complete the picture of light reflection and refraction; we are now able to describe light motion inside media and its behavior at interfaces.

We will now make use of the knowledge of light propagation in media for our analysis on the light impinging onto the Storage Node. It may seem trivial that, in order to diminish as

much as possible the number of charges photo-generated inside the Storage Node region, a light shield right above the Storage Node is required. In a first hypothesis, we will focus on using some Back End Of Line (BEOL) layer to shield the Storage Node from light, notably the metal layers used for creating interconnections; we will suppose that the metal layer has been carefully designed to cover the entire Storage Node zone, that said, there is no possibility that light penetrating with normal incidence would reach the Storage Node before reaching the metal layer. We have to first suppose that the metal is not transparent to the wavelengths in play, otherwise it will be right away clear that the metal layer is not the right shield to use. Let us consider a 100 nm thick slab of aluminum and suppose that light penetrates the material from the top surface to the bottom surface. Aluminum has been widely used in CMOS processes, like the 0.18 µm and the 0.15 µm technology node, while a usage of copper can be appreciated in modern CMOS processes [Tor95]; [IBM]. Using the Beer-Lambert law, we want to compute the amount of light that is able to reach the bottom surface at each wavelength from 400 nm (ultra-violet) to 950 nm (near infra-red). The material's absorption coefficient has been retrieved from the refractive index repository [Ref]. It is easily understood from Fig. 2.3 that at the desired wavelengths light does not penetrate Aluminum deeply and that the percentage of light attaining the 100 nm depth is negligible. Usually, in modern CMOS Image Sensor technology, interconnection layers are of the order of few hundreds of nanometers. Moreover, it has to be taken into account that interconnection metal layers have high refractive index compared to the oxide in which they are submerged; a high light reflection due to metal has to be taken into account, which strongly diminishes the amount of light allowed to overcome the metal shield.

We have discovered that Aluminum, or in general metallic interconnection layers, can be considered optimal shields for normal impinging light. Light is though not always impinging at normal angle; light can penetrate at a steeper angle inside the pixel and though reflection has to be taken into account when shielding of Storage Node is required. Notably, it can be appreciated from Fig. 2.4 that light can penetrate inside the BEOL stack and reach the silicon surface, reflecting and pointing towards the metal shield and reflecting again towards the Storage Node. We now want to try to model the amount of light able to reach the silicon surface after multiple reflections; we will suppose that the metal shield is submersed in Silicon Dioxide (SiO_2). Exploiting the Fresnel equations (Eqs. (2.9)-(2.12)) to make an analytical calculation and averaging the result of the two polarizations, we obtain the result in Fig. 2.5; it can be seen that the amount of light reaching the Si surface after two reflections is non-negligible and may be able to photo-generate charges inside the Storage Node region. Moreover, it can be seen how the intensity ratio after multiples reflections is wavelength dependent, given by the fact that the reflection and transmission coefficients of Si and Al are function of wavelength themselves (the SiO_2 refractive index can be considered constant in the wavelength range 400 - 950 nm).

There is one more point that has to taken into account when Storage Node shielding from impinging light is required: *light diffraction*. Diffraction is a property of waves that appears when the wave is obliged to pass through a hole which has similar dimensions compared to its wavelength. Concerning image sensors, it is not difficult to realize that the feature sizes through which impinging light has to pass are of the same order of magnitude of the

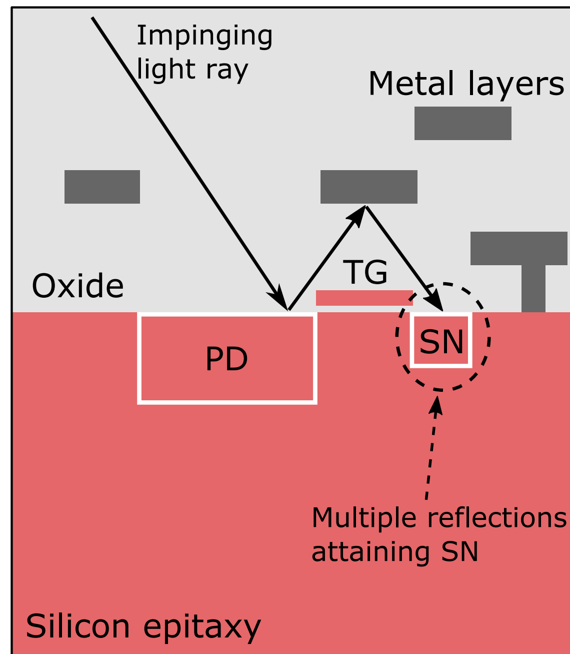


Figure 2.4: Illustration of multiple reflections taking place inside a pixel structure. A fraction of the light impinging onto the Si/SiO_2 interface is reflected and supposed to impinge onto the metallic interconnection. A part of this latter is then reflected and impinges onto the Si/SiO_2 interface, maybe close to the Storage Node region, depending on the impinging angle.

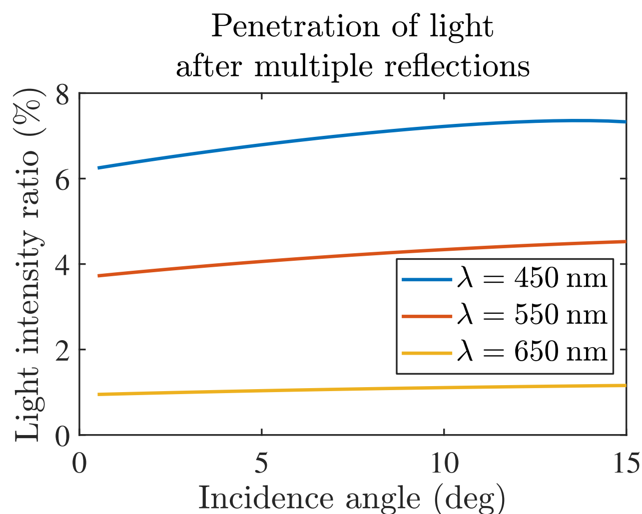


Figure 2.5: Amount of light penetrating silicon after two reflections and one transmission (Si/SiO_2 interface reflection, SiO_2/Al interface reflection, Si/SiO_2 interface transmission), following the scheme given in Fig. 2.4.

light wavelength. Nowadays, the CMOS Image Sensor industry is racing for pixel shrinking; smaller pixels are continuously designed and desired, as well as the features integrated are

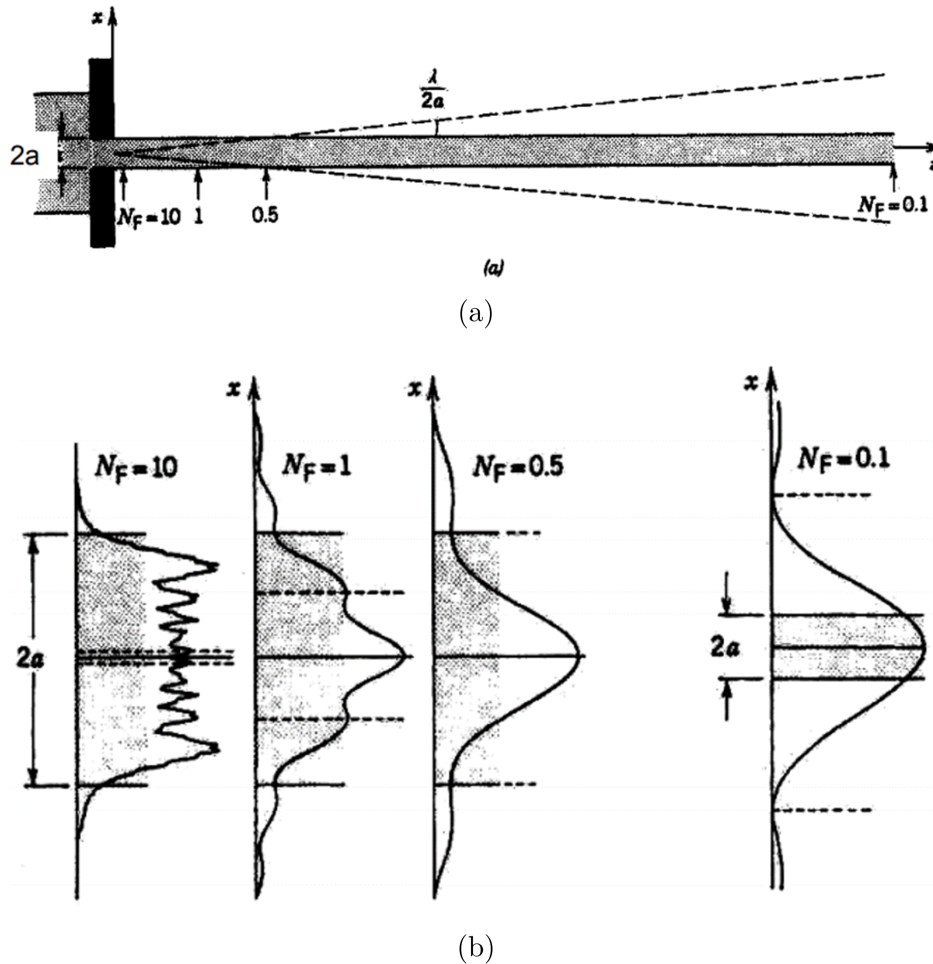


Figure 2.6: (a) Schematic of a diffraction slit (in solid black). The gray area on the right of the slit represents the region where we expect to see light. In dashed, the expansion cone of light diffracting. (b) Examples of Fresnel and Fraunhofer diffraction pattern as function of the Fresnel number N_F. The gray area and dashed lines in (b) are equivalent to the ones presented in (a) at the given Fresnel number. The two figures have been retrieved from [Xia].

getting smaller and smaller. It is evident that a correct analysis of light propagation inside a pixel would not be complete without taking into account diffraction.

Light diffraction theory is complex and is not aim of this work to detail it extensively. It will be sufficient to know that light follows the Huygens-Fresnel principle, thus the amplitude of the optical field, or of the electromagnetic wave, builds-up by superposition of secondary spherical wavelets generated by every unobstructed points of the wavefront. In other words, whenever light passes trough an opaque surface, the wavefront is “trimmed” and the new amplitude follows a spherical shape at the borders of the trimmed wavefront, as shown by Fig. 2.7. To make it even simpler, diffraction is the property of light to propagate beyond a corner when passing through a hole. If we place ourselves at a distance z_0 from the pin-hole, we will be able to observe a particular pattern, caused by light self-interference when passing

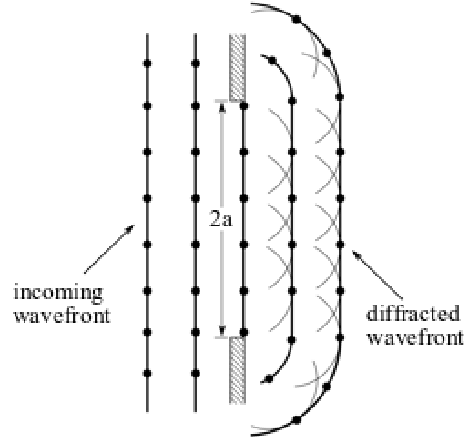


Figure 2.7: Schematics of the wavelet approximation for a single slit diffraction. The sum of all wavelets wavefront builds the diffracted wavefront.

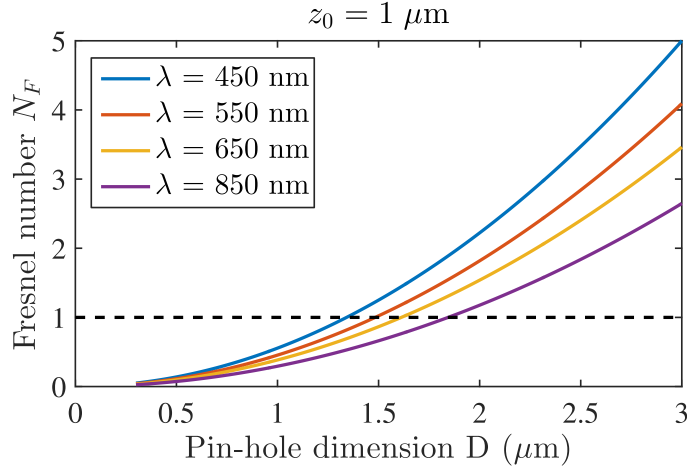
through a pin-hole and diffracting. The pattern shape is dependent on wavelength, pin-hole dimension D (noted as $2a$ in Fig. 2.6) and also on the observing distance. Two cases are worth of notice:

- if the observing distance respects the following criteria, $z_0 \gg \frac{D^2}{\lambda}$, Fraunhofer approximation can be made and pattern can be analytically described;
- if the observing distance is smaller compared to the one in Fraunhofer approximation and if the following criteria applies, $z_0^3 \gg \frac{\pi}{4\lambda}D^4$, Fresnel approximation can be applied.

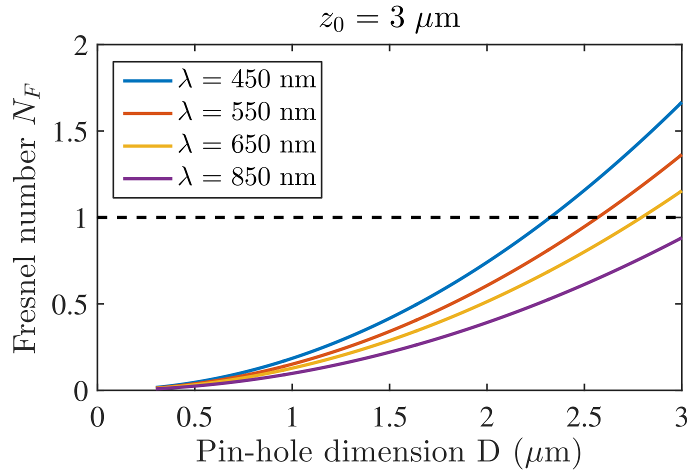
Fraunhofer and Fresnel approximation are applied on the consideration of propagating field phase after the passage through the pin-hole. Fraunhofer approximation considers the propagating field as a plane wave, thus the phase is varies linearly with the distance. On the other hand, Fresnel approximation considers the propagating field as a spherical wave [Goo05]. One parameter comes in handy to distinguish between the different diffraction situations: the Fresnel number N_F [Hec15]. The Fresnel number is defined as follows:

$$N_F = \frac{D^2}{4\,\lambda\,z_0}. \tag{2.13}$$

Notably, for $N_F \ll 1$, Fraunhofer approximation can be made; for $N_F \sim 1$ Fresnel approximation can be made; for $N_F \gg 1$ no approximation can be made. The latter is generally the case in which the observing plane is extremely close to the diffraction pin-hole. An example of Fresnel and Fraunhofer patterns as function of the Fresnel number can be appreciated in Fig. 2.6. It is evident how the further we go from the diffracting point, the more the light spreads beyond the corner.



(a)



(b)

Figure 2.8: Evolution of the Fresnel number as function of the pin-hole dimension and its distance to the silicon surface, where (a) $z_0 = 1\,\mu$m and (b) $z_0 = 3\,\mu$m.

Going back to image sensors, it must be clear that, when light strikes a rectangular aperture created by two metallic layers (we will refer to this as the *shield aperture*), it will diffract. If we want to understand the regime in which we are, we can use the Fresnel number to obtain an idea of the diffraction pattern that light is going to reproduce at the Si/SiO_2interface. Fig. 2.8 shows the Fresnel number as function of wavelength λ, the shield aperture dimensions and the distance from the shield aperture and the Si/SiO_2 surface; notably (a) shows the Fresnel number for a distance $z_0 = 1\,\mu$m and (b) shows the Fresnel number for a distance $z_0 = 3\,\mu$m. For both cases, light at the considered wavelengths suffer from diffraction, especially when the shield aperture dimension is small. One last thing to notice, the further the shield aperture is from the Si/SiO_2 surface, the more light will spread beyond the aperture, following Fraunhofer diffraction.

It should be evident by now that Storage Node shielding from impinging light is therefore not trivial, careful operations have to be performed to mitigate the diffraction problem.

2.1.2 Collection of diffusing charges

We will try to give an understanding of the problem of charges, photo-generated away from the PhotoDiode, that can reach the Storage Node and become part of the parasitic light-generated charges. Carriers generated deeper down into the epitaxial layer are generally found in quasi-neutral regions, where almost no electric field is present, with the exception of the one generated at the graded interface between the epitaxial layer and the substrate, that is though not controlled by any polarization. To understand minority carriers diffusion in doped silicon, we require the use of drift-diffusion equations; current in a semiconductor can be described as follows [Sze08]:

$$J_n = q\mu_n\mathscr{E} + qD_n\frac{\delta n}{\delta x} \tag{2.14}$$

$$J_p = q\mu_p\mathscr{E} + qD_p\frac{\delta p}{\delta x} \tag{2.15}$$

where J_n and J_p are respectively the current density for electrons and holes, q is the electron charge, μ_n and μ_p are respectively the mobility of electrons and holes, D_n and D_p the electron and hole diffusion coefficient and n and p are respectively the electron and hole density.

When considering a p-doped epitaxial layer, minority carriers are electrons. Let us suppose that no electric field is present in the epitaxial layer; if an electronic concentration is created somewhere in the epitaxial layer, looking at drift-diffusion equations it is evident that the concentration gradient $\frac{\delta n}{\delta x}$ will act on carriers thus producing an electron current flow. If electrons do not reach a region where an electric field is present, they will keep diffusing.

Carriers diffusing and not being collected by the PhotoDiode are the reason for a poor Internal Quantum Efficiency (η_i) of the pixel; a part of those diffusing carriers can therefore reach the Storage Node, resulting in an increase of the Storage Node light sensitivity and leading to a higher impact of the Parasitic Light Sensitivity on the image sensor. In order to improve the Internal Quantum Efficiency, various techniques have been used in literature as for example graded substrate doping [Dul+09] that creates an electric field allowing charges to be driven towards the upper side of the epitaxial layer and deep implants allowing for design of both PMOS and NMOS [Coa+10] thus physically separating collection from storage, substrate polarization allowing for fully depletion of the epitaxial layer [SCH16]. These enhancements can led to an improved PhotoDiode Quantum Efficiency, especially at the NIR range where charges are generated deeper; a reduction of the image sensor Parasitic Light Sensitivity can be expected. Usage of high resistive substrates can also help in improving Quantum Efficiency through increasing the PhotoDiode Space Charge Region area [Lin+15], though parasitic collection may still happen.

In some cases, the technological process with which the image sensor is built does not allow

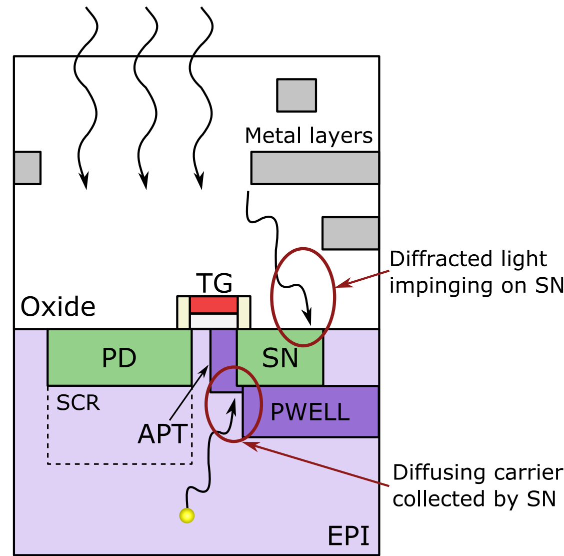


Figure 2.9: Schematic cross-section of a pixel where are shown PhotoDiode, Storage Node, PWELL and Anti Punch-Through doping layers as well as metal layers exploited as interconnections and for shielding purposes. The phenomena leading to a non-negligible Parasitic Light Sensitivity are visually shown, being the light diffracted by the metallic shield and impinging onto the Storage Node region, and the electron diffusing from the epitaxial layer.

for the options previously presented. It is therefore crucial to understand how to reduce the amount diffusing carriers reaching the Storage Node, thus placing some "diffusion shielding layers" in the correct locations.

As a summary, we can take a look at Fig. 2.9, where the phenomena which are responsible for the degradation of the signal stored in the Storage Node are highlighted: direct light impinging on the Storage Node caused by multiple reflections or diffraction; carriers photo-generated in the neutral region of the epitaxial layer that diffuse towards the Storage Node.

2.2 Photo-generation of charges

Let us first start with the modeling of charges photo-generation inside the Si epitaxial layer, knowing the wavelength, the incidence angle and its intensity. In order to choose the best tool for modeling the impinging light and photo-generation of charges, a few elements have to be taken into account:

- light diffraction have to be accurately modeled by the tool;
- impinging light power density inside the silicon region, as function of the incoming wave intensity, has to be given as result of the tool. We want to be able to compute the photo-generated charge density inside the silicon, this requires the calculation of the

impinging photon density by means of the light power density;

- the tool has to be suitable for the dimensions of the structure that is wanted to be modeled. Notably, aim of the simulation tool will be to model impinging light onto a pixel, thus a few tens of micron square (for 2D simulations);

- periodic boundaries are required especially if modeling of an array of pixels is required.

Some of the most used tools for modeling light include Ray-Tracing [Gla89] and Transfer-Matrix-Method (TMM) [Hal64]. Both methods use an approximation of the electromagnetic wave model to describe light interaction with media and its propagation. Ray-Tracing is mostly suited for simulations in which the objects dimensions have a greater order of magnitude in comparison to the impinging wavelength, this allows to perform very fast simulations through approximation of the behavior of light, but diffraction is not reproduced and the object dimensions are far bigger than what we would like to model (Ray-Tracing is generally used for modeling light propagation inside a series of optical lenses). The TMM makes use of the successive matrix products to model the propagation of light in media. The advantage of this method compared to Ray-Tracing is that it becomes more handy when dealing with smaller dimensions, as for example pixel dimensions, and it can successfully model light interference due to phase shifts. As a disadvantage, TMM is not able to model diffraction given that its geometrical modeling of light [Goo05]. Therefore, an alternative method has to be found.

2.2.1 Introduction to FDTD simulations

The Finite-Difference Time-Domain (FDTD) method is arguably the simplest, both conceptually and in terms of implementation, of the full-wave techniques used to solve problems in electromagnetics. It can accurately tackle a wide range of optical problems, as for example diffraction, since it deals directly with Maxwell's equations.

The FDTD method employs finite differences as approximations to both the spatial and temporal derivatives that appear in Maxwell's equations; notably, the finite difference method make use of the Taylor series expansions at the first order of a function at a point. A function f at a point x_0 can be approximated through Taylor series expansion as follows:

$$\frac{df(x)}{dx}|_{x=x0} \approx \frac{f\left(x_0+\frac{\delta}{2}\right)-f\left(x_0-\frac{\delta}{2}\right)}{\delta} \tag{2.16}$$

where the offset from the central point x_0 is represented by $\pm\frac{\delta}{2}$. The Taylor expansion technique is therefore used to approximate the Maxwell's equation per each point in space,

given that Maxwell's equations can be described in a differential form, as the following:

$$\nabla \cdot \vec{E} = \frac{\rho}{\epsilon_0} \tag{2.17}$$

$$\nabla \cdot \vec{B} = 0 \tag{2.18}$$

$$\nabla \times \vec{E} = -\frac{\delta \vec{B}}{\delta t} \tag{2.19}$$

$$\nabla \times \vec{B} = \mu_0 \left(\vec{J} + \epsilon_0 \frac{\delta \vec{E}}{\delta t} \right) \tag{2.20}$$

where $\vec{E}$ and $\vec{B}$ are respectively the electric and magnetic field vectors, ρ represents the charge density and $\vec{J}$ is the current density vector [Sch10].

The algorithm to solve Maxwell's equations through use of the finite difference method was first proposed by Kane Yee in 1966 [Yee66].

It is built as a time-dependent method, simulating the impulse response of the system to light. Impulse response as function of frequency, or wavelength, is then calculated through a Fourier transformation. Energy conservation from the time domain to the frequency domain is ensured by the Parseval's theorem, ensuring no information is lost in the transformation process [IH98].

Once understood how the method works, it is important to model the materials with which light will get into contact. For our purposes, we can define three types of materials: dielectrics, (n,k) materials and conductive materials, like metals.

- **Dielectrics**. The dielectric materials are the simplest ones to model. Those materials are considered non-dispersive, meaning that they have a constant refractive index n at all frequencies; this is particularly true for dielectric materials in case we are dealing with a restrained set of frequencies, in which the refractive index can be considered constant. Moreover, the dielectrics show no light absorption; the imaginary part of refractive index k can be considered null.

- **(n,k) materials**. Modeling of non-conductive materials behavior (as for example Silicon or dispersive dielectrics) can be done through knowledge of the complex refractive index $n + \mathrm{i}\, k$; a table containing values of n and k per each frequency can be imported. Nevertheless, the software requires an analytical model of the complex refractive index to operate since the simulation is performed in time-domain; model fitting to the complex refractive index of the material is crucial for the validity of simulation at a large spectrum of frequencies.

- **Conductive materials**. Metallic interconnections are often present in CMOS Image Sensor structures, it is therefore crucial to accurate model their light response. For a non-magnetic material, i.e. the relative permeability μ_r is equal to 1, the refractive index and the relative permittivity ϵ_r are linked as follows: $n = \sqrt{\epsilon_r}$. In conductive materials, the relative permittivity is modeled by the conductivity of the material as

given by $\epsilon = \epsilon_0 \epsilon_r + i\frac{\sigma}{2\pi f}$, with σ being the conductivity, f the frequency [BBB13]. Derivation of the material conduction can be done by use of various models, like the Drude, Debye or Lorentz models.

However, due to usage of direct solution of Maxwell's equations, FDTD is a fundamentally coherent simulation method. This means that the propagating field phase is coherent in the temporal window the simulation is performed. It results in the appearance of fringes, or large fluctuations, of the reflection and transmission coefficients as function of wavelength when a plane wave is impinging on materials, due to coherent phase interference, better reproducing the behavior of a coherent laser source rather than the behavior of an incoherent light source. When dealing with incoherent light sources, which is generally the case for scenes that are imaged by an image sensor, temporal incoherence is vital for a correct simulation of light propagation inside the structure. The issue can be solved through *partial spectral averaging* (PSA) of simulation results over a small frequency range δf (via Lorentzian weighting) surrounding the principal simulation frequency. In our simulations, δf has been chosen to obtain a wavelength range of ± 10 nm, which has been chosen with the aim in reproducing the behavior of color filters that are exploited in our image sensors test benches.

With the knowledge of material refractive index fitting and PSA, it has been proved that, for a wide range of wavelengths (e.g. from 400 nm to 950 nm, as in requirements for our study), a proper modeling of light propagation inside a silicon slab (that can be extended to a more complex structure for image sensing) is performed through single wavelength simulations with PSA [Kel10]. The simulations that will be presented hereon have been developed following these criteria and exploiting the software Lumerical Inc. to perform the FDTD simulations [Lum].

2.2.2 Light propagation simulation in pixel structures

In a primary approach, we will model the lightwave propagation in a 2D pixel structure. Fig. 2.10 gives an example of the pixel geometry that has been used: the 5 µm thick silicon epitaxial layer; the poly-silicon gates along with their SiO_2 gate oxide and nitride spacers; the Pre-Metal-Dielectric (PMD), being a specific glass deposited before the first metal layer deposition; the Inter-Layer Dieletric (ILD), being a specific glass deposited between the metal layers; and the metallic elements, like VIAs, made of Tungsten (W) and metal layers, made of Al.

With the aim in comparing the simulation results with a real image sensor, the structure has been created following dimensions given by a known technology; however, some approximations had to be made, due to lack of detailed knowledge in the device process:

- Presence of an anti-reflection coating layer between the silicon surface and the oxide is unknown; no anti-reflection layer has then been integrated in the simulated pixel structure.

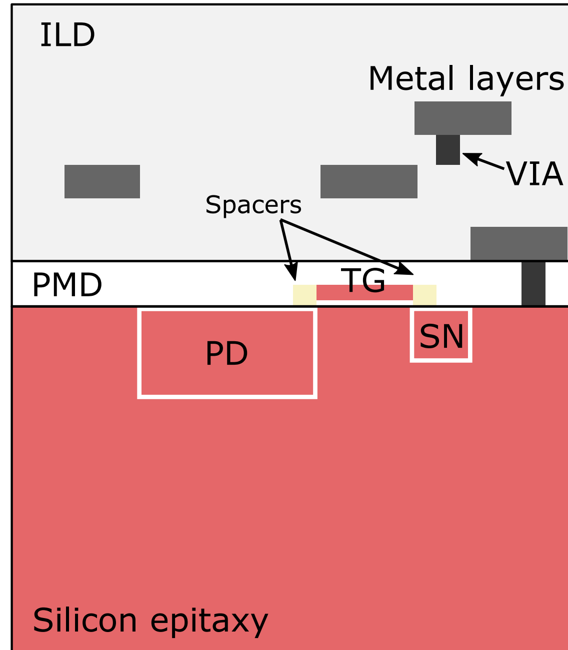


Figure 2.10: Schematic of a pixel structure that can be modeled in FDTD simulations, following the known specifications of a selected technology, as for the Inter-Layer Dieletric (ILD), Pre-Metal Dielectric (PMD), metal layers and TG thicknesses. The presence of PhotoDiode and Storage Node is just symbolic for a visual understanding of their placement.

- Similarly, presence of an anti-reflection coating layer between the Inter-Layer Dieletric surface and air is unknown; also in this case the anti-reflection layer has not been integrated.

- Contact-forming through salicide process is unknown. The salicide process consist in a reaction between a transition metal layer and silicon, but not with SiO_2 that produces a thin low-resistance layer called *silicide*. It is known that in classical CMOS technology, salicide process is used to improve stability and resistance of contacts between silicon and the metallic interconnections; in CMOS technology for image sensor though, this step is performed in some specific areas, given the fact that the silicide is partially transparent, thus reducing the number of photons transmitted in the silicon layer. In our case, it is unknown whether the salicide process takes places and the transition metal that is used; no silicide is therefore modeled in our optical structure.

- Refractive index model as function of wavelength of the Pre-Metal Dielectric and the Inter-Layer Dieletric is unknown, only one constant value of the real part of the refractive index is given. Our structure will therefore be modeled through a constant refraction index value for both Pre-Metal Dielectric and Inter-Layer Dieletric.

On the other hand, layer thicknesses are known, as for example the oxides, gates and interconnection thicknesses, and have been taken into account in our optical structure.

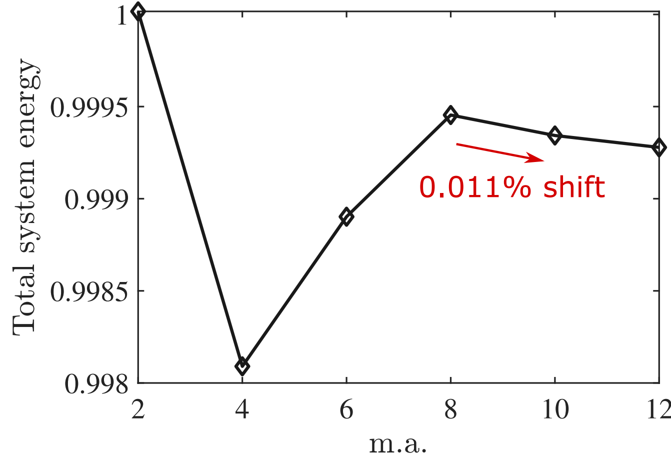


Figure 2.11: Convergence test result for different mesh accuracy (m.a.). The convergence parameter has been determined as the total energy absorbed and reflected by the structure with respect to the initial energy of the simulation.

As previously said, it is required to be able to simulate one pixel integrated in a pixel array: Periodic Boundary Conditions (PBC) are therefore mandatory on the x direction to reproduce this behavior. It is worth of notice that PBC can only be used in presence of a Plane Wave light source. A Plane Wave light source can be readily implemented in FDTD simulations, though it is not representative of real light conditions, as for example a Gaussian source. Simulation of an array of pixel in real conditions would therefore require building a larger structure with more pixels in parallel, using a Gaussian source; it has though been proven that the sum of a number of Plane Wave impinging at different angles can successfully approximate the behavior of a Gaussian source, thus simulating the smallest possible structure (one pixel) with PBC [Vai+07]. The usage of PBC though requires careful attention at the boundaries, due to phase shift when the Plane Wave is impinging with a non-zero angle; the simulation software allows the use of Bloch boundary conditions, through which the phase is accurately taken into account. However, Plane Wave property of impinging with one defined angle allows us to study and analyze the pixel response at different incidence angles separately.

Finally, z-direction boundary conditions have to be given. We suppose that the light reflected at the oxide/air surface is no more able to come back and attempt to reach the pixel structure again, we will consider it as “lost”. Similarly, when light reaches the bottom of the epitaxial layer, it will generate electrons in the deep substrate. The substrate is though highly doped and the net recombination rate of free electrons is high; we therefore suppose that all electrons generated in the substrate rapidly recombine (diffusion length of less than 10 µm) and are not able to reach the epitaxial layer. To take into account these conditions, the software allows to use Perfectly Matching Layer (PML) absorbing boundary conditions; through impedance match of the simulation region and material, PML are able to absorb lightwaves with minimal reflections.

Finally, structure meshing is an important matter for FDTD simulations. FDTD simula-

tions, being of the finite-difference type, operate on a rectangular grid; accurate fine meshing of round objects is therefore mandatory to properly take into account the shape. It is common rule that FDTD simulations optimal operation between speed and accuracy is given for a maximum mesh size dimension Δx respecting the following equation:

$$\Delta x = \frac{\lambda}{\text{m.a.} \cdot \Re\{n\}}, \tag{2.21}$$

with $\Re\{n\}$ being the real part of the complex refractive index and where m.a. is defined as the *mesh accuracy*. In order to improve simulation efficiency, adaptive x and z meshing has been performed, as function of the area refractive index. Mesh accuracy has been proven by convergence tests shown in Fig. 2.11. The convergence parameter has been determined as the sum of power that has been absorbed and reflected by the structure. If the following equation stands, where P_{source} is the source power, P_r is the power reflected by the structure and P_{abs} is the total absorbed power, the mesh can be defined as accurate.

$$P_{source} = P_{abs} + P_r \tag{2.22}$$

It is shown that, starting from m.a. = 8, the simulation gradually reaches convergence. A value of m.a. = 8 has been chosen as a trade-off between accuracy and simulation time.

2.2.3 Extraction of results: the Optical Generation Rate Density map

Optical simulations are needed for extracting the charges photo-generation density rate G_{abs} inside the silicon volume. In general, semiconductors behave as absorbers and emitters of radiation, though the latter is negligible in Si due to the material's indirect bandgap and trap-dominated recombination [SN06]. Therefore, in absence of optical emission, the photo-generation rate can be determined from the divergence of Poynting vector. Under steady-state harmonic conditions, absorbed power, and thus photo-generation, can be expressed in terms of the electric field magnitude $|\vec{E}|$ and the imaginary part of the material's permittivity $\epsilon = \epsilon_0\, \epsilon_r$, as given by Eq. (2.23) [SN06]; [PFC97], where we remind that E_{ph} is the photon energy as function of wavelength, $\vec{S}$ is the Poynting vector and $\Re\{\cdot\}$, $\Im\{\cdot\}$ represent respectively the real and the imaginary part. We further suppose that photon-charges generation efficiency (defined as η in [SN06]) is equivalent to 1, meaning that one impinging photon generated one electron-hole pair.

$$G_{abs} = \frac{1}{E_{ph}}\, P_{abs} = \frac{1}{2\, E_{ph}} \Re\{\nabla \cdot \vec{S}\} = \frac{\pi f}{E_{ph}}\, |\vec{E}|^2\, \Im\{\epsilon\} \tag{2.23}$$

Thanks to the fact that the FDTD method is computed at each grid point, recording of the steady-state electromagnetic field phasor $\vec{E}$ as well as the complex refractive index of silicon is possible, allowing for calculation of $G_{abs}(x, z)$ per each grid point. Moreover, the steady-state response of the system allows for a time-independent result of the photo-generation; $G_{abs}(x, y)$ results to be the charges photo-generation per units of time and space, also defined as *Optical Generation Rate Density*. An example of G_{abs} in space can be appreciated in

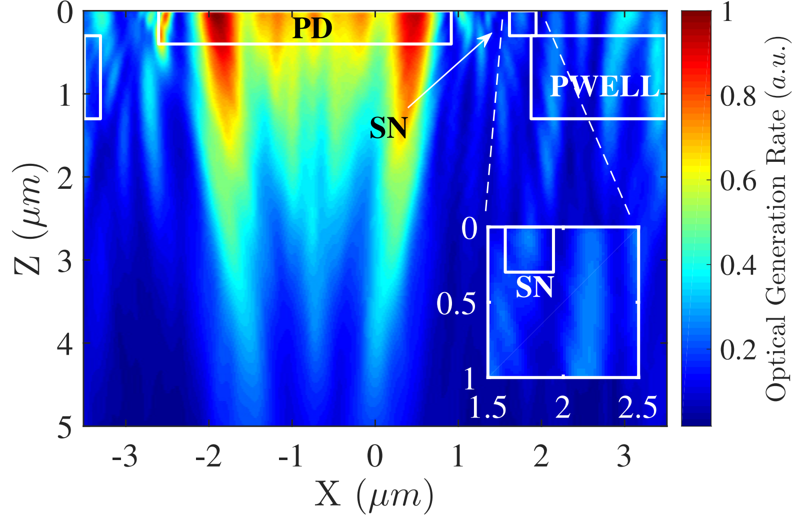


Figure 2.12: Optical Generation Rate Density (G_{abs}) of the pixel structure given in Fig. 2.10, result of an FDTD simulation. The PhotoDiode, Storage Node and PWELL locations are highlighted in white with the solely purpose of giving an understanding of the pixel structure. A zoom-in is presented to highlight the non-negligible optical generation in the Storage Node region despite the presence of a metallic layer to optically shield the node.

Fig. 2.12, on a 5 µm thick silicon epitaxial layer. We have suppressed the view of the pixel back-end structure as well as gate structures since absorbed radiation in those region does not matter for our purposes. The zoom-in shows how there is non-negligible optical generation inside the Storage Node area, despite the fact that the Storage Node is shielded with a metal layer, as it has been shown in Fig. 2.10.

Impinging photon number N_{ph} can be retrieved knowing the source power P_{source} with which simulation has been performed and the photon energy E_{ph}, as given by Eq. (2.24). Source power can be similarly derived from the source Poynting vector $\vec{S}_{source}$.

$$N_{ph} = \frac{P}{E_{ph}} = \frac{\int \Re\{\vec{S_{source}}\} \cdot dx}{2\, E_{ph}} \tag{2.24}$$

Integrating G_{abs} in space, it is possible to retrieve the number of absorbed photons N_{abs} (or photo-generated charges) as function of the impinging photon number N_{ph}; the ratio of the two will result in the Optical Quantum Efficiency η_o.

G_{abs}, representing the charges generation rate per units of time and space, can therefore be used as input parameter to perform charges transport simulations.

2.3 Modeling under independence hypothesis of charge photo-generation and transport

As shown in Sec. 2.1.2, modeling of charges transport requires knowledge on the charges density inside the silicon layer; in a steady-state form, i.e. when considering a time-invariant photo-generation of charges, this would require the resolution of the steady-state continuity equation, as given for both electrons and holes by Eqs. (2.25) and (2.26) [SN06],

$$\vec{\nabla} \cdot \frac{1}{q}\,\vec{J_n} - U_n = \frac{\partial n}{\partial t} = 0 \tag{2.25}$$

$$\vec{\nabla} \cdot \frac{1}{q}\,\vec{J_p} - Up = \frac{\partial p}{\partial t} = 0 \tag{2.26}$$

where U_n, U_p account respectively for the net transition rate, given as the recombination rate minus the thermal generation rate $U_n = R_n - G_{th}$ and $U_p = R_p - G_{th}$; $\vec{J_n}$ and $\vec{J_p}$ account respectively for electron and hole current density as given by Eqs. (2.14) and (2.15). We have previously seen that electron and hole generation is function of the impinging lightwave and, with the consideration that one impinging photon produces one electron and one hole, thus an electron-hole pair, this can be written in terms of the Beer-Lambert law as follows:

$$G_n = G_p = \alpha(\lambda)\, I_0\, e^{-\alpha(\lambda)\, z} \tag{2.27}$$

where I_0 is the lightwave intensity at the silicon surface, E_{ph} the photon energy and $\alpha(\lambda)$ the silicon absorbing coefficient. It becomes evident through combination of Eqs. (2.25) and (2.26) with Eq. (2.27) that an accurate model of the charge transport phenomena has to be performed once the steady-state photo-generation rate is known. In other words, charges transport simulation would require prior knowledge of the optical generation rate; optical simulations would therefore be an input for charge transport modeling. This conditions poses some difficulties when multiple illumination conditions have to be simulated, coupling them with transport simulations: following the previous assumption, this would mean that a transport simulation has to be performed per each different illumination condition. In other words, if the pixel has to be modeled under N different illumination conditions (for example, different incidence angles, different illumination intensities, different wavelengths, ...), this would require a total of $2N$ simulations.

Given that the aim of our approach is to simplify this process through modeling the charge transport problem independently of the optical charge generation, allowing to perform $N+1$ simulations given N different illumination conditions, it would be no more possible to exploit the drift-diffusion and the continuity equations to model the charge transport phenomenon, since this method requires the actual charge density as input to be correctly modeled. We will therefore try to develop another method that allows us to understand the *probability that a photo-generated charge has to reach a certain region*, given conditions as for example the electric field distribution in the epitaxial layer.

First of all, let us set the boundaries for the validity of this assumption, giving first a brief

reminder of charges lifetime since it would be a critical point for our assumption.

2.3.1 Carriers lifetime in silicon

Giving a closer look to continuity equation, there is a recombination term for both electrons and holes, R_n, R_p, that refers to the process with which the semiconductor tries to get back to its equilibrium condition once it has brought away from it. In other words, when carriers are generated in a region of the semiconductor, thus putting it out of equilibrium, the recombination process helps the semiconductor to re-establish its equilibrium state by bringing the generated carriers to their initial state. This process is though not instantaneous, so carriers recombination happens after a given amount of time, defined as *carriers lifetime.*

Radiative recombination is dominant in direct-bandgap materials. Silicon is though an indirect-bandgap semiconductor; non-radiative is more likely to take place. To model the non-radiative recombination phenomena, the Shockley-Read-Hall (SRH) statistics is exploited. Non-radiative recombination is modeled as trap-assisted recombination: electron falls into a “trap”, an energy level within the bandgap caused by the presence of a foreign atom or a structural defect; the electron occupying the trap energy can in a second step fall into an empty state in the valence band, thereby completing the recombination process. Considering only one trap level at the center of the bandgap, the net transition rate for both electrons U_n and holes U_p will read [SN06]:

$$U_n = U_p = \frac{np - n_i^2}{\tau_n (n + n_i) + \tau_p (p + n_i)}, \tag{2.28}$$

where, n is the concentration of electrons out of equilibrium $n = n_0 + \delta n$, p is the concentration of holes out of equilibrium $p = p_0 + \delta p$, n_i is the intrinsic electron concentration and τ_n, τ_p are respectively the electron and hole lifetimes for non-radiative process. In a more compact form, in case of low-injection conditions in a p-type semiconductor, the net transition rate reads [SN06]:

$$U_n = U_p = \frac{\delta n}{\tau_n}. \tag{2.29}$$

Carriers lifetime plays an important role in silicon and in the feasibility of using silicon as a detector of photons; if photo-generated electrons were to recombine straight after their generation, it becomes evident that the capability of creating a photo-current with the photo-generated carriers would be very little.

2.3.2 Validity conditions of the hypothesis

We can now focus on the validity of modeling carriers transport independently from the optical generation rate. Let us give the 1D continuity equation in a neutral p-type region, i.e. where no electric field is present thus the current density will only be diffusion current,

in low-injections and steady-state conditions, given a uniform photo-generation rate:

$$D_n \frac{\partial^2(\delta n)}{\partial x^2} - U_n = D_n \frac{\partial^2(\delta n)}{\partial x^2} - \frac{\delta n}{\tau_n} = 0. \tag{2.30}$$

Solution of this equation is possible, given that the second order differential equation roots are real, and reads:

$$\delta_n(x) = C_1\, e^{\frac{x}{L_n^2}} + C_2\, e^{-\frac{x}{L_n^2}} \tag{2.31}$$

where C_1 and C_2 are constants depending on the boundary conditions and $L_n = \sqrt{D_n\, \tau_n}$ is defined as the minority carriers diffusion length, i.e. the mean distance that diffusing electrons reach before recombining.

It becomes clear that, at steady-state conditions and between the boundaries of diffusion length, the excess carriers δ_n can be considered constant, given that C_1, C_2 and L_n are constants. There does not exist a preferential diffusion direction. This allows us to compute carriers propagation independently from the knowledge of carrier density; it is possible to build a steady-state weighting function of the photo-generation rate containing information on carriers propagation in the semiconductor. Optical phenomena and transport phenomena can therefore be considered independent between the boundaries of diffusion length.

This assumption is though valid only under low injection conditions; the net transition term U_n changes under high-injection conditions and both D_n and τ_n change consequently. Nevertheless, the assumption of uniform photo-generation rate has been made to obtain the carriers distribution result, though being an approximation of real conditions. In real conditions, photo-generation rate is not constant throughout the epitaxial layer of the pixel, leading to preferential carriers diffusion directions. The model can therefore have some imperfection if strong photo-generation gradients are present.

2.4 Modeling of charges transport

Given the conditions of optical and transport phenomena separability and with the aim in modeling the Internal Quantum Efficiency (η_i), we aim in developing a function that could map the behavior of photo-generated charges at a point in space inside the epitaxial layer as function of its electric field distribution; to be more specific, the desire is to develop a method allowing to compute the probability that an electron photo-generated at a point can be collected by the desired region, as for example the PhotoDiode or the Storage Node. We will call this function *Collection Probability*, which essentially represents a weighting function W. Notation-wise, the subscript “node” (W_{node}) is added when generally referring to the Collection Probability and can be replaced by either the subscript “PD” or “SN” to denote the respective Collection Probability.

We can easily understand that the product between G_{abs} and the newly computed weighting function W describes, per point in space, the number of photo-generated charges that are going to reach the desired node, assuming a random independent motion of charges. To dif-

ferentiate the weighting function of PhotoDiode and Storage Node, a subscript is introduced

We have seen that the Internal Quantum Efficiency of the desired node $\eta_{i,node}$ represents the number of photo-generated charges that are collected by the desired node. A spatial integration of the product between G_{abs} and W_{node} would give as a result the total number of photo-electrons generated in the epitaxial layer that can reach the desired node, $N_{coll-node}$, as shown in the following Eq.:

$$N_{coll,node} = \iiint G_{abs} \cdot W_{node} \cdot dV \tag{2.32}$$

where V is the epitaxial layer volume. In other words, it would be possible to compute the Internal Quantum Efficiency by means of the following Eq.:

$$\eta_{i,node} = \frac{N_{coll,node}}{N_{abs}} = \frac{\iiint G_{abs} \cdot W_{node} \cdot dV}{\iiint G_{abs} \cdot dV} \tag{2.33}$$

in which we have exploited Eq. (2.32) and the total number of photo-generated charges (which we remind it is supposed equal to the total number of absorbed photons N_{abs}) as given by the following:

$$N_{abs} = \iiint G_{abs} \cdot dV. \tag{2.34}$$

We have represented the Internal Quantum Efficiency described in Eq. 2.33 for a three-dimensional calculation.

Once the Internal Quantum Efficiency has been described, we can focus our attention on the method used to create W_{node} through non-equilibrium charge transport modeling as function of the electric field distribution inside the silicon epitaxial layer. A simplified approach to Boltzmann Transport Equation solution has been chosen to perform this task.

2.4.1 The Boltzmann Transport Equation

Non-equilibrium statistical mechanics seeks to describe thermodynamic systems which are out of equilibrium. The classic example of such a system is a fluid with temperature gradients in space causing heat to flow from hotter regions to colder ones, by the random but biased transport of the particles making up that fluid. For a general non-equilibrium setting, system solution would require integration of particle motion equation for all constituent particles; though some approximations can be made in situations where external forces or constraints are imposed over some macroscopic scale, as for example the application of an electric field, or voltage drop, in a semiconductor medium. In such cases, scattering at microscopic length and time scales can be described through the Boltzmann Transport Equation (BTE) [Vas]. In other words, the Boltzmann Transport Equation has been derived to describes the change of a macroscopic quantity in a thermodynamic system, such as energy, charge or particle number. Notably, for our purposes, Boltzmann Transport Equation will be used to describe the motion of out-of-equilibrium photo-generated electrons inside the silicon epitaxial layer.

2.4.1.1 Theoretical model

The Boltzmann Transport Equation is a semi-classical equation that is used to model the distribution of charges $f(\vec{r}, \vec{k}, t)$, where $\vec{r}$ is the position vector, $\vec{k}$ the momentum vector and t is time, in space and time in presence of external forces [Sin99]. There are three possible reasons for charges distribution to change over time:

1. Thermal motion, or diffusion, of electrons; charges change their position vector $\vec{r}$.
2. Influence of external forces like electric field. Both position $\vec{r}$ and momentum $\vec{k}$ vectors change over time due to the external force.
3. Scattering process, i.e. charge collision with the lattice or with other charges. Momentum vector $\vec{k}$ is affected by this process.

The total Boltzmann Transport Equation taking into account this three phenomena would then read:

$$\frac{\partial f(\vec{r}, \vec{k}, t)}{\partial t} = \left.\frac{\partial f}{\partial t}\right|_{diffusion} + \left.\frac{\partial f}{\partial t}\right|_{ext.forces} + \left.\frac{\partial f}{\partial t}\right|_{scattering} \tag{2.35}$$

Let us consider the simplest case, where no scattering process takes place, and analyze the terms on the right-hand side of the equation. The diffusion part will read as follows:

$$\left.\frac{\partial f}{\partial t}\right|_{diffusion} = -\frac{\partial f}{\partial \vec{r}} \cdot \vec{v} \tag{2.36}$$

where $\vec{v}$ is the velocity vector in the current state (where we have just replaced ∂t with $\frac{\partial \vec{r}}{\vec{v}}$). The external field part will read as follows:

$$\left.\frac{\partial f}{\partial t}\right|_{ext.forces} = -\frac{q}{\hbar}\,\vec{\mathcal{E}}_{ext}\,\frac{\partial f}{\partial \vec{k}} \tag{2.37}$$

where $\vec{\mathcal{E}}_{ext}$ is the external applied force, in our case being the electric field, and $\hbar$ the reduced Planck's constant. Eq. (2.37) simply represent the semi-classical law of motion [Kel85].

The Boltzmann Transport Equation is a complex equation to be solved straightforward; some techniques have been though developed to help numerically solve the problem. Notably, the random walk Monte Carlo technique applied to one-particle distribution function has been shown to satisfy the Boltzmann Transport Equation for a homogeneous system for a sufficiently long simulation time [Fer91]. The Monte Carlo technique has been widely used over the last 30 years as a numerical method to simulate non-equilibrium transport in semiconductor materials and devices [JR83]; [Hes12].

The Monte Carlo technique is used to simulate the free particle motion (referred to as the *free flight*) terminated by instantaneous random scattering events. Its algorithm consists of generating random free flight times for each particle, choosing the type of scattering occurring at the end of the free flight, changing the final energy and momentum of the particle after

scattering, and then repeating the procedure for the next free flight. Some Monte Carlo techniques uses an ensemble of particles to represent the physical system of interest, thus allowing to simulate the charges distribution as function of time.

In our case, a simpler approach of the Monte Carlo technique will be used to simulate the single particle free flight. In a first approximation, scattering process has not been taken into account. This approximation can be tolerated given that the simulations aims to model the steady-state response of the pixel structure, and thus the precise path of each single charge is not of great interest. This reduces to the time-step solution of the particle state equation as function of an applied external field given by Eq. (2.38), derived from Eq. (2.37) given that the single particle distribution can be represented by its momentum vector $\vec{k}$, also defined as wavevector due to the quantum nature of particles under analysis.

$$\frac{\partial \vec{k}}{\partial t} = -\frac{q}{\hbar}\,\vec{\mathcal{E}}_{ext} \tag{2.38}$$

Through use of the motion equation $\partial \vec{r}/\partial t = \vec{v}$, it is possible to retrieve, knowing the velocity at a time instant, the particle's position per each time step. In order to retrieve the velocity, and thus the charge position, it mandatory to explicit the wavevector $\vec{k}$ as function of the velocity vector. It is supposed that all free particles are generated in the lowest silicon band, the X band, in which is known that particle energy E has a parabolic behavior with respect to wavevector, as shown by Eq. (2.39), where m_c is the electron mass in the valley; relation between velocity and wavevector can thus be found in Eq. (2.40), using the mass-energy equivalence [Fer91].

$$E(k) = \frac{\hbar^2\,|\vec{k}|^2}{2\,m_c} \tag{2.39}$$

$$|\vec{v}| = \sqrt{\frac{2\,E(\vec{k})}{m_c}} = \frac{\hbar\,|\vec{k}|}{m_c} \tag{2.40}$$

It is possible to realize that, given all these conditions, the final Boltzmann Transport Equation for single particle without scattering would read as in Eq. (2.38), since the right-hand side term in Eq. (2.36) vanishes as we have no dependence of the single particle wavevector on its velocity (hence, on its position):

$$\partial \vec{v} = -\frac{q}{m_c}\,\vec{\mathcal{E}}_{ext} \cdot \partial t. \tag{2.41}$$

Finally, given a small increase in time Δt, it is possible to retrieve the final charge wavevector $\vec{v}_{fin}$, as given by Eq. (2.42) given the initial particle wavevector $\vec{v}_{ini}$, and consequently the final charge position $\vec{r}_{fin}$, given by Eq. (2.43) given the initial charge position $\vec{r}_{ini}$.

$$\vec{v}_{fin} = \vec{v}_{ini} + \Delta\vec{v} = \vec{v}_{ini} - \frac{q}{m_c}\,\vec{\mathcal{E}}_{ext} \cdot \Delta t; \tag{2.42}$$

$$\vec{r}_{fin} = \vec{r}_{ini} + \Delta\vec{r} = \vec{r}_{ini} + \vec{v}_{fin} \cdot \Delta t. \tag{2.43}$$

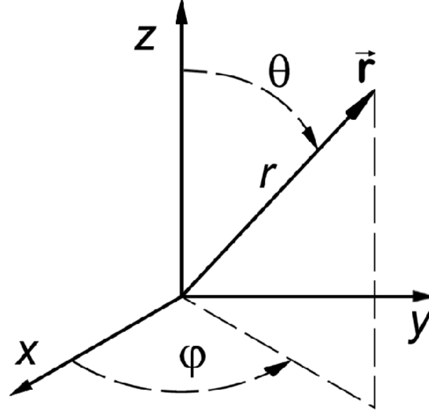


Figure 2.13: Schematic of polar (θ) and azimuthal (ϕ) angles for a general vector $\vec{r}$ given the Euclidean space of orthogonal vectors $\hat{x}$, $\hat{y}$, $\hat{z}$.

2.4.1.2 Usage of Boltzmann Transport Equation for charges collection probability

We have so far described the simplifications made on the main Boltzmann Transport Equation, adapting it to a single particle parabolic band motion. As previously said, scattering has not been taken into account, but it could be added to our model to slightly improve its efficiency as well as giving the model a temperature dependence.

Let us try to model single particle motion inside the silicon epitaxial layer, keeping in mind that the desire is to recreate a mapping function giving the probability that a number N_{carr} of charges, photo-generated in a small unit volume in space $\vec{r} = x\,\hat{x} + y\,\hat{y} + z\,\hat{z}$ of the Euclidean space[1], reach the desired region, and thus can be considered "collected". It becomes clear that a high number of charges per unit volume in space is therefore required to be simulated to obtain a sufficiently high statistic; we will refer to the number of charges simulated per unit volume in space as the number of throws N_{throw}.

One thing has to be noted before getting into the details of the model initial conditions: one Collection Probability weighting function is created per each interesting region in pixel. Notably, it is possible to compute the Collection Probability weighting function for the PhotoDiode as well as for the Storage Node; it has though to be noted that electrons reaching the region "Y" while Collection Probability weighting function is being calculated for region "X" will be considered lost. This allows to take into account the presence of other potentially collecting reversely biased $p-n$ junctions and to improve modeling truthfulness.

In order to perform the simulation, initial charges energy E_{ini} has to be given. It is possible to suppose that initial charges energy will be dependent on the incoming lightwave that has them generated. We will give two more assumptions to model the charges initial energy:

[1] $\hat{x}$, $\hat{y}$ and $\hat{z}$ are the unitary vectors of the orthogonal dimensions of the Euclidean space

- after photo-generation, photon energy is equally distributed between the electron and the hole;
- the electron-hole pair is generated from an electron found at the top of the valence band that is promoted to the conduction band.

This initial energy modeling results in a linear energy dependence on the lightwave frequency, or an inverse dependence on lightwave wavelength, as given by the photoelectric effect reproduced in Eq. (2.44), where h is the non-reduced Planck's constant, c the speed of light and E_g the energy bandgap of the semiconductor [KS01].

$$E_{ini} = \frac{1}{2}\left(\frac{h\,c}{\lambda} - E_g\right) \tag{2.44}$$

From this latter, it becomes clear that the definition of a Collection Probability weighting function per each considered wavelength is required. Initial charge energy will therefore define its initial velocity, initial electron direction can be randomly selected or, since no scattering process is taken into account, the entire space can be subdivided as function of the number of throws. Initial wavevector in 3D will then be modeled as follows:

$$\vec{k}_{ini,p} = \frac{\sqrt{2\,E_{ini}\,m_c}}{\hbar}\left(\sin\theta_p\,\cos\varphi_p\,\hat{x} + \sin\theta_p\,\sin\varphi_p\,\hat{y} + \cos\theta_p\,\hat{z}\right), \tag{2.45}$$

where θ_p and φ_p are respectively the polar and the azimuthal angle, depicted in Fig. 2.13 for the $p-th$ throw.

Collection Probability weighting function has to be defined per each point in space. Therefore, the silicon epitaxial volume has been divided in small rectangular cuboid voxels, where a voxel can be defined as an infinitesimal volume $\delta V = \delta x\,\delta y\,\delta z$. W can be therefore defines as the number of electrons reaching a certain zone, in other words being collected by the desired node, N_{coll} over the total number of electrons simulated per voxels, as given by Eq. (2.46).

$$W(x,y,z) = \frac{N_{coll}(x,y,z)}{N_{throw}} \tag{2.46}$$

Finally, boundary conditions have to be taken into account for the correct operation of the simulation. In our simplified case, we will suppose that, whenever reaching any surface, the simulated charge will immediately recombine and therefore considered lost; notably, surface recombination velocity could also be modeled, but that has not been the aim in our modeling. Instantaneous charge recombination is also considered when the charge is reaching the pixel border, thus the planes that are perpendicular to the Si/SiO_2 interface; improvements of the model could be performed through addition of supplementary neighbor pixels to take into account cross-talk charges, i.e. charges photo-generated in a pixels that are collected by a neighboring pixel.

Fig. 2.14 summarizes the method developed to model the Collection Probability weighting function on the silicon epitaxial layer. The epitaxial layer volume has been divided into

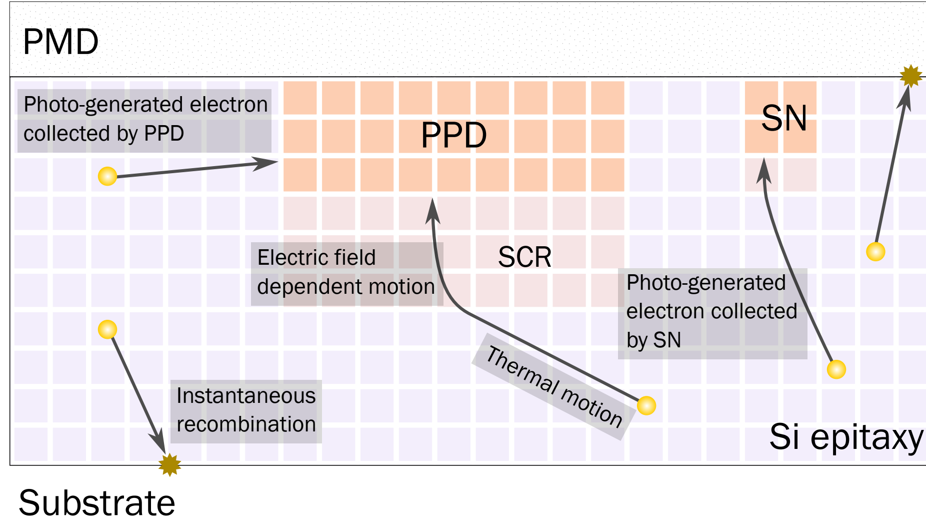


Figure 2.14: Explanation of the modeled Boltzmann Transport Equation inside the silicon epitaxial layer for a single pixel.

sub-voxels, N_{throw} electrons are simulated per each voxel with an incident light wavelength dependent initial energy E_{ini} and initial wavevector k_{ini}, the charge successively moves following the simplified single particle Boltzmann Transport Equation as function of the electric field distribution; instantaneous recombination at the boundary conditions is taken into account the Collection Probability weighting function is the result of per-point collected charges over the total number of generated charges.

As repeatedly mentioned, the charge responds to the local electric field. We will focus now on the building of the electric field distribution inside the silicon epitaxial layer.

2.4.1.3 Simple modeling of the Electric Field

In order to model the electric field distribution, we make the simple assumption that all n-p junctions are abrupt; this allows to easily calculate the electric field distribution inside the epitaxial volume. A more appropriate simulation of the electric field distribution can be performed through the solution of the Poisson's equation; nevertheless, Poisson's equation solution would require finite-element modeling, which is not in the aim of our simple approach.

We will therefore use the abrupt junction diode model [Sze08] for calculation of the electric field. Notably, given a constant donor density N_D and a constant acceptor density N_A, it is possible to first obtain the built-in voltage V_{bi} of the structure, given as follows (in the 1D example):

$$V_{bi} \approx \frac{k_B T}{q} \ln \left(\frac{N_D N_A}{n_i^2} \right), \tag{2.47}$$

where k_B is the Boltzmann constant, T is the temperature and n_i the intrinsic electrons concentration in silicon. Once the built-in voltage is known, it is possible to compute the depletion region, or Space Charge Region, width W. The Space Charge Region width had already been given in Chapter 1 as function of a reverse bias V_R; a reminder of the equation is given hereafter:

$$W = \sqrt{\frac{2\epsilon_s}{q} \frac{N_A + N_D}{N_A N_D} (V_{bi} + V_R)}. \tag{2.48}$$

Notably when taking into account the Space Charge Region projected by the PhotoDiode junction or the Storage Node junction, it is crucial to take into account the fact that reverse bias is applied after the reset operation; V_R has therefore been modeled at the pinning voltage V_{pin} for PhotoDiode and at the $V_{DD-RST} - V_{th}$ voltage for the Storage Node, were V_{DD-RST} is the source polarization voltage of the RST transistor and V_{th} its threshold voltage.

It is possible to derive the extension of the Space Charge Region in the n and p regions, respectively W_n and W_p, through the following:

$$W_n = \sqrt{\frac{2\epsilon_s}{q} \frac{N_A}{N_D (N_A + N_D)} (V_{bi} + V_R)}, \tag{2.49}$$

$$W_p = \sqrt{\frac{2\epsilon_s}{q} \frac{N_D}{N_A (N_A + N_D)} (V_{bi} + V_R)}. \tag{2.50}$$

Finally, the electric field distribution as function of space can be derived as [SN06]:

$$\begin{aligned} \mathscr{E}(x) &= -\frac{qN_A}{\epsilon_s} (x + W_p) \qquad \text{for } -W_p \leq x \leq 0 \\ \mathscr{E}(x) &= -\frac{qN_D}{\epsilon_s} (W_n - x) \qquad \text{for } 0 \leq x \leq W_n \end{aligned} \tag{2.51}$$

Doping gradient generated electric field has also been taken into account and modeled, in order to correctly model the interface between the epitaxial layer and the deep substrate, as well as the p-doped layer generating potential barriers like the Anti Punch-Through and the PWELL. In the case of a p-doping gradient, the built-in voltage will read as follows:

$$V_{bi} = \frac{k_B T}{q} \ln \left(\frac{N_A^+}{N_A} \right) \tag{2.52}$$

where N_A^+ denotes the higher acceptor concentration in p^+ region and N_A the lower acceptor concentration in the p region. Similarly to what has been previously done, we can now calculate the Space Charge Region extensions in the p^+ and p regions as well as the electric field profile. An example of the electric field profile in 1D between the epitaxial layer and the deep substrate is given in Fig. 2.15. This simple method gives similar results to the solution of Poisson's equation through finite-elements for a $p^+ - p$ doping gradient.

Finally, it is widely known how abrupt corners can cause singularity in the calculation of the Poisson's equation. Similarly in our case, it would be hard to define a proper electric field

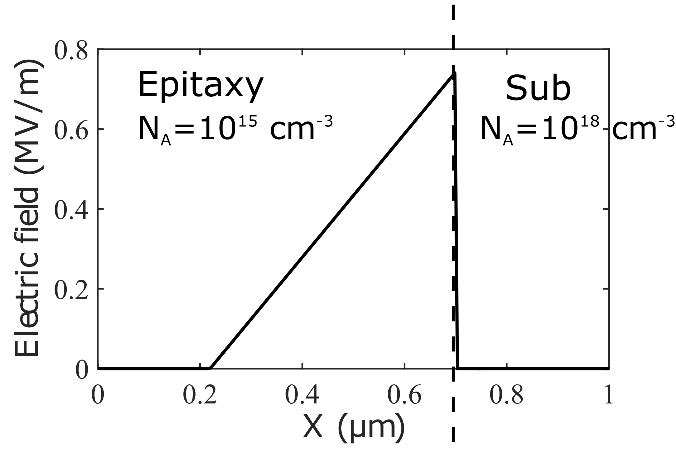


Figure 2.15: Electric field generated due to a *p*-doping gradient in an abrupt junction. Acceptor concentration of the Epitaxy and the Substrate are constant and respectively of $10 \times 10^{15}\,\text{cm}^{-3}$ and $10 \times 10^{18}\,\text{cm}^{-3}$.

distribution around the corners; angles are therefore not taken into account for our electric field modeling. Electric field will be modeled only in the $\hat{x}$, $\hat{y}$ and $\hat{z}$ parallel directions.

2.4.2 The Straight Line propagation

The single particle Boltzmann Transport Equation can be a valid method to define the Collection Probability weighting function in space. Nevertheless, it requires small time-step resolution to accurately model the particle motion; 3D simulations could therefore require an important amount of time before, especially when simulating big pixels for multiple wavelengths. In order to accelerate the development process of the Collection Probability weighting function, a simpler and faster approach has been modeled.

This new modeling supposes that charges that have been photo-generated in the epitaxial volume propagate on a straight line, given a random initial direction, without the influence of any other external term as for example scattering or local electric field. The model has the advantage in using just geometrical factors to understand if the photo-generated charge can or cannot reach the desired node, thus highly improving the timing performances, not requiring any stepping-time simulation.

The Straight Line propagation (SL) model shares some similarities with the Boltzmann Transport Equation model:

- the system under analysis, i.e. the epitaxial layer, is subdivided in voxels to allow for a spatial calculation of the Collection Probability weighting function;
- any charges reaching the boundaries of the system, the epitaxial layer volume, before being collected by the required node will considered as lost;

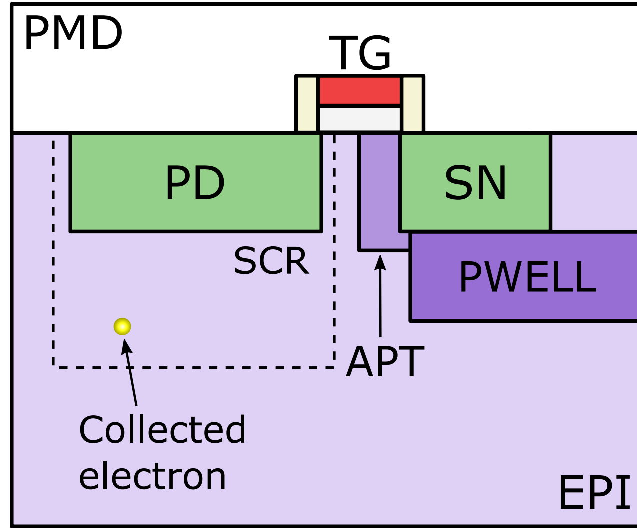


Figure 2.16: Schematic of the electron collection as modeled by the Straight Line model. A pixel cross-section is depicted, presenting the PhotoDiode with its Space Charge Region, the TG, the Storage Node and the PWELL. For sake of simplicity, other transistors, as for example the RST transistor, have not been depicted. The electron, generated or reaching the PhotoDiode Space Charge Region is considered collected by this latter.

- if a charge reaches another node Y while we are building the Collection Probability weighting function for node X, it will be considered as lost.

This very simple modeling has though some requirements in order to successfully take into account the behaviors of particles modeled under the Boltzmann Transport Equation.

2.4.2.1 Modeling of p-n junction Electric Field

When a free electron is reaching a region with electric field, it would tend drift following the opposite direction of field lines; if the electric field is high enough and the electron energy is not high, the electric field will successfully drive the electrons towards the n-doping region. The electric field presence can therefore be modeled as a region in which the charge is considered collected. For a better understanding, the charge depicted in Fig. 2.16 which has attained the electric field region can be considered collected by the PhotoDiode.

As previously said, this simplification is valid if the charge energy is sufficiently small. It has been shown before that the charges initial energy depends on the incoming light wavelength, as described in Eq. (2.44). It is evident that electrons generated by shorter wavelengths will have a higher initial energy ($E_{ini} \approx 0.99\,\text{eV}$ at 400 nm is much higher compared to $E_{ini} \approx 0.39\,\text{eV}$ at 650 nm), so the electric field model would be less accurate for shorter wavelength; nevertheless, it has to be remembered that charges photo-generation at shorter

wavelengths (400 nm to 500 nm) is primarily superficial and thus charges infrequently interact with electric fields that are found to be more profound. This latter observation mitigates the inaccurate Collection Probability weighting function for shorter wavelengths with the Straight Line propagation model.

2.4.2.2 Modeling of Potential Barriers

Finally, it is important to be able to model potential barriers, as for example the ones represented by the p-doping concentration gradient. Let us focus on the barrier between the PWELL and the epitaxial layer: the PWELL is often used to shield the n-diffusions from charges roaming at the bottom of the epitaxial layer. It is nevertheless easy to understand that, if having a sufficient energy, a free charge has a higher probability of overcoming the PWELL barrier and diffuse towards shallower zones. Charges chance to overcome the electric field barrier also depends on the attacking angle with which they reach the barrier. To better explain, the velocity of a charge attacking the barrier at an oblique angle will have a vertical and an horizontal component. At a given energy, the vertical component of the oblique impinging charge will be smaller in comparison to a charge impinging perpendicularly. Supposing that the electric field generated by the PWELL barrier has only a vertical component, it has a higher chance of rejecting the oblique impinging charge, given its smaller vertical component. We have therefore chosen the transmission factor T through the use of single particle Boltzmann Transport Equation simulations. The choice can be resumed as follows:

- A high number of charges (100) has been simulated per each point in space below the $p^+ - p$ junction, defined as z_0, to determine the spatial probability to pass through the PWELL barrier;
- only charges having the possibility to reach the region past the electric field barrier have been taken into account for the calculation of T, charges propagating in the opposite direction are of course of no interest;
- in order to determine the T parameter per every impinging wavelengtht, charges initial energy has been given following the photoelectric effect model presented in Eq. (2.44) per each wavelength of the considered spectrum (from 400 nm to 950 nm with steps of 50 nm);
- T is calculated by averaging the resulting pass-through probability $P(x, y, z)$ in space as given by Eq. (2.53).

$$T = \frac{1}{x_{max}} \frac{1}{y_{max}} \frac{1}{(z_{max} - z_0)} \sum_{0}^{x_{max}} \sum_{0}^{y_{max}} \sum_{z_0}^{z_{max}} P(x, y, z) \tag{2.53}$$

Results of transmission factor simulation as function of wavelength and PWELL acceptor concentration can be appreciated in Fig. 2.17. High energy charges, as the ones generated by shorter wavelengths, are easily passing through the electric field barrier, though it has

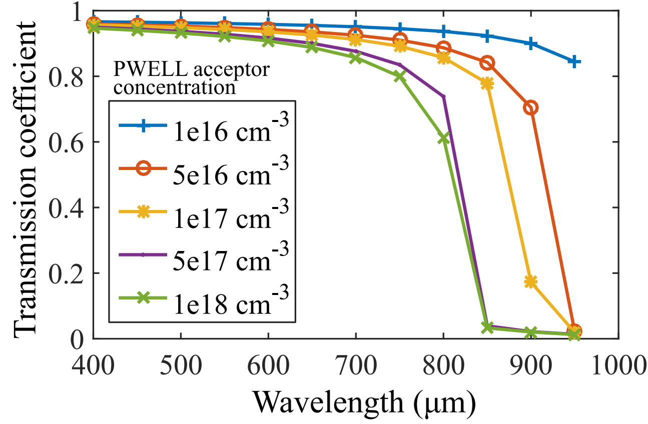


Figure 2.17: Transmission coefficient of the PWELL barrier as function of wavelength and PWELL doping, as simulated with the Boltzmann Transport Equation model given an abrupt $p - p^+$ junction.

to be kept in mind that high energy charges are generated close to the surface from shorter wavelengths and do never get in contact with the PWELL barrier. On the other hand, longer wavelengths tend to generate charges deeper in the epitaxial layer; the PWELL barrier is therefore more efficient at rejecting those charges carrying smaller energy. Moreover, shielding effect improves with the increase in the PWELL doping, as expected.

Finally, the electric field presence between the epitaxial layer and the deep substrate has not been taken into account; charges reaching the substrate will be considered as lost.

2.4.3 Calculation of Quantum Efficiency and Parasitic Light Sensitivity

Once both the G_{abs} and W_{node} have been calculated, either using Boltzmann Transport Equation or Straight Line (SL) approximation, their usage is needed for computing the image sensor Quantum Efficiency as well as its Parasitic Light Sensitivity.

Let us start with the Quantum Efficiency: as previously said, spatial integration of the product between G_{abs} and the W_{node}, divided by the total number of absorbed photons N_{abs} per units of time, gives as result the Internal Quantum Efficiency (η_i). Optical Quantum Efficiency (η_o) is now required to compute the full Quantum Efficiency. Calculations of η_o are simply done using the results of the FDTD simulations, i.e. exploiting the ratio between the number of absorbed photons N_{abs} per units of time and the total number of impinging photons N_{tot} per units of time. N_{tot} can be recovered knowing the Plane Wave source Poynting vector S_{source} as from Eq. (2.24). were Σ is the pixel surface $\Sigma = p^2$, given the pixel pitch p. We can therefore compute η_o as follows:

$$\eta_o = \frac{N_{abs}}{N_{tot}} = \frac{\iiint G_{abs} \cdot dV}{\iint \Re\{\vec{S}_{source}\} \cdot d\Sigma} \tag{2.54}$$

Remembering that the number of photo-generated charges per units of time is consider equal to the number of absorbed photons N_{abs} per units of time, we can write the Quantum Efficiency as follows:

$$QE = \eta_o \times \eta_i = \\ = \frac{\iiint G_{abs} \cdot dV}{\iint \Re\{\vec{S}_{source}\} \cdot d\Sigma} \frac{\iiint G_{abs} \cdot W_{node} \cdot dV}{\iiint G_{abs} \cdot dV} = \\ = \frac{\iiint G_{abs} \cdot W_{node} \cdot dV}{\iint \Re\{\vec{S}_{source}\} \cdot d\Sigma} \tag{2.55}$$

Only the simulations mapping functions as well as the source input power would be required to compute the image sensor Quantum Efficiency.

In order to compute the image sensor Parasitic Light Sensitivity we would need the Photo-Diode and Storage Node Quantum Efficiency ratio. It becomes clear that, since both Quantum Efficiency have been calculated using the same optical simulation result, the two Quantum Efficiency would have the denominator in common that gets suppressed by the ratio. This concept appears of crucial in the Parasitic Light Sensitivity modeling, stating that *Parasitic Light Sensitivity is independent of illumination intensity*, as it will be shown further on with experimental data. In the end, the Parasitic Light Sensitivity calculation would read:

$$PLS = \frac{QE_{SN}}{QE_{PD}} = \frac{\iiint G_{abs} \cdot W_{SN} \cdot dV}{\iiint G_{abs} \cdot W_{PD} \cdot dV} \tag{2.56}$$

2.5 Inter-comparison of methods for modeling Parasitic Light Sensitivity

We have seen how to develop two methods for simulating Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors; the first method is based on a time-step solution of single particle Boltzmann Transport Equation, building the electric field distribution through consideration of abrupt $p-n$ and p^+-p junctions; the second method is based on a simplification of charges behavior, considering their propagation just on a straight line, though electric fields effect have been taken into account through direct acceptance in the n-doped region, for the $p-n$ junction electric field, or by a transmission parameter modeled on the p^+-p junction electric field barrier. We will refer to the first method as the **Boltzmann Transport Equation model** and to the second one as the **Straight Line model**.

We will hereafter compare the results of the two given methods to understand if the behavior is comparable. Even if mathematical theory had been given in 3D, simulations have been performed in 2D and results are to be taken as 2D results. Motivation, advantages and disadvantages of 2D simulations will be given in Sec. 2.6. Simulations have been performed

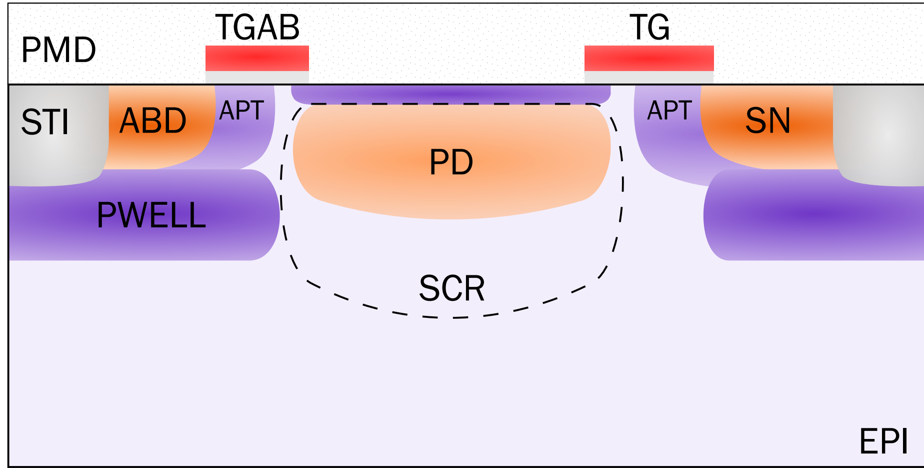


Figure 2.18: Schematic of the Global Shutter pixel modeled in the simulations. The Back-End Of Line (BEOL) layers are not shown for sake of simplicity. The pixel presents a PhotoDiode (PD) with its Space Charge Region, a Storage Node (SN), a Transfer Gate (TG), an AntiBlooming Gate (TGAB) and its drain (ABD), the Anti Punch-Through (APT) and PWELL doping layers, the Shallow Trench Isolations (STI) and the Pre-Metal Dielectric (PMD) which passivates the Front-End Of Line (FEOL). The epitaxial layer (EPI) represents the base on which the different doping implants are performed.

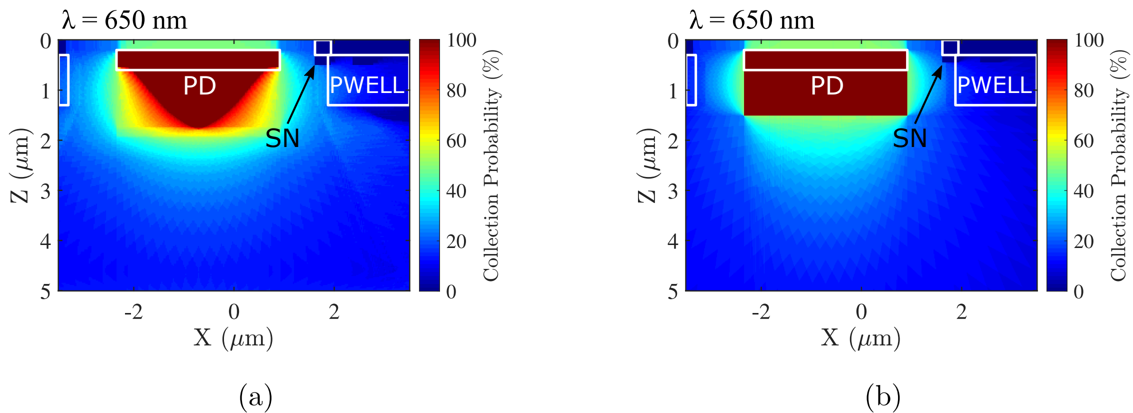


Figure 2.19: PhotoDiode Collection Probability weighting functions for both (a) Boltzmann Transport Equation and (b) Straight Line methods at $\lambda = 650\,\text{nm}$.

following the structure of a typical 5T Global Shutter pixel, on which the electric field distribution has been modeled. For an easier analysis, only the PhotoDiode (PD), Storage Node (SN) and PWELL are shown. For a complete pixel structure please refer to Fig. 2.18.

Fig. 2.19 shows the Collection Probability weighting function for the PhotoDiode resulting from (a) the Boltzmann Transport Equation model and (b) the Straight Line model, computed for charges photo-generated by a wavelength of $\lambda = 650\,\text{nm}$. At a first glance, it becomes clear

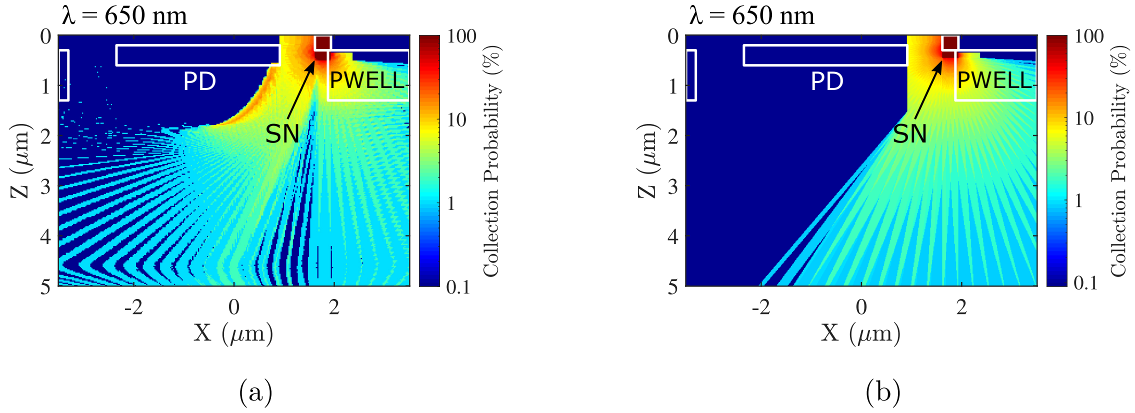


Figure 2.20: Storage Node Collection Probability weighting functions for both (a) BTE and (b) Straight Line methods at $\lambda = 650\,\text{nm}$.

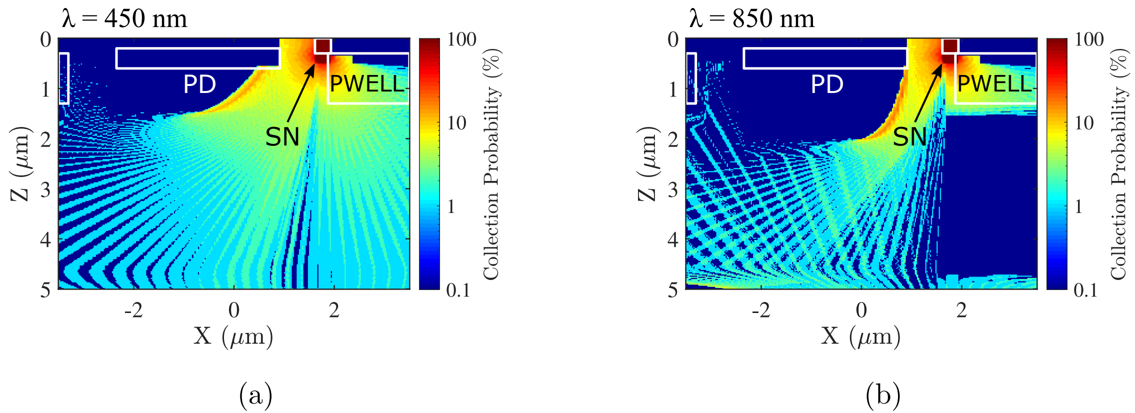


Figure 2.21: Storage Node Collection Probability weighting functions given by Boltzmann Transport Equation method at two different wavelengths: $\lambda = 450\,\text{nm}$ and $\lambda = 850\,\text{nm}$.

that charges photo-generated in the PhotoDiode area have maximum probability of being collected by the PhotoDiode, supposing that those charges cannot escape the PhotoDiode region due to the surrounding electric field. Moreover charges photo-generated in the Storage Node region are supposed incapable to escape, thus incapable to reach the PhotoDiode, their collection probability is therefore null. Due to the chosen "electron capture" mechanism in the Straight Line model, the collection around the $p-n$ junction is approximated with respect to the Boltzmann Transport Equation model, where a non-steep change in the Collection Probability can be seen when moving further from the $p-n$ junction.

In a same fashion, Fig. 2.20 shows the Collection Probability weighting function for the Storage Node resulting from the Boltzmann Transport Equation model 2.20a as well as the Collection Probability weighting function for the Storage Node resulting from the Straight Line model 2.20b in logarithmic scale to better appreciate the weak collection further away

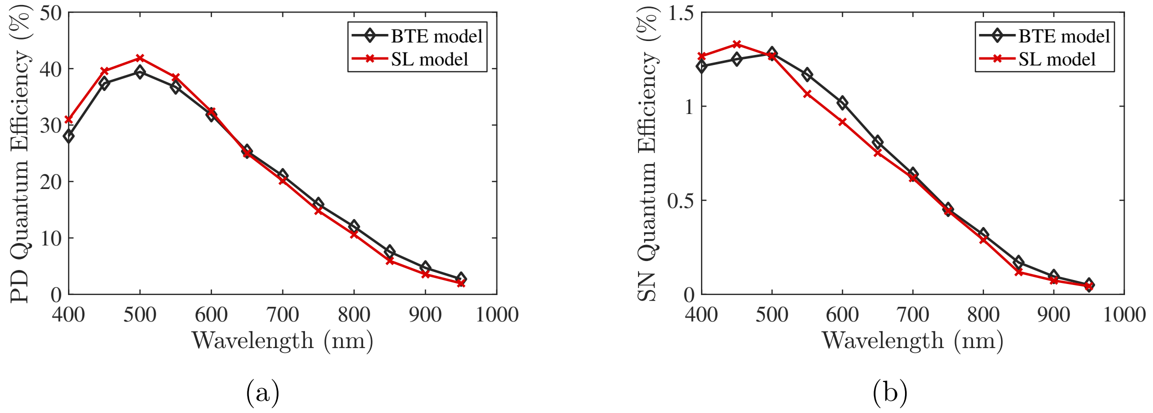


Figure 2.22: Comparison of the Boltzmann Transport Equation and Straight Line methods to simulate PD and Storage Node Quantum Efficiencies.

from the Storage Node. Results are shown for charges photo-generated by a wavelength of $\lambda = 650\,\text{nm}$. Similarly to Collection Probability weighting functions on PhotoDiode, charges photo-generated in the Storage Node region have maximum probability of being collected by the Storage Node; conversely, charges photo-generated in the PhotoDiode region are unable to reach the Storage Node.

In order to appreciate the evolution of the Collection Probability for the Storage Node, Fig. 2.21 shows the simulation result for charges photo-generated at (a) 450 nm and (b) 850 nm. It can be seen how, at a longer wavelength, charges have lesser change of passing through the PWELL barrier. Nevertheless, non-negligible charge collection can be observed all over the epitaxial layer.

We now would like to compare the Quantum Efficiency results using the same G_{abs} for both methods. Fig. 2.22 shows both the comparisons for (a) PhotoDiode and (b) Storage Node Quantum Efficiency. The two methods give similar results, acknowledging slight differences in both PhotoDiode and Storage Node Quantum Efficiency.

Given the Quantum Efficiency results, we expect that the two methods would give similar Parasitic Light Hardness (1/PLS) results. Fig. 2.23 shows the Parasitic Light Sensitivity comparison between the two methods; as expected, the two modeled Parasitic Light Hardness (1/PLS) are quite similar, though some differences may be appreciated (around 550 nm and around 850 nm) as a small shift in the Storage Node Quantum Efficiency drives to an important shift in the resulting Parasitic Light Hardness (1/PLS).

2.5.1 A comparison tool: TCAD simulations

TCAD simulations are a powerful tool to simulate charge propagation through finite-element solution of the drift-diffusion, continuity and Poisson's equations. TCAD is the method of

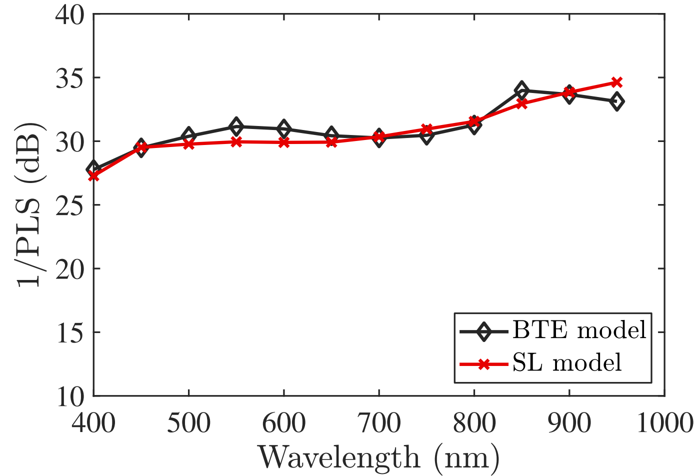


Figure 2.23: Comparison between the Boltzmann Transport Equation and Straight Line models for Parasitic Light Hardness (1/PLS) simulation.

reference when accurate simulations of the semiconductor physics are required.

TCAD simulations for Parasitic Light Sensitivity modeling require photo-generation rate as input to solve the drift-diffusion equations. FDTD simulations could be performed exploiting the Synopsis suite, which also includes these simulations. Nevertheless, it has been shown that the FDTD simulator we have used so far is more accurate and computationally efficient [RF15]. It is important to notice that grid adaptation, from finite-difference rectangular grid to finite-element triangular grid, has to be done in order to transfer the photo-generation rate to the TCAD simulation input. This process has been done through a MATLAB script, given the basis of what had first been developed by Dr. Michael David Kelzenberg in his thesis [Kel10], and modified to adapt it to our scope (cf. Appendix A).

In order to compare our model to something more realistic, we have reproduced the pixel structure following accurate doping profiles that have been taken from Secondary Ion Mass Spectroscopy (SIMS) measurements. Different models have been activated: high field saturation of both electrons and holes, Philips unified mobility model (PhuMob) [Kla90], Shockley-Read-Hall (SRH) and Auger recombination. This could help to prove that our simplified model can anyway approximate the more realistic solutions, allowing for a faster modeling of the Parasitic Light Sensitivity at different illumination conditions. It is here reminded that the use of the drift-diffusion model exploited by TCAD simulations requires previous knowledge on the charge photo-generation, as charge density is a crucial input for the simulations. This leads to multiple TCAD simulations at every illumination condition that is tested. On the other hand, the developed model allows to generate only once the Collection Probability weighting function and that can be reused in combination with different illumination conditions, accelerating the whole simulation process. Fig. 2.24 shows the simulated 2D structure. All the elements that we have seen before are present in the TCAD simulated structure as well, with one addition: the RST transistor. Simulation of pure floating nodes in TCAD are time-consuming and often do not converge; in order to solve this issue, a RST transistor is

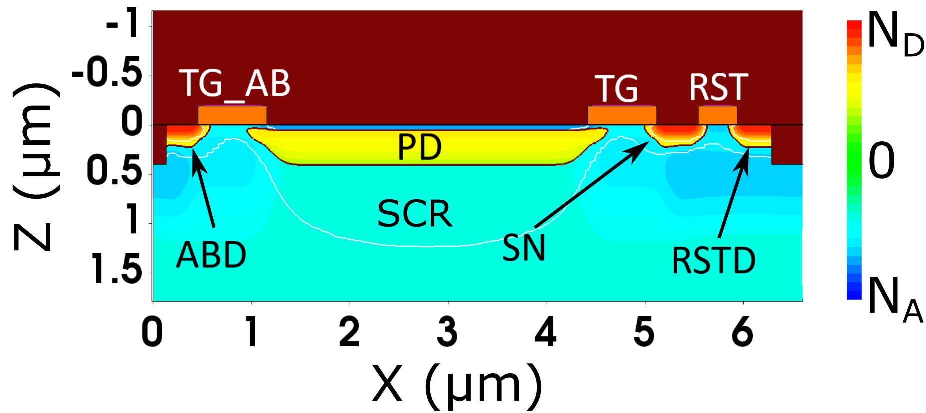


Figure 2.24: Structure simulated in TCAD for Parasitic Light Sensitivity modeling. The structure contains a PhotoDiode (PD), a Transfer Gate (TG), an AntiBlooming Transfer Gate (TGAB), a Storage Node (SN) and a Reset Gate (RST) with the purpose in allowing the Storage Node to be floating. The Space Charge Region is delimited by the thin white line. In the color scale, hotter tones indicate prevalence of donor concentration (N_D) while cooler tones indicate prevalence of acceptor concentration (N_A).

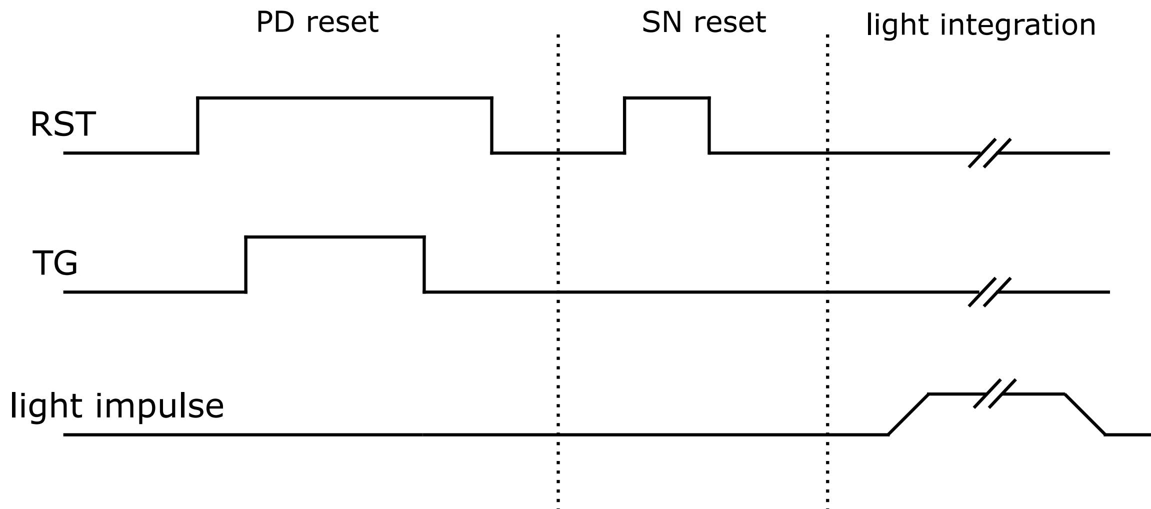


Figure 2.25: Time diagram of the control signals exploited in TCAD simulations to reset the PhotoDiode via the RST and TG gates, reset the Storage Node via the RST gate and then integrate light. Light impulse represents the photo-generation given by FDTD simulations.

present to help making the Storage Node potential floating.

We will follows the steps that have been performed to simulate Parasitic Light Sensitivity with the help of TCAD simulations:

- First, the Poisson's equation is solved to determine the thermal equilibrium status of

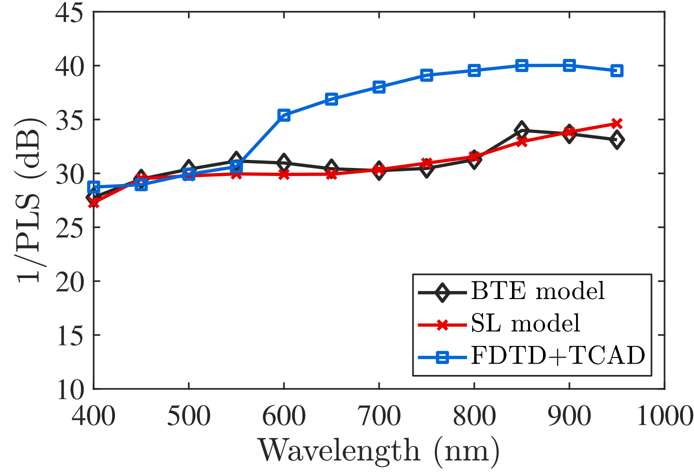


Figure 2.26: Parasitic Light Sensitivity simulation comparison of the three modeling methods: Boltzmann Transport Equation model, Straight Line model and FDTD+TCAD simulations. The FDTD simulations results exploited in the three methods are the same.

the structure.

- Reset operation of the PhotoDiode is performed, first the transistor RST is turned on and successively the TG transistor is turned on; while both transistors are on, electrons flow from the PhotoDiode to the Storage Node. The operation is completed when no electrons are left in the PhotoDiode; first the TG transistor is turned off and soon after the RST transistor is turned off.
- An operation of Storage Node reset is performed. The transistor RST is turned off and few time after turned off.
- The photon integration can now start. Photo-generation, given by the FDTD simulations, last for some millisecond and then turned off, the simulation ends.

The control signals of these steps (TG and RST, knowing that TGAB is constantly biased at 0 V, ABD and RST are constantly biased at 3.3 V) are synthesized in Fig. 2.25, where the light impulse represents the photo-generation given by FDTD simulations. The outcome of TCAD simulation will be a file with the number of charges integrated in the node as function of time, one file for the PhotoDiode and one file for the Storage Node. It will be sufficient to make the time derivative of charges number to retrieve the sensitivity $\mathcal{S}$ of the two nodes. Parasitic Light Sensitivity can therefore be computed from the sensitivities ratio.

We have compared the TCAD simulations results with the developed models and plotted in the more suitable form of Parasitic Light Hardness (1/PLS), as can be seen in Fig. 2.26. An important difference between the model and the TCAD simulations can be appreciated. This difference may be relative to a wrong estimation of the charges diffusing through the PWELL and reaching the Storage Node. In the developed models, an over estimation may be caused by the use of abrupt junctions, like the graded p-doping junction of the PWELL.

Similarly, in TCAD simulations an under estimation of the Storage Node light sensitivity at longer wavelengths may be caused by the approximated doping profiles exploited. In any case, as it will be seen further on, the measured Parasitic Light Sensitivity on real 5T CMOS Image Sensors do not show a jump around $\lambda = 600\,\text{nm}$, which leads to believe in a wrong estimation of the TCAD simulations. Nevertheless, the two models seem to reproduce a similar behavior of Parasitic Light Hardness (1/PLS) as function of the wavelength, with the exception of the "jump" at $\lambda = 600\,\text{nm}$; this can be a promising result, meaning that the model could be used not as an absolute reference, but as a relative reference to compare different structures.

2.6 Limitations of 2D simulations

So far, we aimed to develop a fast and efficient method to develop Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors. The fast paradigm passes also through the use of 2D simulations. Compared to 3D simulations, 2D simulations are surely more rapid, given the important complexity increase when adding the third dimensions. 3D simulations are also known for being memory consuming and sometimes, if meshing is too coarse, they could easily diverge.

Nevertheless, 2D simulations need a correction factor in order to take into account the missing third dimension and simulate the behavior of a real 3D device. Our simulations do not make any exception. The equations we have presented for the Quantum Efficiency calculations, Eq. (2.55), comes in handy to find the geometrical factor. When integrating G_{abs} and the W_{node} in 2D, one of the dimension is therefore considered constant; if we give y as the constant dimension, the Quantum Efficiency would result:

$$\begin{aligned} QE_{node} &= \frac{\iiint G_{abs} \cdot W_{node} \cdot dV}{\iint \Re\{\vec{P}_{source}\} \cdot d\Sigma} \\ &= \frac{w_{node} \iint G_{abs} \cdot W_{node} \cdot dxdz}{p \int \Re\{\vec{P}_{source}\} \cdot dx} \end{aligned} \tag{2.57}$$

where w_{node} is given to be the y-dimension length, in other words its width, of the node we are taking into account, being the region in which the calculation of W_{node} is considered valid. Please note that the geometrical correction factor of the source power is the pixel pitch p, since the validity of the integral is over the entire pixel pitch. This correction is applied for both nodes so Parasitic Light Sensitivity will finally result as:

$$PLS = \frac{w_{SN}}{w_{PD}} \frac{\iint G_{abs} \cdot W_{SN} \cdot dxdz}{\iint G_{abs} \cdot W_{PD} \cdot dxdz} \tag{2.58}$$

It is evident that this consideration is an approximation of the real 3D conditions, since the 2D Collection Probability weighting function does not take into account the contribution given by charges flowing along the third non-considered dimension.

2.7 Conclusion

Understanding and modeling of the output degradation due to the Parasitic Light Sensitivity issue is crucial to improve the performances of Global Shutter CMOS Image Sensors. The Parasitic Light Sensitivity issue appears because the shielding of the Storage Node to photo-generated charges is not perfect, thus leading to a non-negligible light sensitivity of the Storage Node. There are two main phenomena that contribute to increase the Storage Node light sensitivity: the direct collection of photons and the collection of free diffusing charges.

Direct collection of photon consists in photons able to reach the silicon surface at the region in which the Storage Node is found; direct light shielding is not perfect due to two main factors: light multiple reflections and light diffraction. The latter, becomes increasingly important when dealing with small dimensions pixels, since diffraction strongly depends on feature sizes with which light interacts. Common available light propagation methods like ray-tracing are able to model accurately light reflection, refraction and interference, though if diffraction has to be taken into account, FDTD simulations are better suited.

Collection of free diffusing charges happen because some photons, penetrating deep into the neutral region of the silicon epitaxial layer, generate electron-hole pairs that are not straightforward guided by an electric field. It is important to model photo-generated charges propagation inside the silicon epitaxial layer to understand the preferred paths that lead charges toward the Storage Node. Given the high carriers diffusion length in silicon (for an doping concentration of $10^{15}\,\mathrm{cm}^{-3}$ it can get to $50\,\mu\mathrm{m}$), two methods have been developed to create a collection probability mapping function to understand the probability that one charge has to reach a certain region; the first method consists in the application of the single particle Boltzmann Transport Equation, given a simplified electric field distribution; the second method consists in modeling the charges propagation as a straight line, reconsidering the potential barriers and the collection through electric field. Given the similar results shown by the two modeling methods, use of the Straight Line model is preferable, given its lower simulation time requirements compared to the Boltzmann Transport Equation model.

The two methods have been compared to more accurate TCAD simulations to give an understanding of the behavior of the model. It has been shown that the two methods differ in the absolute value from TCAD simulations at long wavelengths, though keeping a similar behavior. On the other hand, the methods and the TCAD show equivalent results at shorter wavelengths. The “jump” in the TCAD simulations at $\lambda = 600\,\mathrm{nm}$ is still to be explained. This could suggest a use of the newly developed models to compare different pixel structures or even different light conditions.

Finally, geometrical correction for 3D approximation using 2D simulation has been given.

Chapter 3

Design optimization for Global Shutter CMOS Image Sensors

We have seen that the use of Global Shutter mode in CMOS Image Sensor is required if fast-moving objects are to be imaged, though Global Shutter CMOS Image Sensors performances are limited by the non-negligible sensitivity to light during the storage and readout phase; impinging light during this phase can cause artifacts on the resulting output image, hard to quantify.

With the aim in the improvement of Global Shutter CMOS Image Sensors performances, an understanding of the phenomena causing the non-negligible Parasitic Light Sensitivity is required. The previous chapter has been conceived with the aim in laying the foundations for an understanding of the underlying phenomena causing the non-negligible Parasitic Light Sensitivity of the image sensor, thus allowing for the development of a simple and effective modeling method. In a cost-effective way, targeted Global Shutter Efficiency performances improvement in Global Shutter CMOS Image Sensors could be sought through an accurate analysis of critical areas, element sizing and positioning. Usage of the model presented in chapter 2 allows for a profound analysis of the image sensor critical areas as well as a rapid comparison between different pixel designs.

The developed model can serve as a basis for determining design guidelines for pixel optimization and Global Shutter Efficiency improvement with a given technological process. Shielding metal layers positioning, PhotoDiode and Storage Node sizing as well as micro-lens positioning may play a fundamental role in the image sensor response to the parasitic light. Aim of this chapter is therefore to exploit the developed model to analyze the impact of design parameters on the image sensor Global Shutter Efficiency performances.

3.1 Introduction on the use of the model for pixel analysis

The Parasitic Light Sensitivity modeling method has been developed through the use of two different components, the optical propagation of light inside the pixel structure and the propagation of photo-generated charges in the silicon epitaxial layer. The assumptions of independence given in the modeling allows for both individual and combined analysis of the two phenomena, giving an additional perspective to the image sensor analysis.

At the beginning of this chapter, we will use the combination between the optical and the transport problem to get an insight on the pixel light response. Consecutively, we will focus on the optical propagation of light inside the pixel, thus analyzing the critical issues related to light interacting with the Back-End Of Line (BEOL) elements of CMOS fabrication. Finally, we will focus on the Front-End Of Line (FEOL) of CMOS fabrication, giving a closer look to how the different doping layers may impact the propagation of free photo-generated charges.

3.1.1 Quantum Efficiency calculations

As a reminder, Quantum Efficiency determines the number of photo-generated electrons that are being collected by a node with respect to the total number of photons impinging onto the pixel. It has to be recalled that the Parasitic Light Sensitivity is a figure of merit defined as the ratio between the light sensitivity of two nodes: the node on which the information has to be stored (the Storage Node in our case), and the node responsible for direct collection of light (the PhotoDiode in our case). In other words, Parasitic Light Sensitivity can be defined as the ratio between the Storage Node and the PhotoDiode Quantum Efficiency. As we have understood that light sensitivity of the node and its Quantum Efficiency differ by just a multiplicative constant, we will indistinctly use light sensitivity and Quantum Efficiency as two sides of the same coin.

A closer look to the nodes' light sensitivities is crucial for the understanding of the phenomenon of Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors; notably, being the Parasitic Light Sensitivity calculated as a ratio, both nodes' light sensitivities have to be taken into account if a targeted improvement of the image sensor is required.

Given so, let us quantify the impact that the nodes' sensitivities have on Parasitic Light Sensitivity. For our purposes, the usage of the inverse of the Parasitic Light Sensitivity, "Parasitic Light Hardness (1/PLS)" comes in handy to describe improvements of the image sensor with respect to its Global Shutter Efficiency; in other words, if Parasitic Light Hardness (1/PLS) increases, the performances of a Global Shutter CMOS Image Sensors in suppressing the parasitic light increase. Recalling the definition given in chapter 1 in the logarithmic form, it follows:

$$1/PLS = 20 \cdot \log_{10}\left(\frac{QE_{PD}}{QE_{SN}}\right).$$

It is easy to appreciate that a higher PhotoDiode Quantum Efficiency leads to an increase in the Parasitic Light Hardness (1/PLS), as well as a decrease in the Storage Node Quantum Efficiency similarly leads to an increase in the Parasitic Light Hardness (1/PLS). We would like to further evaluate the increase in the Parasitic Light Hardness (1/PLS) as function of both PhotoDiode and Storage Node Quantum Efficiency. Given a reference pixel with reference values of PhotoDiode and Storage Node Quantum Efficiency (QE_{PD} and QE_{SN}), we define *pp* as the increase with respect to the reference Quantum Efficiency. Two cases can therefore be analyzed:

- **Case 1** The PhotoDiode Quantum Efficiency is increased of a certain amount $QE_{PD,new} =$

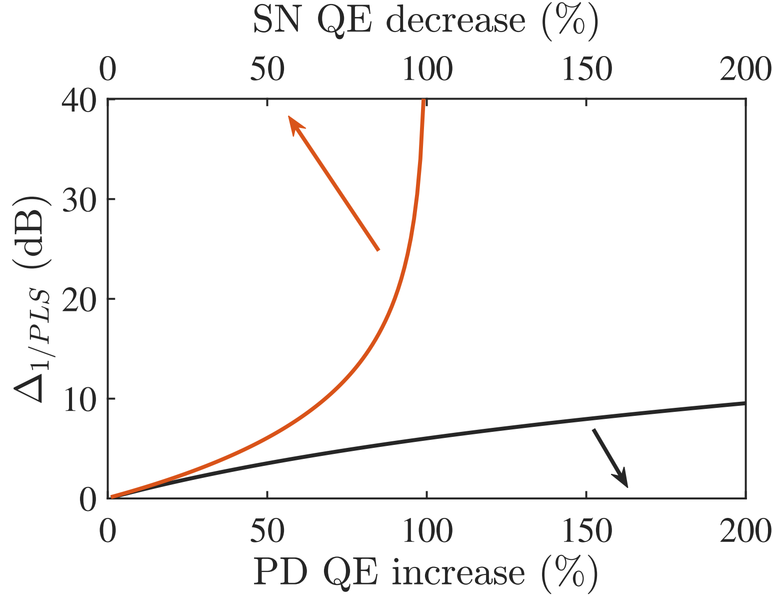


Figure 3.1: Parasitic Light Hardness (1/PLS) improvement as function of two cases: (1) in black the increase in the PhotoDiode Quantum Efficiency and (2) in red the decrease in the Storage Node Quantum Efficiency.

$QE_{PD} \cdot (1 + pp)$ and the Storage Node Quantum Efficiency is kept constant;

- **Case 2** The Storage Node Quantum Efficiency is decreased of a certain amount $QE_{SN,new} = QE_{SN} \cdot (1 - pp)$ and the PhotoDiode Quantum Efficiency is kept constant.

It has to be noted though that the following conditions must apply in order to consider separately the two cases:

- **Case 1** $\quad QE_{PD} \cdot (1 + pp) \leq 1 - QE_{SN}$
- **Case 2** $\quad QE_{SN} \cdot (1 - pp) \geq 0 \;\Rightarrow\; pp \leq 1$

Thanks to the logarithmic properties, we can define the Parasitic Light Hardness (1/PLS) increase ($\Delta_{1/PLS}$) in the two cases as follows:

- **Case 1** $\quad \Delta_{1/PLS} = 20 \cdot \log_{10}(1 + pp)$
- **Case 2** $\quad \Delta_{1/PLS} = -20 \cdot \log_{10}(1 - pp)$

The improvements in the two cases are described in Fig. 3.1 where the black curve represents “Case 1”, the red curve represents “Case 2”. In “Case 1” the curve gently increases as function of the PhotoDiode Quantum Efficiency increase. On the other hand the red curve of “Case 2” rapidly increases as function of the Storage Node Quantum Efficiency; an

exponential behavior in the Parasitic Light Hardness (1/PLS) increase can be appreciated, notably the performances improve when the Storage Node Quantum Efficiency is reduced by more than its half. Moreover, the red curve goes to infinite when the Storage Node Quantum Efficiency reduction reaches the 100%, denoting perfect shielding to the parasitic light. We will focus on the reduction of the Storage Node Quantum Efficiency to achieve improvement of the Global Shutter Efficiency performances, having a stronger impact in its improvement.

This simple investigation allows us to understand the importance of the analysis on the nodes' Quantum Efficiency to improve the Global Shutter performances to suppress Parasitic Light Sensitivity. It has been shown that a reduction of the Storage Node Quantum Efficiency has to be targeted to improve the Global Shutter performances; as an alternative, improvements on the PhotoDiode Quantum Efficiency can also help achieve better Global Shutter performances.

Nevertheless, the model can be adapted to allow calculation of both PhotoDiode and Storage Node Quantum Efficiencies, seeking to the reduction in the latter for Global Shutter Efficiency performances improvements. Model adaptation is done through the use of the incoming light source power which is given by the simulator, previously presented by Eq. (2.55) and briefly recalled as follows:

$$QE_{node} = \frac{\iiint G_{abs} \cdot W_{node} \cdot dV}{\iint \Re\{\vec{S}_{source}\} \cdot d\Sigma}$$

where G_{abs} is the photo-generation of charges per units of time and surface computed thanks to the use of the Lumerical software, W_{node} is the weighting function associated to the Collection Probability of the node, determining the probability that the desired node collects a charge photo-generated at a point in space, $\vec{S}_{source}$ is the Plane Wave source Poynting vector with which the FDTD simulation has been performed, V is the pixel volume and Σ is the surface parallel to the Si/SiO_2 interface, being equal to the the pixel pitch square.

As it will be seen further on, some improvements in the Global Shutter Efficiency performances of the image sensor may lead to a reduction in the PhotoDiode Quantum Efficiency, thus lowering the image sensor sensitivity: a *trade-off* has to be made between the image sensor Parasitic Light Sensitivity and sensitivity. The presented models therefore allows for a direct analysis on both Parasitic Light Sensitivity and PhotoDiode Quantum Efficiency, thanks to the fact that the model has been developed using the Quantum Efficiency calculations as building blocks.

3.1.2 Investigation of the optical response

We have seen that an important reduction in the Storage Node Quantum Efficiency is highly desired to improve the Global Shutter Efficiency performances of a Global Shutter CMOS Image Sensors. Following the main idea of the developed model, achievement of Storage Node Quantum Efficiency reduction depend on the capability of the structure to: 1) reduce the number of direct incoming photons onto the Storage Node area and 2) reduce the collection

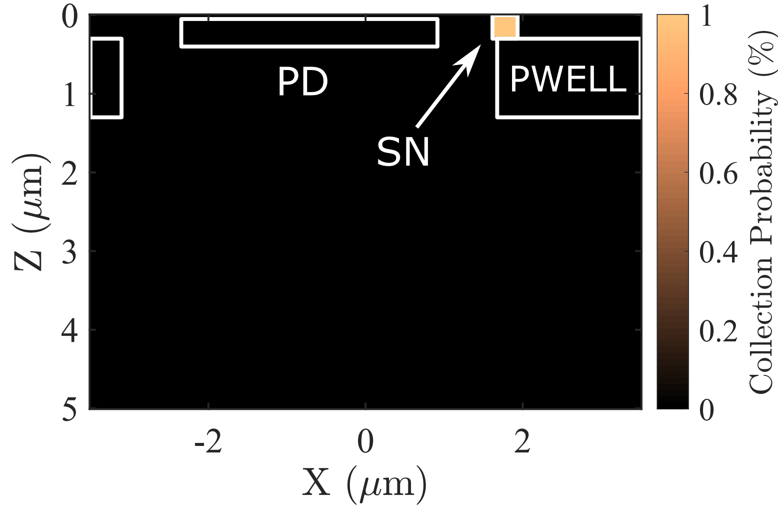


Figure 3.2: Collection Probability weighting function for direct light collection in the Storage Node region. The orange represents the region in which the spatial weighting would value 1; the dark region values 0.

free-roaming photo-generated charges. While for the first case it is sufficient to take into account the number of direct impinging photons onto the Si/SiO_2 interface in the Storage Node area and its surroundings, the second case requires a deeper analysis, since both Collection Probability and charges photo-generation density have to be taken into account. For this subsection, we will focus on case number 1 and how the model can be exploited on this purpose.

In order to improve the understanding on the amount of photo-generated charges in the Storage Node region leading to Parasitic Light Sensitivity, it is sufficient to directly analyze the FDTD simulation results. Giving the photo-generation of charges G_{abs} per units of time and space, it is possible to compute the total number of photo-generated charges in the Storage Node, N_{SN}, as follows:

$$N_{SN} = \int_{x_{SN,in}}^{x_{SN,max}} \int_{y_{SN,min}}^{y_{SN,max}} \int_{0}^{z_{SN}} G_{abs} \cdot dV \tag{3.1}$$

where $x_{SN,min}$ and $x_{SN,max}$ represent respectively the minimum and the maximum boundaries of the Storage Node region in the $\hat{x}$ direction, $y_{SN,min}$ and $y_{SN,max}$ represent respectively the minimum and the maximum boundaries of the Storage Node region in the $\hat{y}$ direction and z_{SN} represents the depth extension of the Storage Node region in the $\hat{z}$ direction, given the hypothesis of the Storage Node region being a rectangular cuboid. Therefore, differently from the Quantum Efficiency calculations, no weighting function is present. It is possible to transform Eq. (3.1) in a similar form to the one given in (2.32) introducing a weighting

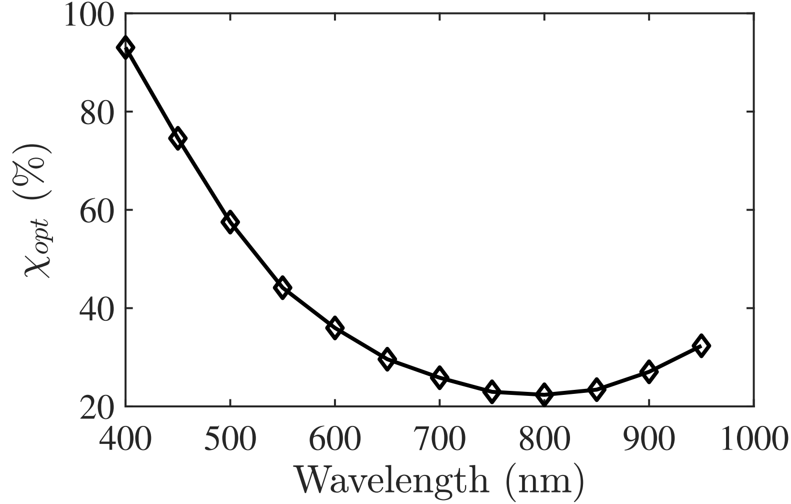


Figure 3.3: Fraction of direct light collection, χ_{opt} over the global Storage Node light sensitivity as function of wavelength.

function $W_{SN,opt}$ which is described as follows:

$$W_{SN,opt} = \begin{cases} 1, & \textit{if } P(x,y,z) \in SN\, region \\ 0, & \textit{otherwise.} \end{cases} \tag{3.2}$$

Therefore, the analysis of direct impinging light generating charges inside the Storage Node region can be carried on exploiting the model through a slight modification of the Collection Probability; the weighting function does not require time-consuming calculations since no transport simulations are required.

In a similar manner, the contribution of direct impinging light generating charges in the PhotoDiode region can be calculated, with a similar modification of the weighting function. Fig. 3.2 is a visual example of the weighting function $W_{SN,opt}$, as represented by Eq. 3.2, that is used to study direct light impact on the Storage Node. The orange part represents the value where the weighting function is worth one, while the black area represent the null value. In order to retrieve the only-optical Quantum Efficiency of the node, the convolution of the only-optical weighting function map and the optical generation map is required.

Let us try to understand the contribution of the direct light collection on the entire Storage Node light sensitivity; with this purpose in mind, we give the following parameter:

$$\chi_{opt}\,[\%] = \frac{\iiint G_{abs} \cdot W_{SN,opt} \cdot dV}{\iiint G_{abs} \cdot W_{SN} \cdot dV} \times 100 \tag{3.3}$$

which describes the fraction of direct light contribution on the total Storage Node light sen-

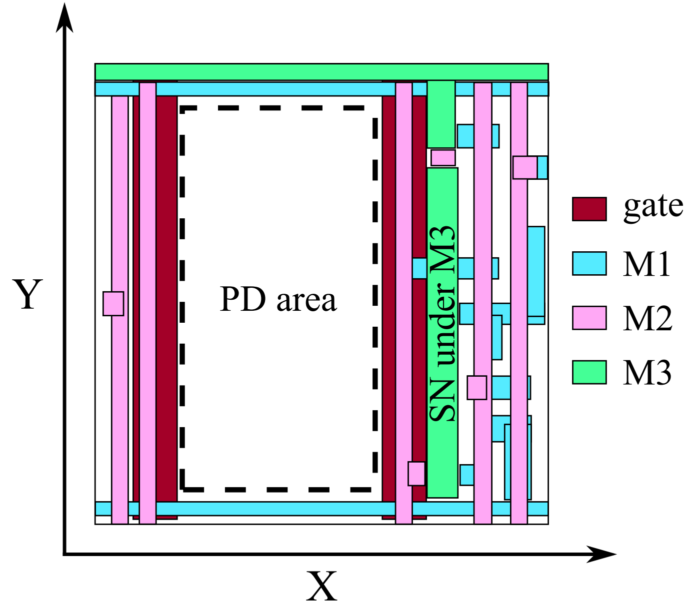


Figure 3.4: Layout example of the real pixel modeled in FDTD simulations. The cyan lines represent M1, the closest to the Si/SiO$_2$ interface. The magenta lines represent M2. The green lines represent M3. The poly-silicon gates are represented in dark red. Location of PhotoDiode and Storage Node are noted as well.

sitivity. In Fig. 3.3 it is possible to appreciate the fraction of direct light contribution on the total Storage Node light sensitivity, as function of wavelength, given the pixel layout in Fig. 3.4. Worth of notice, the simulated pixel structure has been modeled on the basis of a CMOS Image Sensor able to operate in the Global Shutter mode developed by the ISAE-SUPAERO team. This allows modeling of the light propagation in an actual pixel structure. Direct light contribution is high at short wavelengths and decreases going towards longer wavelengths; this can be easily understood since the photo-charge generation at short wavelength is shallow, while longer wavelengths generate charges deeper in the epitaxial layer. Nevertheless, χ_{opt} increases for $\lambda \geq 800$ nm. Charges initial energy is small, due to the smaller associated photon energy in this wavelength region; the PWELL barrier is more efficient in screening charges with low energy, as shown in Fig. 2.17. Therefore, the number of charges reaching the Storage Node by diffusion is reduced, thus resulting in an increase of the optical contribution in percentage.

This last result shows the dualistic behavior of Parasitic Light Sensitivity, where direct impinging light has a higher impact at shorter wavelengths, while charge transport becomes increasingly important at longer wavelengths. Moreover, the importance of direct light collection despite the shielding of the Storage Node proves the relevance of the diffraction phenomenon on the non-negligible light sensitivity of the Storage Node. Nevertheless, a purely optical analysis of a Global Shutter CMOS Image Sensors is not sufficient to fully understand and model its Parasitic Light Sensitivity; charge transport simulations coupled with the optical ones are therefore mandatory.

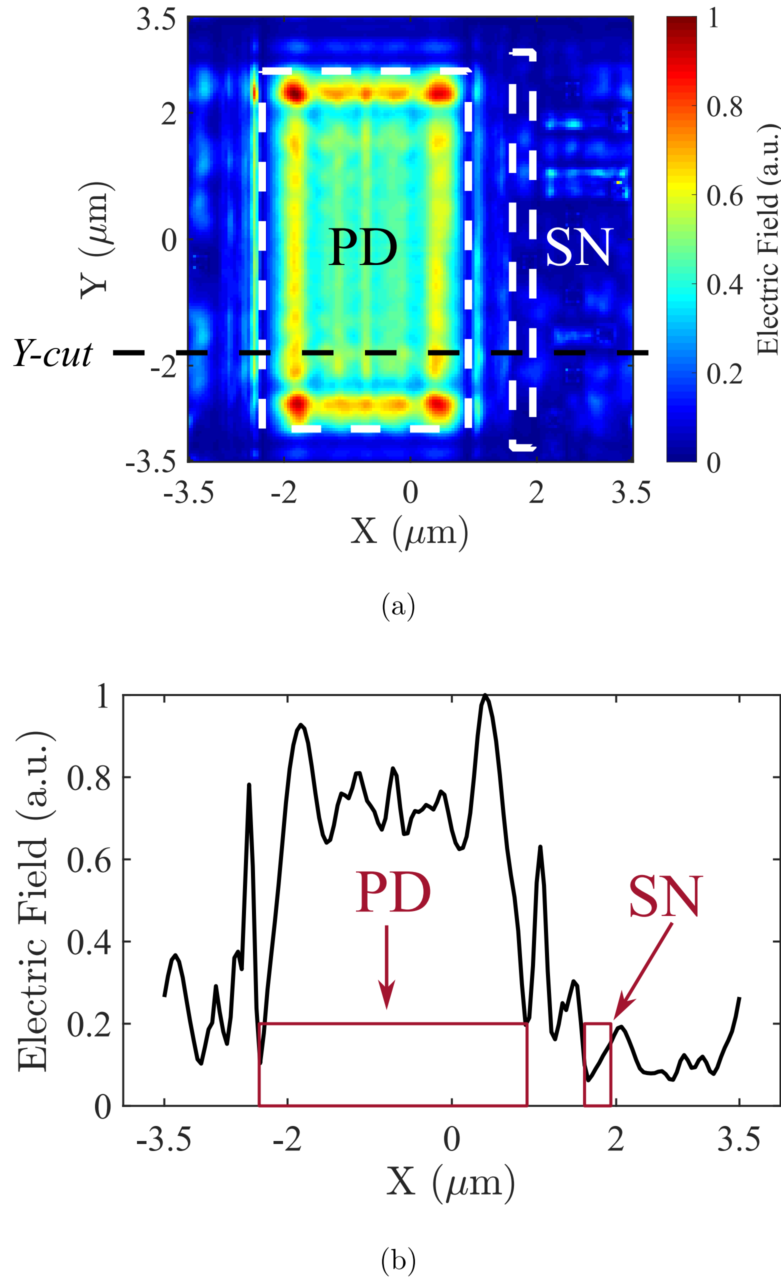


Figure 3.5: (a) 2D cartography for simulated electric field of a real pixel structure (which layout from the top view is shown in 3.4) taken at the Si/SiO_2 interface. The simulation has been performed for a wavelength of $\lambda = 650\,\text{nm}$. (b) relative 1D *Y-cut* electric field distribution. The red rectangles indicate the regions where PhotoDiode and Storage Node are found.

One last investigation can be carried on the amount of photons impinging onto the Si/SiO_2 interface, which is directly related to the charges photo-generation. Charges photo-generation is also related to the square of the electric field, as given by Eq. (2.23). This latter can be

exploited to visually understand the diffraction phenomenon, as it has been shown in chapter 1 that electric field diffraction patterns appear when a beam of light encounters an object which dimensions are comparable to the impinging wavelength. This leads to electric field extension behind the light shielding layers, thus having a impact on direct illumination of the Storage Node region.

The FDTD software allows to get the result of the electric field distribution per every point in space, thus allowing for an analysis of the electric field propagation inside the pixel structure. For our purposes, we will just focus on the electric field distribution at the Si/SiO_2 interface since our interest lies in the inquire of the field magnitude close to the Storage Node region.

Fig. 3.5 shows an example of the 2D electric field distribution at the Si/SiO_2 interface induced by non-polarized impinging lightwave at $\lambda = 650\,\mathrm{nm}$, for the pixel layout presented in Fig. 3.4. Differently from what expected, no uniform electric field distribution can be appreciated in areas where light does not encounter any obstacles (the dashed “PD” region); this is due to the diffraction patterns that build up when light propagates in structures where feature dimensions are comparable to light wavelength.

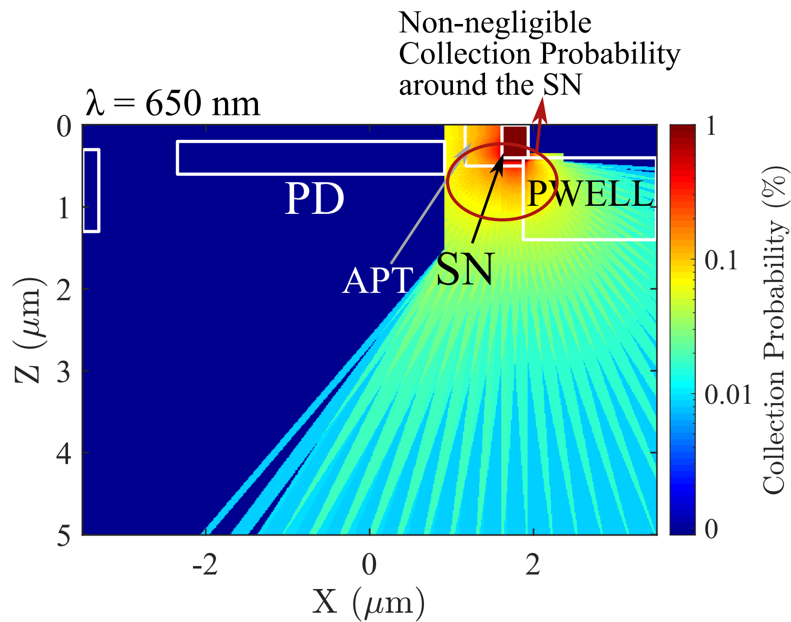
In order to better observe the electric field pattern, let us depict the electric field distribution along the *Y-cut* line, presented in Fig. 3.5b. The figure clearly shows how there is non-negligible electric field intensity above and close to the Storage Node region even though a light shield impeding normal impinging photons has been designed on top of the Storage Node region. This result once more shows the importance in using a method for taking into account light diffraction to model the Global Shutter Efficiency performances in Global Shutter CMOS Image Sensors.

3.1.3 Critical areas analysis

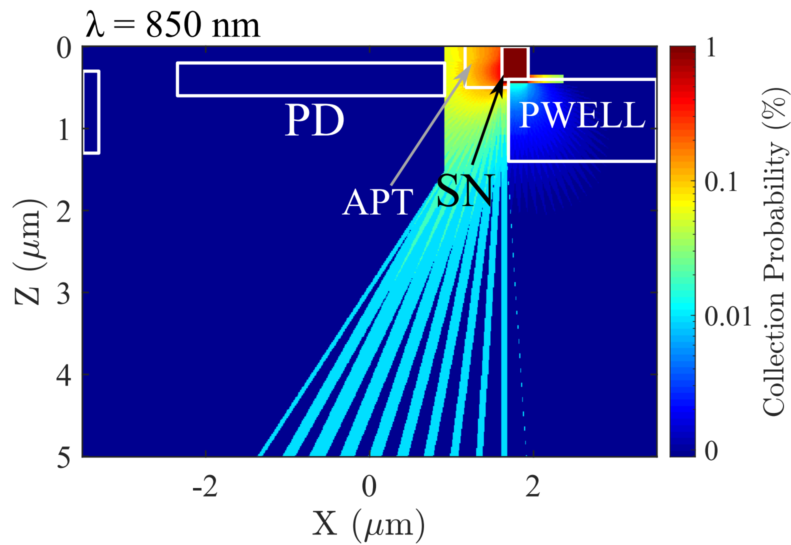
Once investigated the contribution that the developed model can give when considering only the direct impinging photon collection on the Global Shutter Efficiency performances in Global Shutter CMOS Image Sensors, the following step consists in exploiting the developed model to evaluate the impact of the different doping regions on the parasitic free-roaming charge collection.

It has to be reminded that the model has been built given the hypothesis of independence between the optical generation of charges and their transport; the hypothesis allows to evaluate the impact that a given pixel structure would have on the probability to collect parasitic diffusing charges independently from their photo-generation distribution.

The Collection Probability weighting function can be exploited as a visual tool for understanding the possible flow of diffusing charges; when focusing on Storage Node sensitivity reduction and thus in lowering the number of diffusing charges attaining the Storage Node region, the visual tool can be exploited to investigate the main path that the charges may follow to reach the Storage Node region, thus allowing for an improvement in the development



(a)



(b)

Figure 3.6: Collection Probability weighting function of the Storage Node in logarithmic scale, built through exploitation of the Straight Line model at a wavelength of (a) $\lambda = 650\,\text{nm}$ and (b) $\lambda = 850\,\text{nm}$. The critical areas, where photo-generated charges could diffuse or drift and attain the Storage Node region is shown with the red circle in (a) $\lambda = 650\,\text{nm}$. A wide area of possible charges collection can also be appreciated under the PWELL region. In (b) the PWELL is more efficient to shield diffusing charges due to their lower initial energy (given by the light impinging wavelength).

of diffusion barriers or in understanding the targeting zone for main charges photo-generation. In order to give an example of how the visual tool can be exploited, let us take a look at the Storage Node Collection Probability weighting function in Fig. 3.6a at a wavelength of $\lambda = 650\,\text{nm}$. Please note that the color scale is logarithmic to better appreciate the differences at smaller probabilities. There are few critical areas surrounding the Storage Node region for the modeled structure, as marked on the figure. Moreover, charges may diffuse from the deep epitaxial layer passing through the PWELL or Anti Punch-Through barriers. With the knowledge of the critical Parasitic Light Sensitivity areas, the designer would be able to accurately design the shielding layers or improve PhotoDiode light collection through different means (we will see further on how it would be possible to use a micro-lens to do so).

Shielding the Storage Node from diffusing charges by the PWELL is appreciable at $\lambda = 850\,\text{nm}$ as shown in Fig. 3.6b. At longer wavelengths, the photo-generated carriers have low initial energy, thus not sufficient to overcome the PWELL barrier (as shown in chapter 2 in Fig. 2.17). Doping barriers, like the PWELL and the Anti Punch-Through, are therefore not perfectly suited for charge shielding given the weak electric field magnitude generated by the graded doping concentration. This is especially true for charges generated from light impinging in the visible wavelength rang. Conversely, graded doping barriers may result effective for charge shielding for NIR applications given the lower generated charge energy. Increasing the doping concentrations of these layers is not often feasible, therefore an alternative solution has to be sought. Creation of an electric field in the neutral zones to drive charges away from the Storage Node may be a viable possibility, as seen in [Lah+17] exploiting different implants and high resistivity epitaxial layer. Nevertheless, this possibility has not been analyzed in our simulations.

Nevertheless, the presented analysis exploiting the Collection Probability weighting function as a visual tool to evaluate the critical path that diffusing parasitic charges follow can be exploited for different type of Global Shutter CMOS Image Sensors, since it can be adapted for taking into account different type of Storage Node, as for example the Storage Gate [Kry15] or a pinned diffusion [Kaw+16]. It has been shown how the model can be operated as a visual tool to locate the critical areas that can cause weak Global Shutter Efficiency performances, as well as a quantitative tool allowing to calculate the response of the simulated structure in terms of both nodes' sensitivities and Parasitic Light Sensitivity. Notably, it has been shown how a quantitative analysis of nodes' sensitivity becomes crucial in allowing for the improvement in Global Shutter Efficiency performances.

The tool has been conceived as a steady-state transfer function, the optical and the charge transport one, of the pixel structure, thus allowing to model different pixel structures in a fast and efficient way. The two steady-state transfer functions are highly dependent on pixel design, whether mainly on the BEOL elements (as for example the metal interconnections, VIAs, Anti-Reflection (AR) coatings, micro-lenses, ...) as the optical one, or on the FEOL elements (as for example the positioning, the dimensions and the presence of the different doping layers like the PhotoDiode, the Storage Node, the PWELL, the Anti Punch-Through, ...) as the charge transport one. The developed model encourages comparative analysis between different pixel designs in order to find the optimal solution to improve Global Shutter

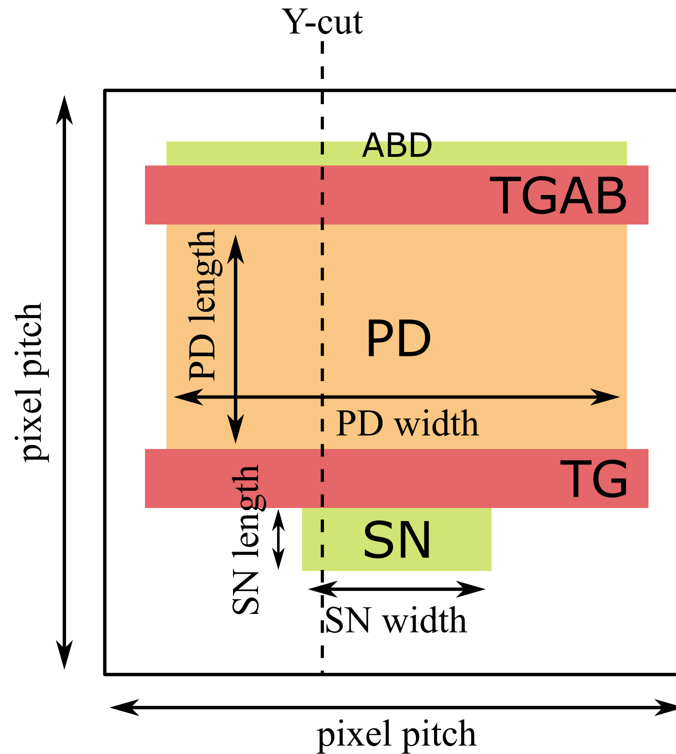


Figure 3.7: Pixel top-view schematic with description of PhotoDiode and Storage Node dimensions. For a better understanding, the RST, SF and SELY transistors have not been shown, while the TG and TGAB as well as the ABD are present.

Efficiency performances in Global Shutter CMOS Image Sensors in an cost-effective way. In this regards, the user is allowed to a good degree of freedom to change some key parameters, as for example the doping concentrations or the shielding metal layer material and positioning.

3.2 Storage Node dimensions optimization

Let us now focus on the transport transfer function and analyze the impact that the Storage Node sizing has on Global Shutter Efficiency performances of Global Shutter CMOS Image Sensors. It has to be kept in mind that we suppose using a 5T technology in which the role of the Storage Node is taken by the Floating Diffusion; distance between the Floating Diffusion and the PhotoDiode is fixed and given by the technological process and cannot be modified. We will therefore consider only the Storage Node length and width impact on Global Shutter Efficiency performances.

3.2.1 The geometrical correction factor in 2D simulations

Fig. 3.7 gives a definition of the nodes' *width* and *length*, where a line (noted as *Y-cut*) that passes through both PhotoDiode and Storage Node is traced. We define *width* as the dimension perpendicular to the line and *length* as the dimension parallel to the line. Let us first focus on the geometry correction factor.

As previously presented in Sec. 2.6, we are only performing 2D simulations. 2D simulations are taken along the *Y-cut* line and therefore a geometrical correction factor is needed in order to take into account the missing 3rd dimension, which has been determined as the node's width. Recalling formulation given in Eq. (2.57), the node's light sensitivity is linearly dependent on the node's width and can be formulated as follows:

$$QE_{PD} = \frac{y_{PD}}{p} \cdot QE_{PD,2D} \tag{3.4}$$

$$QE_{SN} = \frac{y_{SN}}{p} \cdot QE_{SN,2D} \tag{3.5}$$

where y_{PD} and y_{SN} are respectively the PhotoDiode and Storage Node width, p is the pixel pitch and $QE_{PD,2D}$ and $QE_{SN,2D}$ are the PhotoDiode and Storage Node light sensitivity computed from 2D simulations. Increasing the PhotoDiode (or Storage Node) width would therefore linearly increase the PhotoDiode (or Storage Node) light sensitivity.

Remembering that, if improvement of the Global Shutter Efficiency performances is required, the Storage Node light sensitivity should be made as smaller as possible. It is worth of notice that the smallest Storage Node width is determined by the chosen technological process (as an example, the 0.18 µm CMOS image sensor process that has been used to develop test structures, to be presented further on, the minimum Storage Node width is 0.32 µm). Nevertheless, it has to be kept in mind that resizing of the Storage Node in a 5T pixel has an important impact on pixel performances, resulting in a reduction of the Storage Node capacity thus leading to higher conversion gain and higher kTC noise, which have to be carefully taken into account.

It has been shown that the PhotoDiode contributes as well to determine the Global Shutter Efficiency performances. PhotoDiode are often designed as big as possible in order to improve the overall CMOS Image Sensor performances (Dynamic Range, light sensitivity, etc.) and this goes in the same direction of Global Shutter Efficiency performances improvement.

3.2.2 Length and width impact on Parasitic Light Sensitivity

We would like now to analyze the impact that a node's length has on its light sensitivity performances. Differently from what previously presented in the case of a node's width, this cannot be done by a multiplicative factor, since the node's length is an important parameter during the calculation of the transport transfer function.

A study has been conducted to analyze the impact of the Storage Node length on the

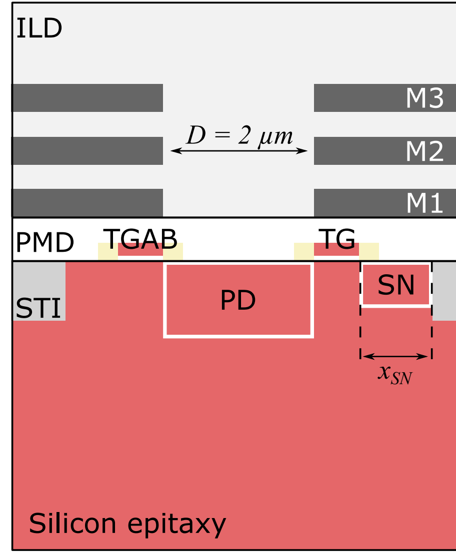


Figure 3.8: Schematic of the FDTD simulated pixel to test the impact of the Storage Node length on the Parasitic Light Sensitivity. The slit dimension D is constant, as well as other dimensions in the structure. The Storage Node length is denoted as x_{SN}. The right-hand STI dimensions vary accordingly to the Storage Node length.

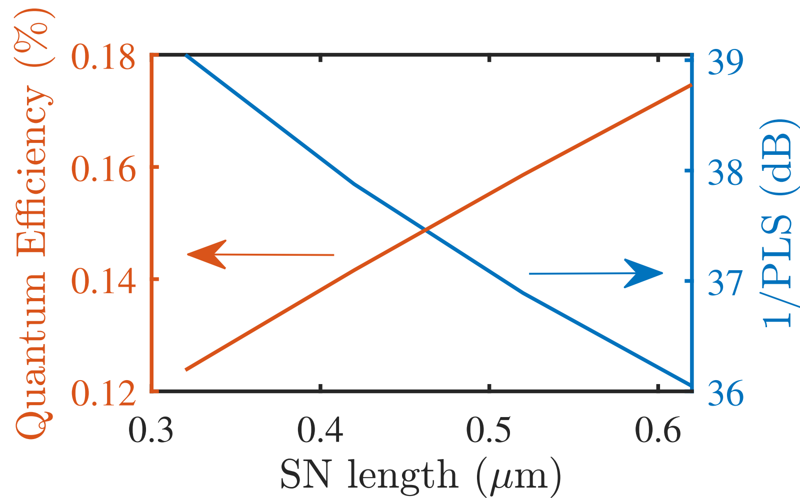


Figure 3.9: Quantum Efficiency (red curve) and Parasitic Light Hardness (1/PLS) (blue curve) simulation results as function of the Storage Node dimensions for $\lambda = 650\,\text{nm}$.

Storage Node light sensitivity as well as on the Parasitic Light Hardness (1/PLS) of the simulated pixel. Simulations, exploiting the Straight Line model, have been performed on a simple 5T pixel structure, as presented in Fig. 3.8 showing the pixel structure modeled

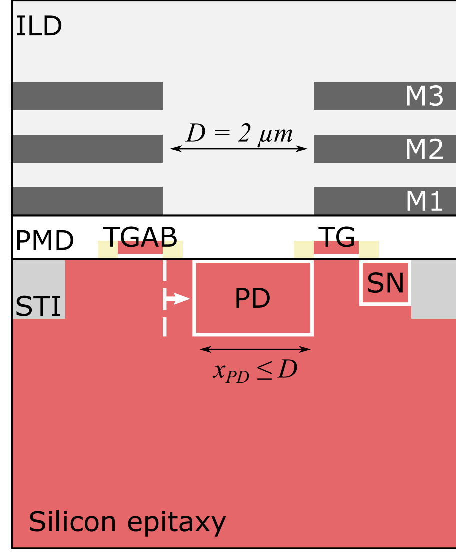


Figure 3.10: Schematic of the FDTD simulated pixel to test the impact of the PhotoDiode length on the Parasitic Light Sensitivity. The slit dimension D is constant. The PhotoDiode length, denoted as x_{PD} varies from one simulation to another. Distance between one end of the PhotoDiode and the other end of the Storage Node are kept constant, as given by technological rules.

in the FDTD simulations. The epitaxial silicon layer sits on the bottom of the structure; Shallow Trench Isolation (STI) are carved into the silicon epitaxyal layer, which is exploited for separating the pixel active layers. All main pixel elements lie inside the active region, being the region where no STI is present; the PhotoDiode sits at the center of the epitaxial layer, the Storage Node sits on the right of the PhotoDiode. Between the PhotoDiode and the Storage Node and right above, the TG structure is shown, consisting of a SiO_2 gate oxide, a poly-silicon TG and nitride spacers. Specularly, the ABD sits on the left of the PhotoDiode and, right above and between them, the TGAB is shown, similarly consisting of a SiO_2 gate oxide, a poly-silicon TG and nitride spacers. The two gates are submersed in the Pre-Metal Dielectric. Right above the Pre-Metal Dielectric layer sits the Inter-Layer Dieletric layer, in which the different metal layers are submersed. As previously said, M1 is the level closer to the Si/SiO_2 interface, M3 is the furthest lever from the Si/SiO_2 interface and M2 sits between them. The Storage Node length is noted as: x_{SN}.The STI on the right-hand side is in contact with the Storage Node region and thus its dimensions reduced with the increase in the Storage Node length.

Fig. 3.9 shows the evolution in the Storage Node light sensitivity as function of the node's length. In a similar way, it is possible to compute the Parasitic Light Hardness (1/PLS) of the pixel structure as function of the Storage Node length, when the PhotoDiode dimensions are kept constant. Results clearly show a deterioration in the Parasitic Light Hardness (1/PLS) as the Storage Node light sensitivity increases with the increase in the Storage Node length.

In a similar manner, another study has been conducted to analyze the impact of the

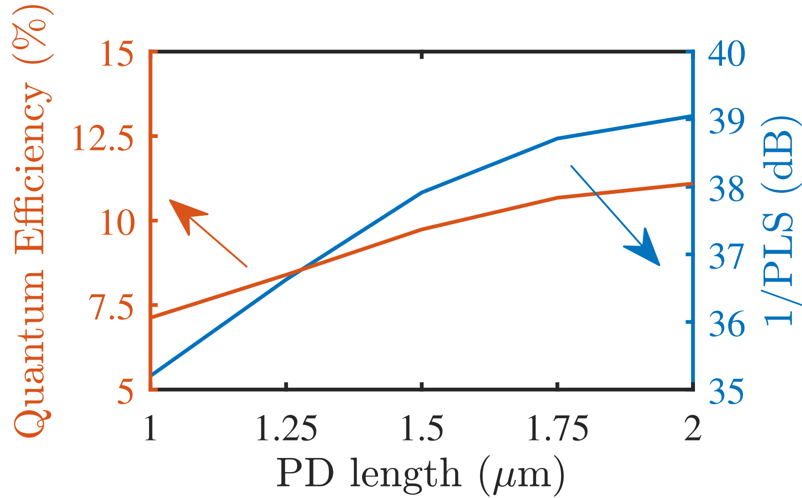


Figure 3.11: Quantum Efficiency (red curve) and Parasitic Light Hardness (1/PLS) (blue curve) simulation results as function of the PhotoDiode dimensions for $\lambda = 650\,\text{nm}$.

PhotoDiode length on the PhotoDiode light sensitivity as well as on the Parasitic Light Hardness (1/PLS) of the simulated pixel. Simulations have been performed on a simple 5T pixel structure, as presented in Fig. 3.10. The PhotoDiode length, denoted as x_{PD} is varied and the TGAB is moved towards the right-hand side accordingly. Distance between the PhotoDiode and the Storage Node is again kept constant. Fig. 3.11 shows the evolution in the PhotoDiode light sensitivity as well as the evolution in the Parasitic Light Hardness (1/PLS) of the pixel structure as function of the PhotoDiode length, when the Storage Node dimensions are kept constant. Differently from what shown for the Storage Node case, an increase in the PhotoDiode length helps in the improvement of the image sensor Parasitic Light Hardness (1/PLS).

Nodes dimensions play a fundamental role in the Global Shutter Efficiency performance of the image sensor. As a rule of thumb, the pixel should be conceived in order to build the biggest PhotoDiode possible and the smallest Storage Node possible.

3.3 Use of BEOL metal layers for light shielding

We have so far analyzed the impact of the design of FEOL elements in 5T Global Shutter CMOS Image Sensors. In a similar manner, the proposed model allows analyzing the impact of BEOL elements design on the pixel performances. As previously described, the BEOL elements only come into the modeling of the steady-state optical response of the pixel structure. This means that, when a parametric analysis on BEOL elements has to be performed without any change in the FEOL design, there will be no need in re-computing the steady-

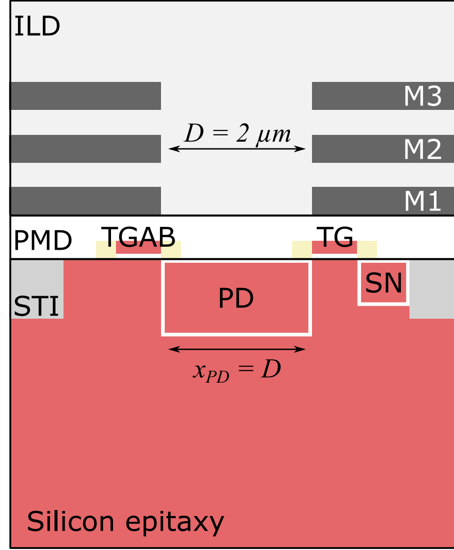


Figure 3.12: Schematic of the FDTD simulated pixel. The slit dimension D is constant and it corresponds to x_{PD}, being the PhotoDiode length. “M1”, “M2” and “M3” are represented in the schematic, though they may not be present for every simulation. If not present, the metal layer is replaced by the Inter-Layer Dieletric (ILD).

state transport function, since it will be valid for the entire parametric analysis. In other words, the criteria that has been presented in chapter 2 allows exploiting one steady-state transport function in combination with different steady-state optical responses since the two phenomena are considered independent.

The aim in using the BEOL for improving the Global Shutter Efficiency performances mainly lies on the understanding of light shielding with the use of metal interconnection layers, through the complete modeling of light propagation inside the pixel structure exploiting FDTD simulation. A commercial CMOS Image Sensor technological process has been selected, having four metal interconnection levels. Only three metal levels will be exploited, denoted as *M1, M2, M3*. Each metal level has a defined distance from the Si/SiO_2 interface as well as a defined thickness. The lower metal level, M1, represents the closest level to the Si/SiO_2 interface; as the metal level increase, so does the distance from the Si/SiO_2 interface.

Metal interconnection layers can be exploited for light shielding purposes through use of two main degrees of freedom: the height positioning of the metal layer (its distance from the Si/SiO_2 interface) and the x, y positioning (relating to the position of the metal layer with respect to the position of the Storage Node). In addition, different metal shielding layers can be used in combination, since technology allows to place two or more metal levels in a corresponding region. This increases the panel of possibilities for studying and improving the Global Shutter Efficiency performances in Global Shutter CMOS Image Sensors.

3.3.1 Choice of metal layers for shielding purposes

It has been shown in chapter 2 how the Storage Node shielding from direct impinging light using a metallic layer, designed and placed in correspondence of the Storage Node region, is far from being perfect; despite not being able to pass through the metallic shield, impinging light can nevertheless reach the Storage Node region through diffraction or multiple reflections.

In the chosen CMOS Image Sensor technological process, light shielding can only be performed through the use of metallic interconnections and each metal level is placed at a different distance with respect to the Si/SiO_2 interface. As previously shown by the Fresnel number theory, the electric field pattern produced on the Si/SiO_2 interface by the impinging light increasingly spreads beyond the light shield when the distance from the diffraction slit increases. In other words, there will be non-negligible light intensity due to diffraction in regions that are supposed to be in “dark”.

In principle, we would expect that metal layers found at a closer distance to the Si/SiO_2 interface are better suited to shield the Storage Node region from light, since light intensity spreads to a lesser extent on the Si/SiO_2 interface. On the contrary, light shielding of the Storage Node region only using the metal layer which is found at a higher distance from the Si/SiO_2 interface may result lesser suited. It is nevertheless possible to use a combination of metal levels to shield the Storage Node region from light. We would like to analyze the contribution given by different metal combinations to the Storage Node light shielding, and thus to Global Shutter Efficiency performances, as it cannot be predicted by simple Fresnel number theory.

Before getting into a detailed analysis of the impact of different metal shielding layers on the Storage Node light sensitivity as well as on the Global Shutter Efficiency performances, let us give a closer look the structure that has been exploited for our simulations, as shown in Fig. 3.12. The metal layers entirely cover the pixel, though leaving one single slit in correspondence of the PhotoDiode; the slit dimension is equal to the PhotoDiode length. Differently from what shown in the figure, not all three metal layers are always present in our simulations, the aim being in studying the impact of the different shielding metal layers on the Global Shutter Efficiency performances of the image sensor. As an example, if one simulation contains the metal layers combination “M1+M3” it means that the M1 layer as well as the M3 layer will be present in the simulation, while M2 will disappear and its place filled by Inter-Layer Dieletric.

One may notice that there exists no VIA contacting the Storage Node. The 2D-cut has been chosen along a line that does not include a VIA, with the aim in allowing for a better visualization of the electric field distribution at the Si/SiO_2 interface and still reproducing a realistic case, since the Storage Node is not contacted throughout its entire region. Nevertheless, it would be possible to perform a supplementary simulation including the VIA contact, but we will not focus on this issue at the moment. The two cases are shown in Fig. 3.13.

Let us start gradually through the analysis of the electric field distribution at the Si/SiO_2 interface for just three shielding combinations: “M1”, “M2” and “M3”. Some numbers first:

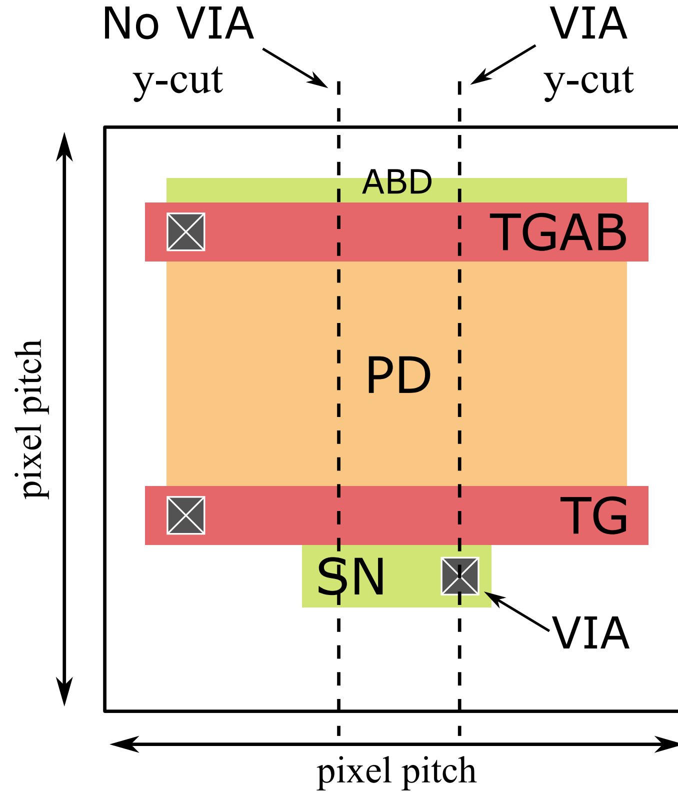


Figure 3.13: Top-view schematic of a pixel including some possible VIA positioning. Two *y-cuts* have been given as examples, one passes through the VIA and both the PhotoDiode and Storage Node, the other one passes through both PhotoDiode and Storage Node but not through the VIA.

when considering a wavelength of $\lambda = 650\,\text{nm}$ and for a slit dimension of $D = 2\,\mu\text{m}$, the Fresnel number results as following:

- **M1:** $N_F \approx 2.56$;
- **M2:** $N_F \approx 1.08$;
- **M3:** $N_F \approx 0.68$.

The three cases are found in Fresnel approximation ($N_F \sim 1$), special case the "M3" going towards the Fraunhofer approximation ($N_F \ll 1$); the Fresnel number decreases as a higher metal level is used. Fig. 3.14 shows the 1D electric field distribution at the Si/SiO_2 interface for the three cases: "M1", "M2" and "M3". The different patterns are clearly visible, especially inside the PhotoDiode region. One thing is worth of notice: the two spikes next to the PhotoDiode region correspond to the light transmitted through the two transfer gates (TG and TGAB) modifying the expected Frensel pattern, as highlighted by Fig. 3.15 in which the 2D electric field distribution is shown for the "M1" case. Again, no salicidation on top of the TG has been simulated; its presence may reduce the spikes due to the high absorption coefficient

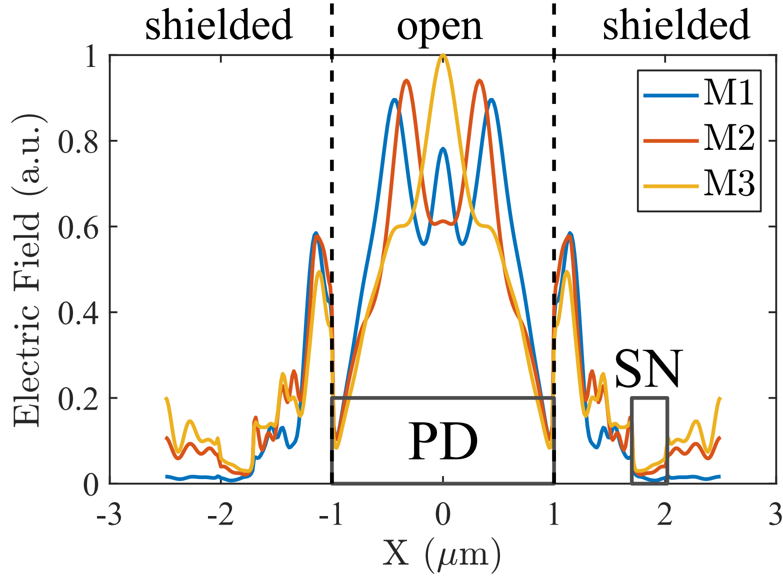


Figure 3.14: 1D electric field distribution at the Si/SiO_2 interface for $\lambda = 650\,\text{nm}$ simulated for different shielding layers. The two circles show the different electric field intensity in the so-called "dark" region as function of shielding layers.

of the material (generally $CoSi_2$ or $TiSi_2$ [HC97]; [Mae+99]). Nevertheless, differences in the electric field intensity are visible in the shielded region, thus comforting our hypothesis.

Fig. 3.16 describes the pixel Parasitic Light Hardness (1/PLS) response as function of shielding metal layer and wavelength. In a first analysis, it can be appreciated how the Parasitic Light Hardness (1/PLS) decreases as function of wavelength, for $\lambda \leq 700\,\text{nm}$ per every chosen shielding combination; exploiting the Fresnel number analysis, when shifting towards longer wavelengths N_F increases, thus leading to electric field distributions that spread increasingly towards the "dark" region, with the Storage Node region being reached by an increasingly number of photons. For $\lambda > 700\,\text{nm}$ the Parasitic Light Hardness (1/PLS) slightly increases; the Fresnel number continues to increase, though photo-generation of charges happens mainly deeper in the silicon substrate than close to the surface. The number of photo-generated charges inside the Storage Node region starts decreasing, charges generated deeply are increasingly screened by the PWELL potential barrier, therefore limiting the Storage Node light sensitivity, as previously shown, and being the main reason behind the slight Parasitic Light Hardness (1/PLS) increase. Let us analyze the presented figure from another perspective. Three colors have been chosen to represent certain categories of shielding and can be described as follows:

- **Blue:** The color blue represents the family of curves resulting from simulations of the pixel structure where the lowest metal shielding layer is "M1". As an example, the combination "M1+M3" exploits two metal layers for shielding purposes and the lowest metal layer exploited is "M1".

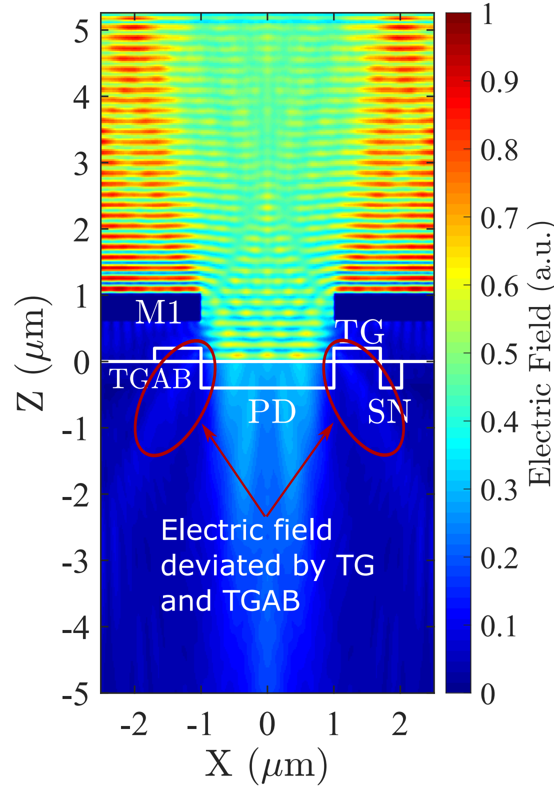


Figure 3.15: 2D electric field distribution for $\lambda = 650\,\text{nm}$ simulated for the "M1" structure. The two ellipses show the deviation of the electric field due to refraction onto the TG and TGAB, thus creating the spikes seen in Fig. 3.14.

- **Red:** The color red represents the family of curves resulting from simulation of the pixel structure where the lowest metal shielding layer is "M2".

- **Yellow:** The color yellow represents the family of curves resulting from simulation of the pixel structure where the lowest metal shielding layer is "M3". Having said that only three metal levels would be exploited, it is evident that only one curve is represented in yellow.

This categorization helps in distinguishing one important result of our simulations: the Parasitic Light Hardness (1/PLS) response of pixels exploiting the same lower shielding layer is similar and groups can be formed. Notably, pixel structures including the lowest shielding metal layer, i.e. "M1", have better Parasitic Light Hardness (1/PLS) performances compared to the other pixel structures. In a similar way, pixel structures including "M2" as the lower metal shielding layer obtain better performances compared to the simple "M3" structure.

A similar analysis can be withdrawn when looking at Fig. 3.17, where the Storage Node Quantum Efficiency is depicted as function of wavelength and shielding metal layers. In a similar manner, the blue curves represent results from structures having "M1" as the lowest

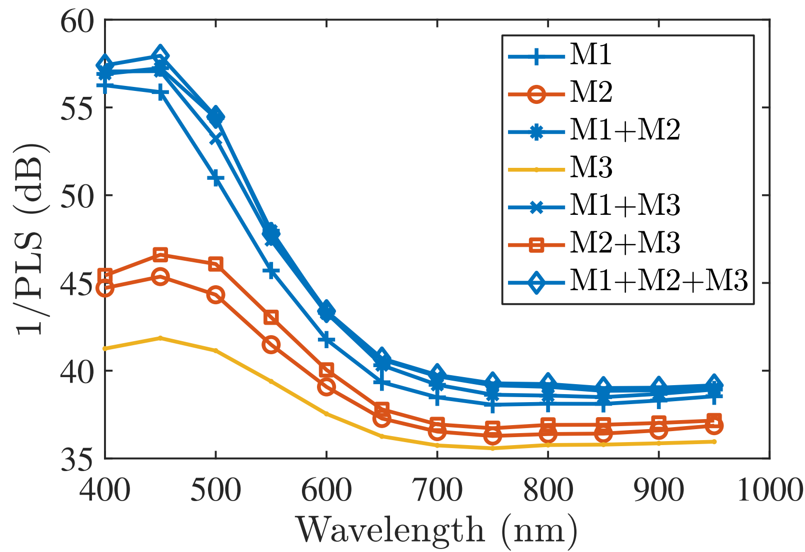


Figure 3.16: Simulation of the evolution of Parasitic Light Hardness (1/PLS) as function of wavelength and shielding metal layers. The blue group has “M1” as the lowest metal shielding layer, the red group has “M2” as the lowest metal shielding layer and the yellow group has “M3” as the lowest metal shielding layer.

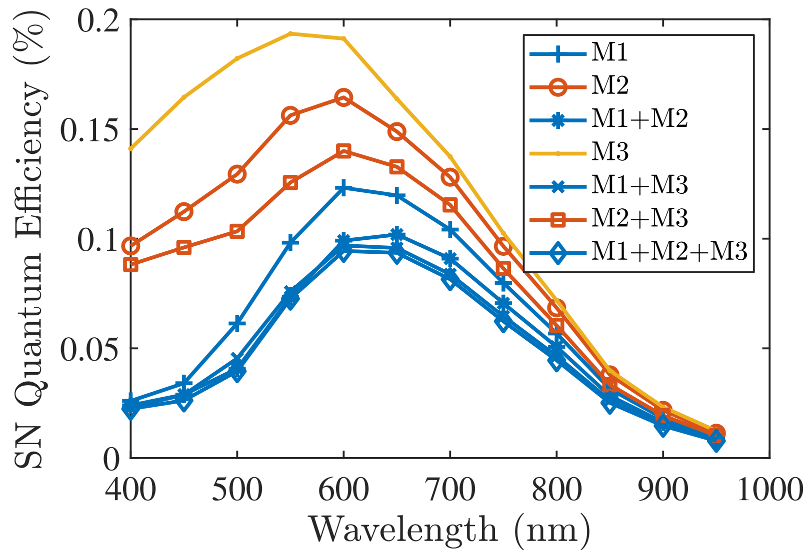


Figure 3.17: Simulation of the evolution of Storage Node Quantum Efficiency as function of wavelength and shielding metal layers. The blue group has “M1” as the lowest metal shielding layer, the red group has “M2” as the lowest metal shielding layer and the yellow group has “M3” as the lowest metal shielding layer.

metal level, the red curves having “M2” as the lowest metal level and the yellow curve having “M3” as the lowest metal level. It appears clearer how exploiting the lowest metal shielding

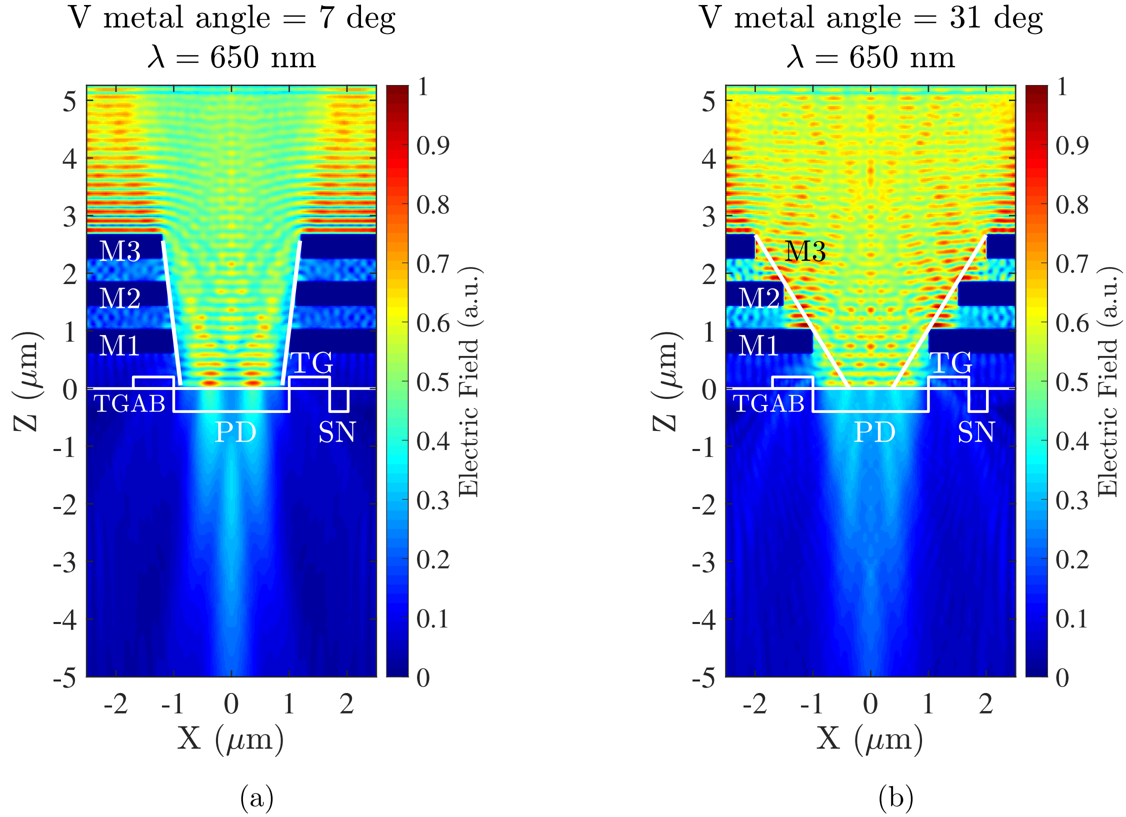


Figure 3.18: 2D electric field of the simulated structure with a V-shape arrangement of the metal layers, (a) at 7 degrees and (b) at 31 degrees. Simulations have been performed at $\lambda = 650\,\mathrm{nm}$. The white lines show the V-shape angle of the structure.

level helps in reducing the Storage Node Quantum Efficiency. Groups are formed as well, where there is little difference between the structures shielded with “M1”. A slight deviance from the “M1” group can be appreciated in the “M1+M3” structure, where around $\lambda = 600\,\mathrm{nm}$ it approaches the “M2” group; reason behind this remains unclear. Strong differences between different metal shielding levels are visible at short wavelengths ($\lambda \leq 700\,\mathrm{nm}$), while at longer wavelengths the diffusing charges collection prevails on direct optical collection, with the latter being more dependent on diffraction. A maximum in the Storage Node Quantum Efficiency can be appreciated around $\lambda = 600\,\mathrm{nm}$ per every structure. The reason behind this maximum could be found in the fact that both diffraction and charges diffusion are contributors at this wavelength, while for longer wavelengths the optical contribution drastically drops (as seen in Fig. 3.17) and conversely for shorter wavelengths the diffusion contribution is limited due to fewer charges generated deep in the epitaxial layer.

Finally, some simulations have been performed arranging the metal layers in a *V-shape*, as shown by Fig. 3.18. Various V-shape angles have been simulated in order to appreciate the impact on the Storage Node light sensitivity. However, it appears from Fig. 3.19 that the V-shape increases the Storage Node light sensitivity in comparison with the all-straight

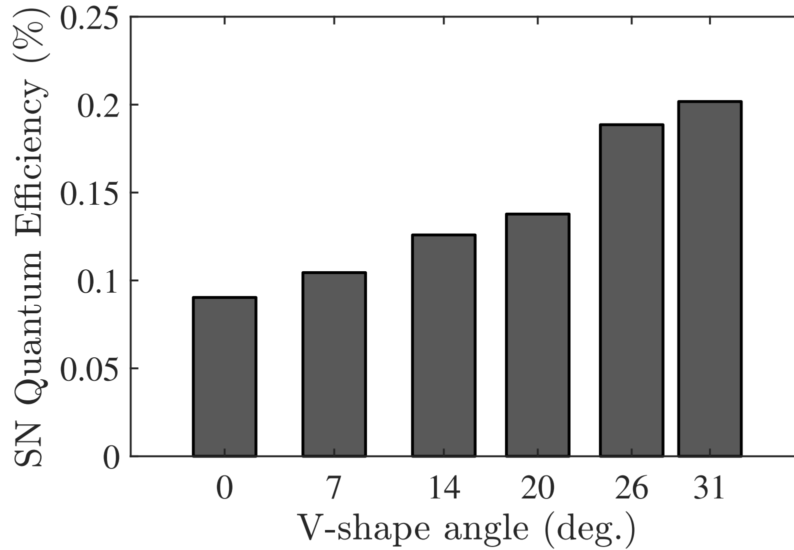


Figure 3.19: Storage Node Quantum Efficiency as function of the V-shape angle of the simulated “M1+M2+M3” structures. Results are presented for $\lambda = 650\,\text{nm}$.

structure “M1+M2+M3” (V-shape angle = 0), probably due to the fact that light is invited to follow a diagonal path instead of a straight one, as shown by the electric field charts.

3.3.2 Metal layers positioning optimization

It has been shown the importance of light diffraction for accounting Global Shutter Efficiency performances in Global Shutter CMOS Image Sensors and how the use of the correct metal shielding level can help in reducing diffracted light to spread towards the “dark” region. However, up until now all considerations have been withdrawn considering only one light shield aperture right above the PhotoDiode, meaning that distance between the beginning of the Storage Node region and the end of the metal shielding aperture has been kept constant. We have seen that light tendency to spread due to diffraction depends on wavelength, shield aperture and distance from the Si/SiO_2 interface and those parameters are not always under our entire control.

With the aim in keeping the diffracted light as far as possible from reaching the Storage Node region, let us analyze the impact of the shielding metal layer positioning with respect to the Storage Node region. We therefore seek for reduction of the slit dimension in the shielding metallic layer, thus keeping fixed one end of the slit and relocating the other end (the one closer to the Storage Node region). As a drawback, this method would lead to a smaller slit dimension, increasing the Fresnel number and thus increasing light diffraction effect as well as reducing the fill factor and the PhotoDiode light sensitivity. It is nevertheless of great interest to understand if the method can still be useful for Global Shutter Efficiency performances improvement.

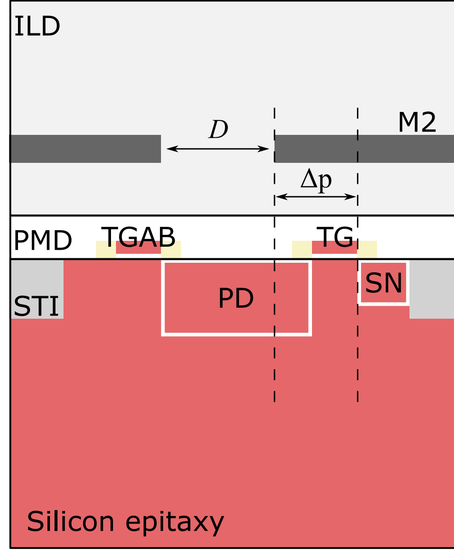


Figure 3.20: Schematic of the FDTD simulated pixel. The slit dimension D changes as function of the *overlap*, which is defined as the distance between the end of the metal shielding layer and the beginning of the Storage Node region. The PhotoDiode dimension is fixed and equal to 2 µm.

In order to better understand the study that has just been described, it could be helpful to take a look at Fig. 3.20, the simulated structure is described. It is similar to the one exploited for studying the impact of different metal shielding layers, with the difference being in the distance between the beginning of the Storage Node region and the end of the shielding metal layer, denoted by the parameter Δp. When $\Delta p = 0.7\,\mu m$, the distance between the left and right hand of the slit, thus the slit dimension, is equal to the PhotoDiode length ($D = x_{PD}$), corresponding to the structure presented for the study on shielding metal layers combination. It becomes clear that if Δp increases, the slit dimensions D decreases accordingly.

Fig. 3.21 shows the Parasitic Light Hardness (1/PLS) simulation results of the presented study for three different shielding metal layers at a determined impinging wavelength $\lambda = 650\,nm$. A reduction in the Parasitic Light Hardness (1/PLS) with respect to the shielding metal level exploited can be noted, starting from $\Delta p \geq 0.5\,\mu m$. As stated in Eq. (2.13), at a given slit size the Fresnel number is lower at longer distances; a lower Fresnel number leads to Fraunhofer diffraction, thus a more pronounced diffraction effect. The PhotoDiode Quantum Efficiency is smaller for a higher metal shielding level due to the spread of the electric field beyond the PhotoDiode region, as shown in Fig. 3.22. Nevertheless, the Storage Node Quantum Efficiency similarly decreases due to the weaker light power reaching the Storage Node region. Further on, a decrease in the Parasitic Light Hardness (1/PLS) for M2 and M3 for $\Delta p \geq 1.4\,\mu m$ is shown in Fig. 3.21. This is due to a reduction in the PhotoDiode Quantum Efficiency, always due to the spread in the electric field, while Storage Node Quantum Efficiency remains relatively constant and seems to have reached a minimum. Finally, one may argue that reducing the slit dimension would also reduce the PhotoDiode light sensitivity. The statement is correct and demonstrated in Fig. 3.22. Nevertheless, the increase in

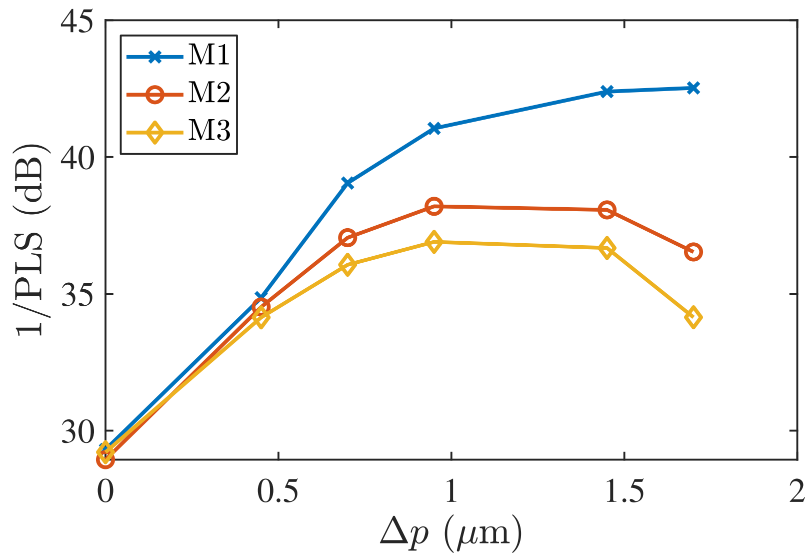


Figure 3.21: Parasitic Light Hardness (1/PLS) simulation results at $\lambda = 650\,\mathrm{nm}$ as function of shielding metal layers and Δp, being the distance between one end of the metal shielding layer and the beginning of the Storage Node region.

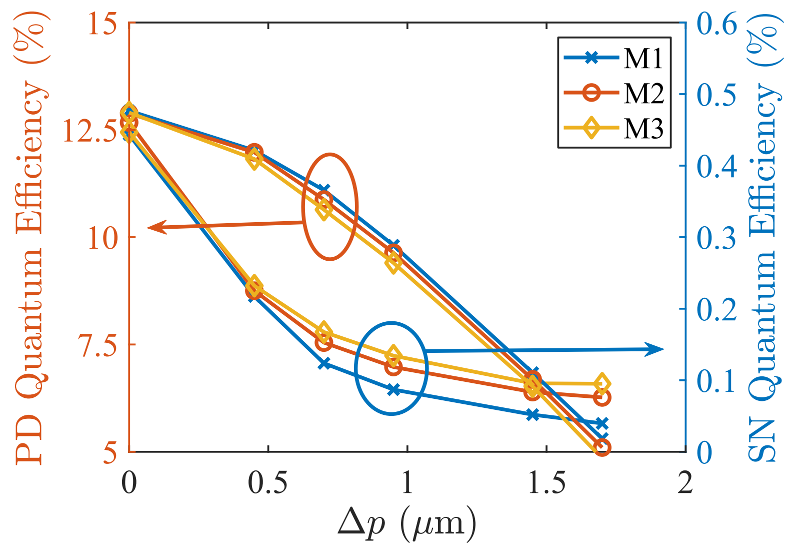


Figure 3.22: Quantum Efficiency simulation results for both PhotoDiode (on the left) and Storage Node (on the right) at $\lambda = 650\,\mathrm{nm}$ as function of shielding metal layers and Δp, being the distance between one end of the metal shielding layer and the beginning of the Storage Node region.

the Parasitic Light Hardness (1/PLS) can be explained from the fact that reduction of the Storage Node light sensitivity has a higher impact on Global Shutter Efficiency performances with respect to the PhotoDiode light sensitivity, as presented at the beginning of this chapter

and better described by Fig. 3.1. The study has been also extended to different metal combinations and impinging wavelengths showing similar results behavior; therefore, this extension has not been presented with the aim in avoiding redundancies.

When advanced technological features (like the Tungsten Buried Light Shield (WBLS) [Vel+16]) for Storage Node shielding are not available, improvements of Global Shutter Efficiency performances in Global Shutter CMOS Image Sensors has to pass through a careful pixel design exploiting metallic interconnections with light shielding purposes. The lowest metal level M1 has proven to be the more suited to reduce Storage Node light sensitivity; exploiting the M1 with other metal levels for shielding purpose does not necessarily bring to improvements in the performances. Further on, a *V-shape* arrangement of shielding metal layers may lower the Global Shutter Efficiency performances if the angle is too steep. Improvements in the Global Shutter Efficiency performances can also be sought by a more accurate positioning of the shielding metal layer. In our case, it has been shown how a slight overlap between the PhotoDiode region and the shielding metal can help in improving Parasitic Light Hardness (1/PLS). As a rule of thumb, the usage of the lowest metal shielding layer and its positioning further beyond the Storage Node region can boost the Global Shutter Efficiency performances of 100% circa (calculated at $\lambda = 650\,\text{nm}$ from the "M3" structure vs. the "M1" structure with $\Delta p = 1\,\mu\text{m}$).

3.4 Use of micro-lenses for performances improvement

In order to operate Global Shutter Efficiency performance improvements exploiting commercial CMOS Image Sensor technology, we have analyzed some pixel design modification exploiting the metallic interconnection layers as light shields. Nevertheless, some commercial CMOS Image Sensor technologies allows the designer in the use of an extra weapon to boost image sensor performances, the *micro-lens*. Convex micro-lenses have become the standard technology for focusing impinging light onto the PhotoDiode region [PSC88], thus improving light propagation through the BEOL stack, pixel light sensitivity and pixel response when light is impinging with a non-perpendicular angle. The micro-lens fabrication process consists in a resin thermal reflow, allowing for the achievement of a convex shaped resin on top of the pixel structure. Generally, another resin layer is put between the pixel stack and the micro-lens, in order to adapt the micro-lens to its focal length. The thermal reflow process allows micro-lenses to obtain a hemispherical shape.

It is easy to understand that the presence of a micro-lens in a pixel structure increases the Global Shutter Efficiency performances of the image sensor, thus focusing light around the PhotoDiode area and considerably improving its light sensitivity. To give an understanding of the impact of micro-lens on the pixel structure, Fig. 3.23 shows the electric field distribution at $\lambda = 650\,\text{nm}$ at the Si/SiO_2 interface for the same pixel structure with and without micro-lens. As expected, the amount of light conveyed towards the PhotoDiode region is higher when exploiting a micro-lens. Lateral fringes can nevertheless be observed, as diffraction is still present even after the addition of a micro-lens [You71].

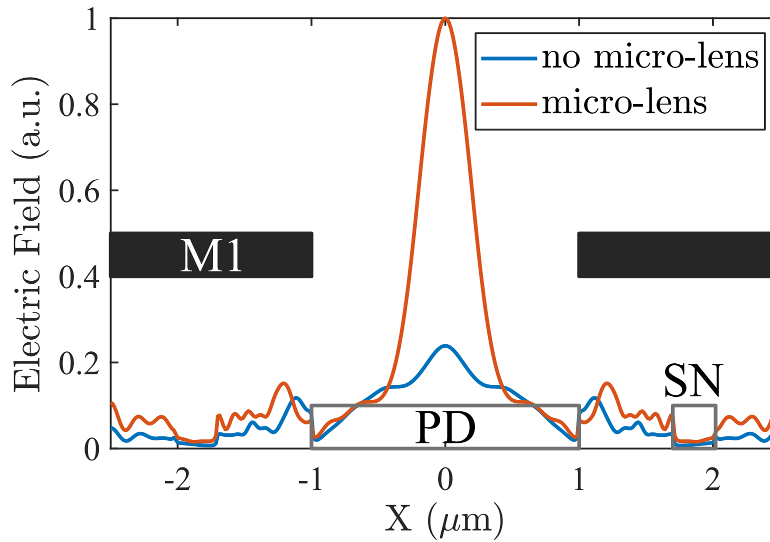


Figure 3.23: 1D electric field distribution at $\lambda = 650\,\mathrm{nm}$ at the Si/SiO$_2$ interface for two similar structures differing only by the presence of a micro-lens. The PhotoDiode and Storage Node location are indicated by the hollow light gray rectangles. Positioning of the shielding metal layer exploited (M1) is indicated by the dark gray rectangles, determining an opening of $D = 2\,\mu\mathrm{m}$.

Micro-lenses are not able to completely suppress the Parasitic Light Sensitivity issue; charges are still generated deep in the epitaxial layer at longer wavelengths and diffraction may still be an issue. The free photo-generated charges can therefore diffuse towards the Storage Node region thus contributing in lowering the Global Shutter Efficiency performance of the image sensor.

Knowing the advantages given by the presence of a micro-lens, we would like to analyze if it is possible to exploit this tool to improve the Global Shutter Efficiency performance even further, as for example changing the focusing point of the micro-lens, or in other words, changing the micro-lens centering.

3.4.1 Micro-lens centering optimization

This study has been conducted knowing that the critical regions for diffusing charges collections are located around the Storage Node area, as previously shown in Fig. 3.6. Reduction of the charges photo-generation around this critical area is expected to bring a decrease in the Storage Node light sensitivity.

In order to perform our study, a few pixel structures have been simulated with the help of the developed model, each pixel structure differing from the micro-lens centering position, as shown in Fig. 3.24. We define the reference position as the PhotoDiode center, denoted as 0, where the micro-lens is normally centered with the aim in increasing the PhotoDiode light

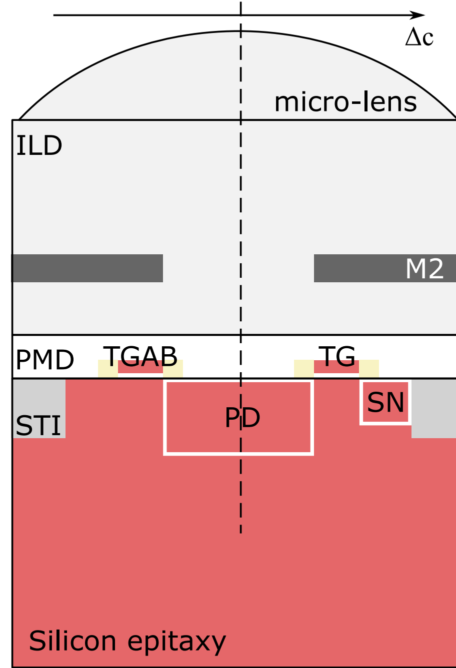


Figure 3.24: Schematic of the FDTD simulated pixel. Δc defines the shift in the micro-lens position with respect to the center of the PhotoDiode. Slit dimension D is constant and equal to 2 µm

collection. Δc defines the shift in the micro-lens center with respect to the reference position, if $\Delta c > 0$, the micro-lens center position is shifted towards the Storage Node region, if $\Delta c < 0$ the micro-lens center position is shifted towards the other end.

Modeling of the micro-lens in the FDTD simulation has to be mentioned. We have modeled the micro-lens shape as a perfect hemispheric structure. Micro-lens material is nevertheless unknown as well as its refractive index; we have therefore supposed that the micro-lens refractive index is identical to the Inter-Layer Dieletric one as well as for the focus-adapting resin. One last thing concerning the focus length: the micro-lens can be considered as a plano-convex lens, with the convex side having a curvature radius R_c. Using the lensmaker's equation [ref Hecht Optics] it is possible to simply calculate the lens focal f distance, when the lens is in contact with air, as:

$$\frac{1}{f} = \frac{n_{lens} - 1}{R_c} \tag{3.6}$$

where n_{lens} accounts for the micro-lens refractive index. Once the focal distance is calculated, it is simply to define the thickness of the focus-adapting resin.

Fig. 3.25 shows the evolution of the Parasitic Light Hardness (1/PLS) as function of the micro-lens centering shift. In accordance with our theories, the Parasitic Light Hardness (1/PLS) increases as the micro-lens center shift far away from the Storage Node region; nevertheless, the PhotoDiode light sensitivity decreases as the micro-lens center is shifted towards the boundaries of the slit (approximately 20% each 0.2 µm), up to the point where

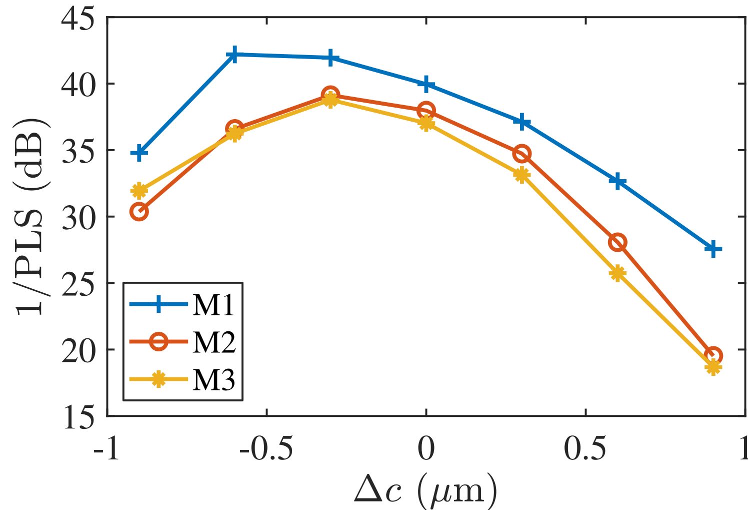


Figure 3.25: Parasitic Light Hardness (1/PLS) simulation results as function of shielding metal layers and micro-lens centering at $\lambda = 650\,\mathrm{nm}$

the PhotoDiode light sensitivity decreases that much (-50% with respect to the micro-lens positioned in the center) that the Parasitic Light Hardness (1/PLS) is consequently affected and thus decreasing, as can be appreciated for $\Delta c < -0.3\,\mu\mathrm{m}$.

Micro-lens is a powerful design tool to exploit for improving the image sensor Global Shutter Efficiency performance. Our simulations show an improvement of the Global Shutter Efficiency performances for a micro-lens center shift of $-0.3\,\mu\mathrm{m}$ with respect to the PhotoDiode center, given a PhotoDiode length of $2\,\mu\mathrm{m}$. Further simulations would be required to choose an optimal center shift given a different PhotoDiode length. A trade-off is nevertheless required between Parasitic Light Sensitivity and PhotoDiode light sensitivity, since this latter may be reduced by the micro-lens center shift.

3.5 Conclusion

This chapter has been devoted to the exploitation of the model as a support for pixel designers to improve the Global Shutter Efficiency performances of Global Shutter CMOS Image Sensors through fast and cost-effective simulations. Three different usage levels of the developed model have been shown:

1. Exploiting the complete model allows for a direct calculation of the image sensor Parasitic Light Sensitivity, as well as the Quantum Efficiency of both PhotoDiode and Storage Node. Notably, calculations of PhotoDiode Quantum Efficiency are highly required, being the main parameter determining the image sensor light sensitivity. On

the other hand, calculation of the Storage Node Quantum Efficiency can be required to compare the performances of different structures and to reduce the image sensor Parasitic Light Sensitivity.

2. Exploiting the optical simulations through a visual analysis of the electric field distribution at the Si/SiO_2 interface. Notably, this visual analysis can help in understanding the amount of light diffracted as well as the regions highly impacted by light diffraction. A global vision of the impinging light onto the Si/SiO_2 interface could improve in accurately designing the light shielding layers.

3. Exploiting the transport simulations and the transport transfer function as a visual tool to inspect the critical areas that are responsible for the non-negligible Storage Node light sensitivity, thus leading to the Parasitic Light Sensitivity phenomenon. The visual location of critical areas could help the designer in limiting the charges photo-generation in certain areas, thus reducing the amount of photo-generated charges that can be collected by the Storage Node.

Subsequently, the developed model has been used to quantify the impact of design elements on the image sensor Parasitic Light Sensitivity. It has been shown how the PhotoDiode and Storage Node dimensions can strongly impact the Global Shutter Efficiency performances, thus leading to an ideal pixel with the smallest Storage Node possible as well as the biggest PhotoDiode possible. Nevertheless, nodes dimensions have to take into account different parameters and fit into the pixel pitch; other tools have to be exploited to further improve Global Shutter Efficiency performances.

The role of light shielding through use of metallic interconnection layers has been investigated, given that the Storage Node direct light shielding could only be performed through metallic interconnection layers in some technologies. The advantages in the use of the lowest metal layer available have been demonstrated, thus confirming the previous hypothesis given by the exploitation of the Fresnel number and the Fresnel patterns for light diffraction.

Moreover, improvement of light shielding of the Storage Node through have been sought through the distance between the light shield end and the beginning of the Storage Node region. Results have shown that the Storage Node light sensitivity is indeed reduced when the given distance is increased; it is nevertheless important to take into account the change in light sensitivity of the PhotoDiode, that could be drastically reduced when operating such a solution.

Finally, micro-lens performances have been analyzed, given their ability to convey light towards a focal point. Notably, the micro-lens focal point can be shifted through an accurate shifting of the micro-lens center; this technique has been analyzed in order to allow for a charge photo-generation further away from the critical areas of the Storage Node light sensitivity. Again, the technique looks promising to reduce the Storage Node light sensitivity, though an important reduction in the PhotoDiode light sensitivity may bring to a sudden reduction of the Global Shutter Efficiency performances.

In the end, the developed model has proven its utility for giving design guidelines to

improve the Global Shutter Efficiency performances in Global Shutter CMOS Image Sensors. Nevertheless, results have shown how trade-offs are to be made between the image sensor Global Shutter Efficiency performances and the image sensor light sensitivity, corresponding to the PhotoDiode light sensitivity.

Finally, these results seem to prove the importance in taking into account the diffraction phenomenon of light whenever improvement in the Global Shutter Efficiency performances of the image sensor, and thus reduction of the Storage Node light sensitivity, are required. Following the shrinking pixel race, where companies are competing to build the smallest pixel possible, feature size inside the pixel would get smaller and smaller, thus phenomena like Parasitic Light Sensitivity would increasingly get affected by light diffraction.

Chapter 4

Characterization and modeling of Global Shutter CMOS Image Sensors

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The previous chapter focused on analyzing different possible solutions to improve the Parasitic Light Sensitivity performances of Global Shutter CMOS Image Sensors by taking advantage of the model developed in chapter 2. The simulations have been performed with two main aims in mind:

1. allowing fast comparison between CMOS Image Sensor technological processes, supposing that the device designer has limited access to technological improvements;
2. giving guidelines to improve design of Global Shutter pixels.

Various design parameters have therefore been analyzed, as for example the Storage Node dimensions, the usage of metal layers as light shielding layers, the presence of a micro-lens, to give a wider understanding on the behavior of Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors. The different simulations have allowed for an estimation of the impact of the different design parameters on the Parasitic Light Sensitivity performances of the image sensor, as well as giving a better understanding of the different phenomena that are responsible for the degradation of performances in Global Shutter CMOS Image Sensors, the Parasitic Light Sensitivity.

Following the path previously set, this chapter aims in providing an experimental reference to prove the assertions given in the previous chapters, thus providing validity of the developed model. Firstly, a metric for characterizing Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors is developed; successively, various Global Shutter CMOS Image Sensors are measured and compared to validate the assumptions made in the previous chapters. Finally, the developed model is compared to the experimental data.

Up to now, the problematic of Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors has been only analyzed from its physical point of view, thus focusing on the underlying phenomena and their modeling, as well as the different ways to improve performances through a careful analysis of the main impacting parameters. This chapters aims furthermore to bring the discussion to the signal point of view, where the existence of a perturbation in the output

signal caused by the non-negligible Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors is assessed, the final intent being in analyzing, proposing and comparing different post-processing solutions to mitigate the impact of Parasitic Light Sensitivity on the output signal of Global Shutter CMOS Image Sensors. In this regard, a model of the pixel output of the Global Shutter CMOS Image Sensors has been proposed and validated through experimental results and successively exploited to develop different post-processing methods.

4.1 Developing a metric for measuring Parasitic Light Sensitivity

Characterization of Parasitic Light Sensitivity, alongside the standard figures of merit (e.g. Quantum Efficiency, Dynamic Range, ...), has been determined as crucial to correctly determine the performances of Global Shutter CMOS Image Sensors. There exist some examples of metrics developed to measure the Parasitic Light Sensitivity of a Global Shutter CMOS Image Sensors [OnS]; [Mey+11]; nevertheless, the techniques mentioned present some drawbacks (time dependency, impossibility of measuring the per-pixel Parasitic Light Sensitivity, ...). Moreover, the *Standard for Measurement and Presentation of Specifications for Machine Vision Sensors and Cameras* (EMVA1288) [EMV] does not give guidelines to a standard metric for measuring Parasitic Light Sensitivity, thus a more general approach is needed, thus including spectral behavior of the Parasitic Light Sensitivity, where publications generally disclose the Parasitic Light Sensitivity behavior of the image sensor at one main wavelength. Finally, the metric should made available to measure Parasitic Light Sensitivity in various types of Global Shutter CMOS Image Sensors, regardless of the type of storing element (charge or voltage). In these regards, the current section will focus on the development of a metric for measuring Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors.

4.1.1 Electro-optical measurements of CMOS Image Sensors

In order to develop a metric to measure Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors, an electro-optical characterization setup has been exploited; its simplified architecture can be appreciated in Fig. 4.1. The CMOS Image Sensor is clamped on a breadboard, called proximity breadboard, on which all signal routing and some operations are performed, as for example analog subtraction of the reference and signal voltages, respectively V_{REF} and V_{SIG}, to ensure subtraction of the double sampling operation [Whi+74]; [Jan+01]. The resulting voltage is routed to an amplifier allowing a selection of 4 different gains and successively to a 14 bit ADC, in order to convert the analog signal to a more PC-friendly code. The ADC output is therefore fed to a PC. Due to the serial nature of the characterization setup, the image sensor is accessed and readout sequentially, i.e. one row is selected at a time and all columns are sequential readout, sampled and fed to the PC. A word generator and an FPGA are used to control the access and readout of the image sensor: the word generator is responsible for the construction of the command signals, while the

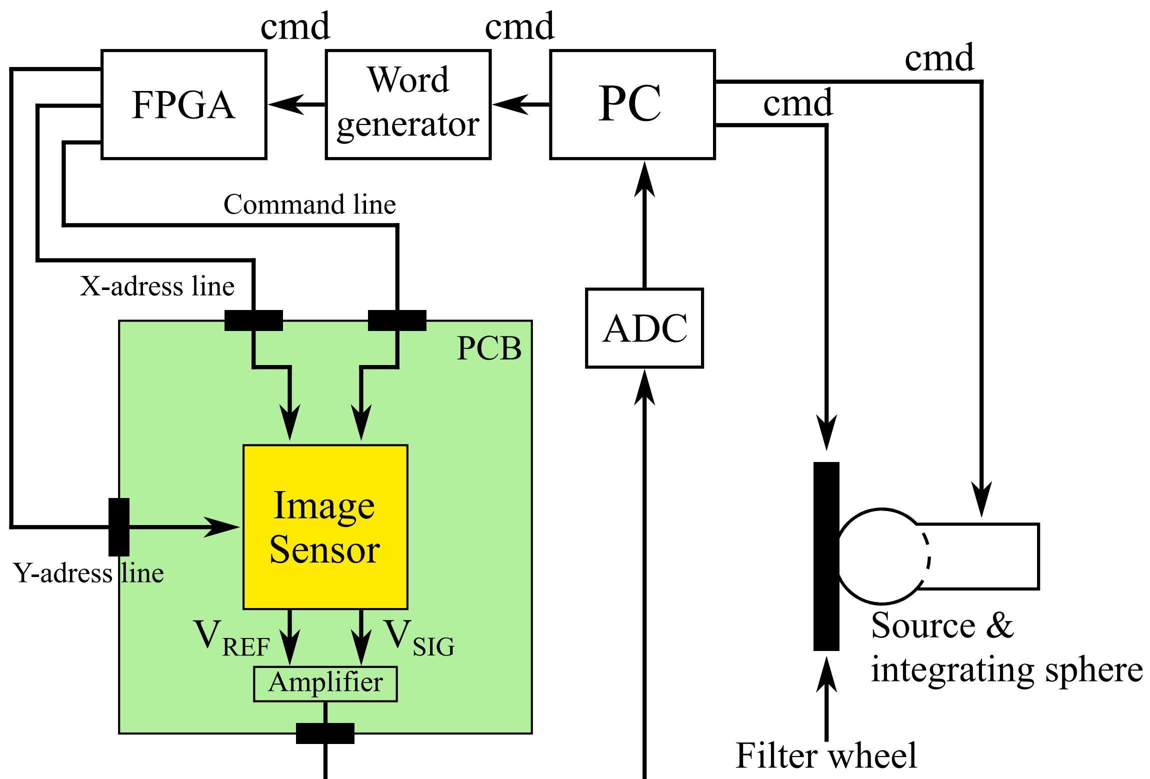


Figure 4.1: Schematic of the characterization setup used for electro-optical characterization. The CMOS Image Sensor is clamped on a PCB, connected to an FPGA, to receive addresses and commands, and to an ADC, for output digitalization. The digital signal is then fed to a PC. A software on the PC drives the FPGA and a word generator, the latter being responsible of the commands fed to the FPGA. Moreover, the PC drives the illumination source (the light source and the integrating sphere) and the colored filter wheel in front to select the wavelength.

FPGA is responsible for construction of the address signals; nevertheless, both address and command signals are routed via the FPGA for voltage adaption. The FPGA is synchronized to the word generator thanks to a clock signal delivered by the latter to the FPGA. For the image sensor illumination, a white light source and an integrating sphere are used as the illumination source. The required wavelength is then selected by placing a colored filter in front of the output slit of the illuminating source; in particular, a remotely controlled filter wheel, mounting 12 different colored filters with a band of ±10 nm, is used to rapidly select the required illuminating wavelength. The different blocks are remotely accessible through use of a software run on a PC; the user can select the illuminating wavelength and luminance as well as the command signals sequence, the size of the array in terms of rows and columns, the integration time and the output gain.

Fig. 4.2 presents a simplified schematic of the timing diagram operating the image sensor. The sensor is operated in a Rolling Shutter mode, i.e. sequential row integration and readout,

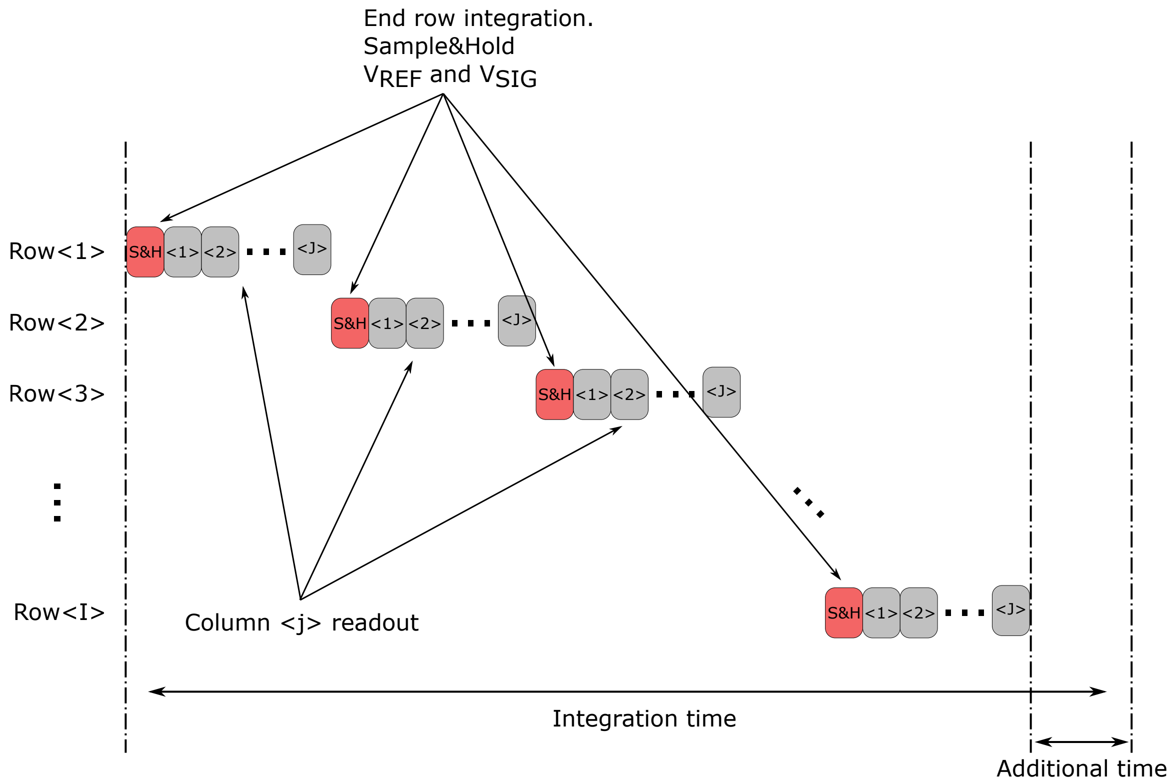


Figure 4.2: Time diagram of the measurement operations of a CMOS Image Sensor. The red block, called Sample&Hold, represents the sampling operation of the voltage shift resulting from charge integration. The gray block represents the readout of one single column, including digitalization of the V_{out} voltage through one ADC. The image sensor is operated on a row basis, first the row sampling operations are performed, followed by the readout of each column per the considered row. The same operations are then performed on the successive rows. The minimum integration time is defined by the time required to sample and readout all rows sequentially. An additional time can be added once the array readout operations are terminated.

in order to avoid any Parasitic Light Sensitivity induced signal on the output altering the measurement as well as exposing the entire array for the same amount of time. The CMOS Image Sensor under test allows both Rolling Shutter and Global Shutter operation modes, hence Rolling Shutter mode is the preferred operation mode for the required measurement.

As previously presented, the analog output signal is converted to digital by an external ADC, therefore the output must be serialized; after sampling and holding the values of V_{REF} and V_{SIG} per each column at one row, column-by-column subtraction and digitalization is performed and stored in the computer before skipping to the subsequent row. Given the structure of the readout method, the minimum integration time is determined by the number of rows and columns as well as the speed of single column readout; for a 256×256 array, the minimum integration time on the exploited characterization setup is set to 34.56 ms. If required, additional time can be added at the end of the array readout.

Details of the row Sample&Hold block time diagram will be given further on, as it differs if a measurement of the PhotoDiode or of the Storage Node is required.

A substantial number of acquisition is performed, per-pixel mean and standard deviation are computed; averaging high number of acquisitions allows to reduce the output noise [GWE04].

4.1.2 Measurements of Quantum Efficiency applied to the PhotoDiode

As presented in the previous chapters, Quantum Efficiency is a measure of the number of electrons collected by the PhotoDiode in a pixel with respect to the number of photons impinging on the same pixel under steady-state conditions; being the ratio of these two quantities, it results dimensionless and it is often presented as a percentage. Exploiting the previously presented characterization setup for the required measurements, it becomes clear that we need to be able to retrieve the number of impinging photons per pixel at a given sphere luminance as well as the number of collected electrons as function of the output voltage $\mathrm{V_{out}} = \mathrm{V_{REF}} - \mathrm{V_{SIG}}$.

Calculation of the impinging photons per pixel requires additional measurement of the irradiance, or power per unit area, at a given distance from the illuminating source. To this purpose, a Newport 818-UV/DB optical power meter has been exploited [New]; through use of precise laboratory mechanical moving parts, the optical power meter has been positioned so that its measuring surface corresponds to the silicon die surface. It is therefore possible to create a table of irradiance values given the wavelength and the sphere luminance. A linear interpolation of the resulting table at each wavelength allows estimation of the irradiance at every sphere luminance assignable value. Supposing uniform irradiance E_e at the silicon die surface, the passage to flux Φ_e requires knowledge of the pixel pitch p, as given by Eq. 4.1; calculation of per-pixel impinging photon rate Γ_{ph} is given by Eq. 4.2 and the total number of impingig photons per pixel at a given amount of time is then trivial [PG09].

$$\Phi_e = E_e \cdot p^2 \quad [=] \quad \mathbf{J \cdot s^{-1}} \tag{4.1}$$

$$\Gamma_{ph} = \frac{\Phi_e}{E_{ph}} = \Phi_e \cdot \frac{h\,c}{\lambda} \quad [=] \quad \#\mathbf{ph \cdot s^{-1}} \tag{4.2}$$

As one may notice, an integrating sphere has been used as the illumination source; integrating spheres use Lambertian reflectance to project a uniformly diffuse light through an exit hole. It is therefore important to verify that the image sensor under test, positioned at a given distance, is uniformly irradiated, to avoid measuring pixel non-uniformity due to non-uniform illumination. The cosine4 law [PG09] has been therefore exploited to verify uniformity throughout the whole array. Nevertheless, positioning the image sensor at an increasing distance will reduce the power per unit area attaining the surface, a trade-off between uniformity and power per unit area has been done; in our case, uniformity is 95%.

It is now important to understand how to retrieve the number of collected electrons as a

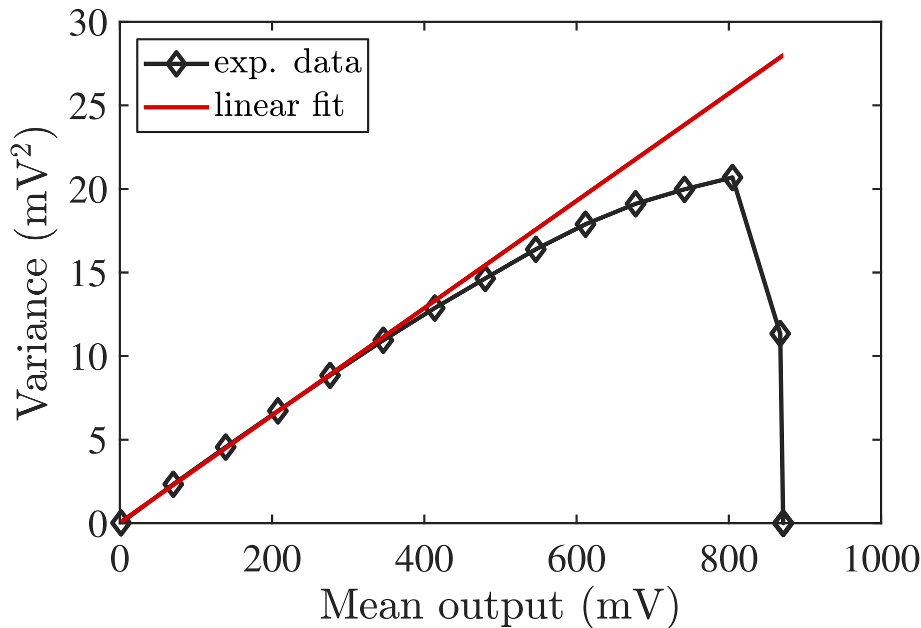


Figure 4.3: Example of Photon Transfer Curve (PTC) in black and estimation of the or conversion gain (CG) with the mean variance method, as represented by the red line [PH03].

function of the output voltage, or better as a function of the digitalized signal. Retrieval of the output voltage is possible knowing the ADC number of bits, its input voltage range and the chain gain in use. Conversion from output voltage to number of electrons requires knowledge of the image sensor conversion gain. Previously defined in Chapter 1, the conversion gain determines the voltage shift produced by an electron added to the floating capacitance, in our case the Storage Node. Fig. 4.3 shows an example of the estimation of the conversion gain of an image sensor by means of the mean-variance method, also known as the Photon Transfer Curve (PTC), presented in [PH03]; the slope of the linear interpolation represents the value of the image sensor conversion gain.

Supposing no lag at the pixel level, i.e. all the electrons collected by the PhotoDiode are transferred to the Storage Node, we are finally able to calculate the number of electrons collected by the PhotoDiode for a given amount of time. It is therefore possible to plot the number of collected electrons for a certain amount of time versus the number of photons given the same amount of time, the slope defining the Quantum Efficiency. Fig. 4.4 gives a visual understanding of the Quantum Efficiency measurements: the shadowed area represents the experimental data taken by 100 similar pixels at different illumination conditions and the black diamonds represent a mean of the experimental data per each illumination condition. Of the two behavioral regions that appear in the figure, the linear region is the crucial one for the estimation of the Quantum Efficiency; the red curve represents the linear regression performed on the linear region. A slight deviation from the linear regime can be appreciated starting from 40×10^3 impinging photons per pixels, this behavior shows as a reduction in the Internal Quantum Efficiency (η_i) at higher filling levels of the PhotoDiode, caused by a

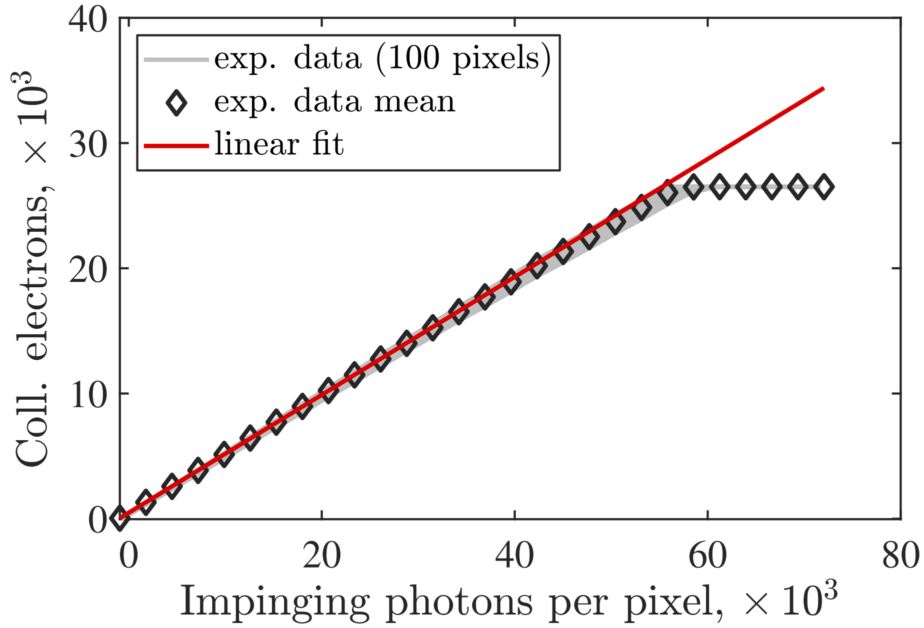


Figure 4.4: Example of Quantum Efficiency measurement. The gray area represents the response of 100 different pixels at different illumination conditions; the diamond markers represent the mean pixel response. The red line represents the linear regression of the mean pixel response. The number of collected electrons is linearly related to the output voltage produced by the image sensor per each measurement step.

reduction of the Space Charge Region associated with the PhotoDiode potential, diminished by a higher electron density presence [PH03]; [Boh+08]. Nevertheless, in a first approximation we will not take into account this deviation from the linear behavior and just compute the Quantum Efficiency exploiting the linear region at lower illuminations.

Taking a look back at Eq. (4.2) that the total number of impinging photons per pixel in a frame can be manipulated in two ways: either increasing the integration time of the frame or increasing the irradiance by adjusting the sphere luminance. It has been shown that an accurate calculation of the Quantum Efficiency requires different illumination levels, thus different numbers of impinging photons per pixel. It has been chosen to perform the Quantum Efficiency measurement through variation of the impinging irradiance, keeping the integration time fixed. The Dark Current contribution will therefore result constant at each illumination step, acting as an offset that is easily canceled out calculating the slope of the linear regression.

Fig. 4.5 shows a detailed time diagram of the row <n> Sample&Hold red block previously shown. Correlated Double Sampling is made available and exploited thanks to the presence of a pinned PhotoDiode, a TG and the operations of the image sensor in a Rolling Shutter fashion. Sample&Hold of V_{REF} is performed through the SHR command soon after the reset operation (RST signal pulsed high); Sample&Hold of V_{SIG} is performed through the SHS command soon after the charge transfer operation (TG signal pulsed high). This sequence

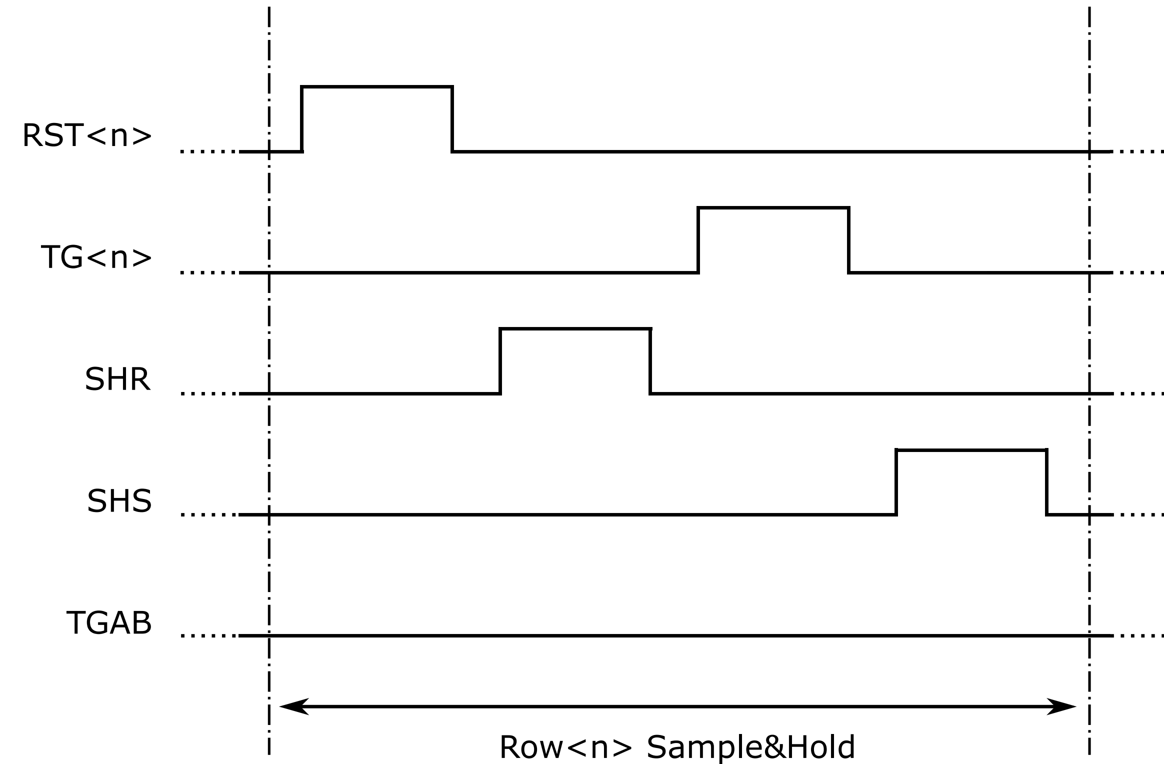


Figure 4.5: Time diagram of the Sample&Hold block exploited to measure the voltage shift produced by the charges collected by the PhotoDiode. Operating with a 5T Global Shutter pixel, Correlated Double Sampling is made possible. Almost at the end of the integration period, the Floating Diffusion is reset operating the RST command and its voltage value is sampled operating the SHR command; the integration period terminates soon after operating the TG command to transfer the charges collected by the PhotoDiode to the Floating Diffusion. The voltage value is then sampled operating the SHS command. TGAB is biased at ground throughout both integration and sampling.

is performed in order to sense the charge collected by the PhotoDiode during the given integration time. Global commands as TGAB_G, TG_G and RST_G are not exploited in this configuration; nevertheless, ABD is continuously biased at 3.3 V to put the image sensor under standard polarization conditions, as well as avoiding possible charge injection from the ABD to the PhotoDiode if left floating or grounded.

4.1.3 Quantum Efficiency measurement on the Storage Node

When defining the Quantum Efficiency of an image sensor, we generally refer to the Quantum Efficiency of the element responsible for the collection of photo-generated charges, the PhotoDiode, regardless of its type (pinned or not) and of the pixel type (3T, 4T, 5T, ...). Nevertheless, any other diffusion element integrated in the pixel is capable, with a higher or lower yield, to collect photo-generated charges. It is therefore possible to define a Quantum

Efficiency of another element integrated in the pixel in a similar manner to what performed on the PhotoDiode, though considering charges collected by the required element. Specifically, we are interested in analyzing and measuring the Quantum Efficiency of the Storage Node within the scope of the development of a metric to measure the Parasitic Light Sensitivity of Global Shutter CMOS Image Sensors.

In a 5T pixel, the Storage Node is represented by the Floating Diffusion; measurements of its collected charges can be performed as a 3T pixel readout operations. Readout operations of a 3T pixel require a different row Sample&Hold block timing diagram with respect to the one presented previously; Correlated Double Sampling is no more available. Nevertheless, Non-Correlated Double Sampling is performed to reduce other sources of noises like 1/f or FPN. Lacking the Correlated Double Sampling operation to cancel kTC noise, the floor noise level is increased. Few charges are expected to be collected from the Storage Node due to parasitic light, noise reduction is therefore important to avoid its dominance. In this regard, noise reduction is achieved through acquisition of a higher number of frame, being in this specific case 200, per each measurement step.

The limited number of electrons expected to be collected by the Storage Node implies an issue that must be addressed before proceeding to the measurements. Expecting a Quantum Efficiency of the Storage Node on the order of a fraction, a high number of incoming photons in the integration time window is required, in the interest of separating the output signal from the readout noise. An extremely high per-pixel photon rate might drive the system out of low-injection conditions, thus being non representative of the behavior of the device under real conditions. A long integration time window must therefore be exploited to accomplish a high number of photons without driving the system to high-injection levels.

Differently from a 3T pixel, a PhotoDiode is present and, upon saturation, can drastically alter the measurement of charges directly collected by the Storage Node; it is therefore crucial to connect the PhotoDiode to a high potential in order to constantly sweep away charges being collected. In other terms, TGAB is polarized high as well as its ABD; in this way, charges have one preferred direction to escape the PhotoDiode (through TGAB) limiting potential overflow towards the Storage Node.

Given all the considerations previously given, Fig. 4.6 shows the timing diagram of the row Sample&Hold block exploited during the Storage Node measurements. It can be noticed that TG is never exploited and TGAB is kept high at all times.

In a similar manner to what presented for the PhotoDiode Quantum Efficiency, the Storage Node Quantum Efficiency is found as the slope of the linear regression curve applied to the number of collected electrons versus the number of incoming photons. The number of electrons collected by the Storage Node can be easily retrieved exploiting the conversion gain calculated as described in sec. 4.1.2.

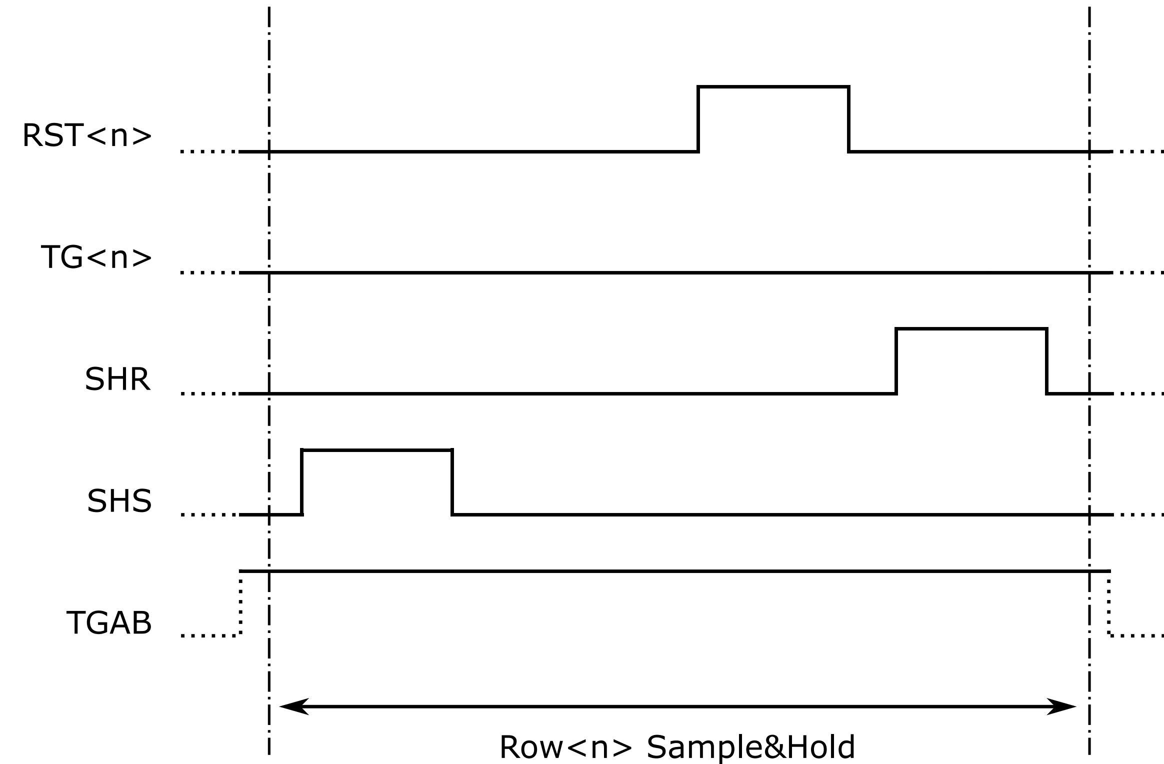


Figure 4.6: Time diagram of the Sample&Hold block exploited to measure the voltage shift produced by the charges collected by the Storage Node. Since the Storage Node is represented by the Floating Diffusion, Correlated Double Sampling is not available, thought Non-Correlated Double Sampling is operated. At the end of the integration period, the Storage Node voltage value is sampled operating the SHS command. Soon after, the RST command is operated to reset the Storage Node and restart the integration period; meanwhile, soon after the reset operation, the voltage value is sampled operating the SHR command, thus allowing Non-Correlated Double Sampling operation. TGAB is biased high throughout both integration and sampling in order to avoid any blooming from the PhotoDiode.

4.1.4 From Quantum Efficiencies to Parasitic Light Sensitivity

It has been previously stated that Parasitic Light Sensitivity can be retrieved as the ratio of the PhotoDiode sensitivity to light versus the Storage Node sensitivity to light; this ratio can be stated in more convenient terms through replacing the light sensitivity with the Quantum Efficiency. The Quantum Efficiency measurements previously presented serve therefore to right away calculate the Parasitic Light Sensitivity of the image sensor. It is interesting to notice that the presented metric allows calculation of Parasitic Light Sensitivity at different wavelengths, since it is simply required to measure the spectral Quantum Efficiency for both PhotoDiode and Storage Node. In our case, spectral Quantum Efficiency has been measured with the help of the filter wheel mounted in front of the exit of the integrating sphere previously presented. 12 filters with central wavelength spanning from 400 nm to 950 nm with a step of 50 nm, each with a bandpass of ±10 nm. If higher spectral precision is required, a

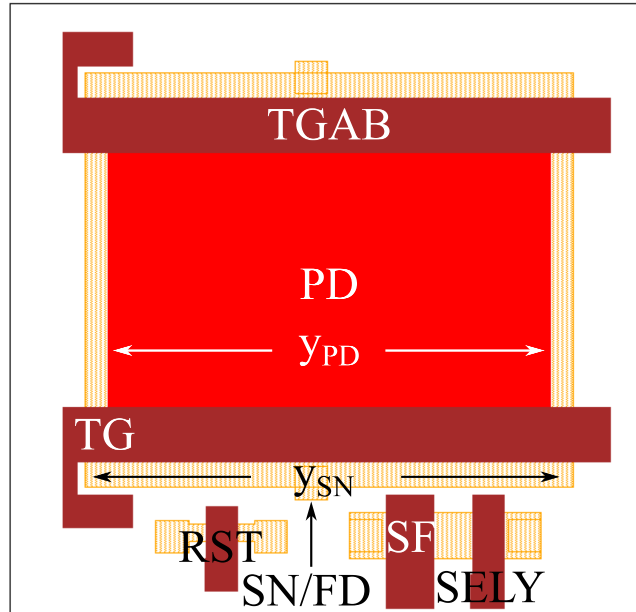


Figure 4.7: Schematic layout of a 5T Global Shutter pixel developed at ISAE-SUPAERO. The red bright zone represents the PhotoDiode implant; the shadowed orange zones represent the opening in the STI to allow ion implantation; the dark red zones represent the polysilicon regions, thus the gates. y_{PD} and y_{SN} represent respectively the width of the PhotoDiode and the Storage Node.

monochromator can be exploited to select the impinging wavelength.

Conclusively, the use of Quantum Efficiency measurements to retrieve the Parasitic Light Sensitivity of the image sensor allow performing spatial characterizations that can lead to a more complete analysis of the Parasitic Light Sensitivity, defining its spatial non-uniformity.

4.2 Characterizing Parasitic Light Sensitivity on a Global Shutter CMOS Image Sensor

In order to test the developed metric, we have exploited a Global Shutter CMOS Image Sensors with 5T pixels of 7 µm pitch, designed at ISAE-SUPAERO and produced with a commercially available 0.18 µm CMOS Image Sensor technological process. The PhotoDiode is of type "pinned" and the Storage Node is represented by the Floating Diffusion; charge transfer between the PhotoDiode and the Storage Node takes place through the TG; RST, SF and SELY transistors are integrated as well as the AB transistor. The array is composed of 256×256 5T pixels; the array is divided into 4 sub-arrays having different designs; each sub-array is itself divided in half, one half has integrated micro-lenses while the other one does not have any micro-lenses. There are therefore 8 different zones in the array, each one having

dimensions of 128×64 pixels. For the time being, we will focus on one of the 8 zones, the one having a large Storage Node width and without any micro-lenses integration. A schematic of its design can be appreciated in Fig. 4.7.

Fig. 4.8 shows the per-pixel characterization results of Quantum Efficiency for both (a) PhotoDiode and (b) Storage Node, as well as the (c) Parasitic Light Hardness (1/PLS). Let us analyze the Quantum Efficiency results before going into the details of the Parasitic Light Hardness (1/PLS). The PhotoDiode Quantum Efficiency figure shows a slight increase in the Quantum Efficiency at the top-left corner; the same analysis can be done on the Storage Node Quantum Efficiency figure (even if slightly more difficult to appreciate). This "vignetting" effect is caused by an inaccurate estimation of the number of photons impinging at the corners, probably caused by the slightly non-uniform illumination of the sample that is found at the top-left corner of the sub-array, given the round shape of the illumination spot. Being the estimation error common for both PhotoDiode and Storage Node, the ratio operation to compute the Parasitic Light Sensitivity cancels it out, thus leaving no visible effect on Fig. 4.8c.

The existence of few dark spots in the Storage Node Quantum Efficiency is related to hot pixels: those pixels present an important Dark Current thus preventing them to show any response to light. A MATLAB routine has been performed to detect hot pixels and assign a value of 0 to their Quantum Efficiency. When computing the Parasitic Light Sensitivity, a value of 0 is again assigned to the hot pixels.

Storage Node Quantum Efficiency non-uniformity has an important impact on the Parasitic Light Sensitivity non-uniformity, as shown by Fig. 4.8c; it is important to remember that the Storage Node Quantum Efficiency is found at the denominator in the calculation of the Parasitic Light Hardness (1/PLS), thus its slight variation results in an important variation for the Parasitic Light Sensitivity value. Hence, it can be said that the Parasitic Light Sensitivity non-uniformity of a Global Shutter CMOS Image Sensors is inversely related to the quality and variability of the Storage Node fabrication.

A closer look to the Parasitic Light Hardness (1/PLS) uniformity is given by Fig. 4.9, where the Parasitic Light Hardness (1/PLS) response histogram of the sub-array is presented for different wavelengths. Histogram peaks are clearly visible, thus determining the mean value of the Parasitic Light Hardness (1/PLS) per each wavelengths; non negligible dispersion is though appreciable. Nevertheless, the histograms show positive skewness (a right tail), thus resulting in few overperforming pixels.

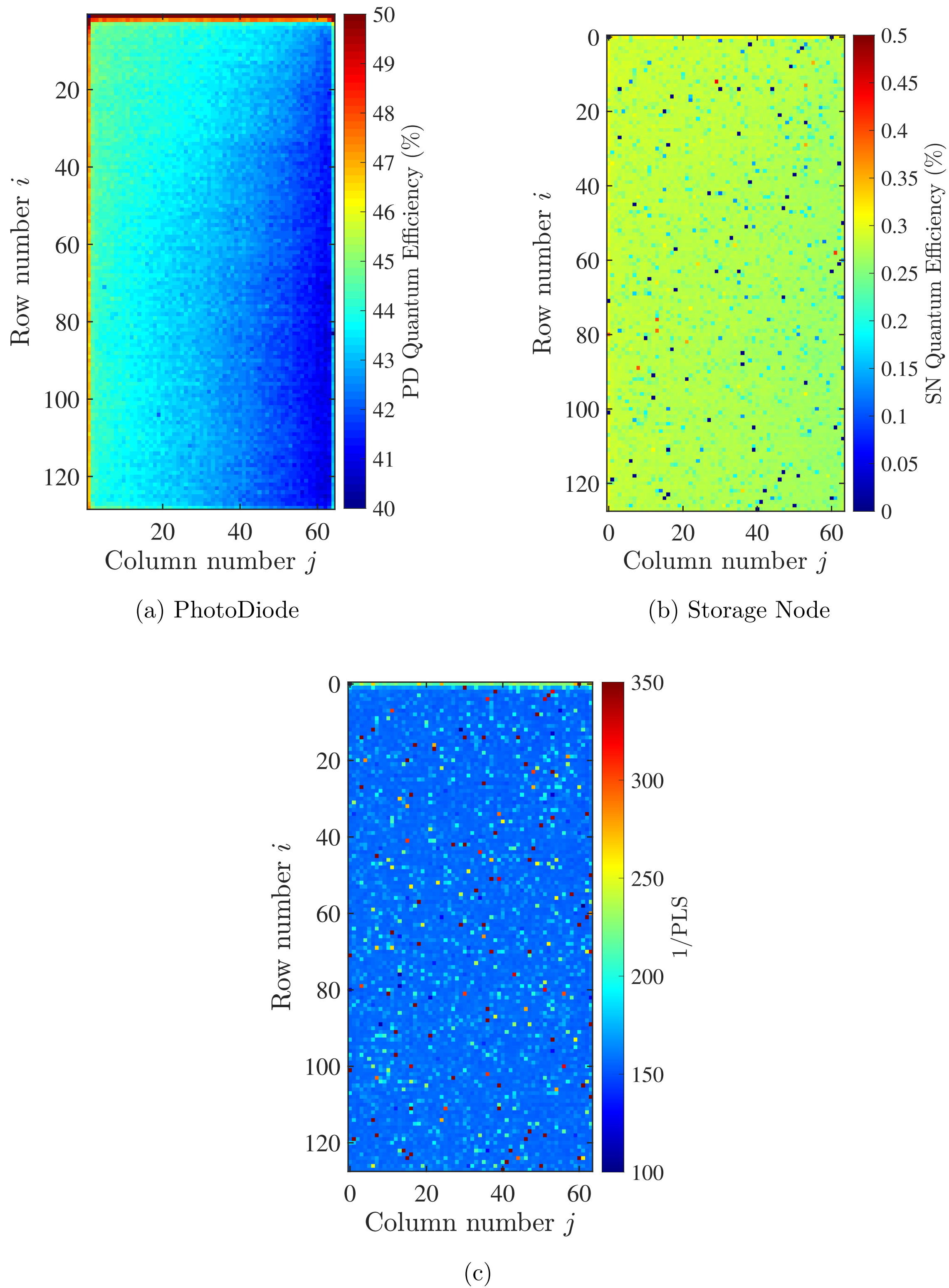


Figure 4.8: Per-pixel distribution of the measured (a) PhotoDiode Quantum Efficiency, (b) Storage Node Quantum Efficiency and (c) Parasitic Light Hardness (1/PLS) of the CMOS Image Sensor under test at a wavelength of $\lambda = 650\,\text{nm}$.

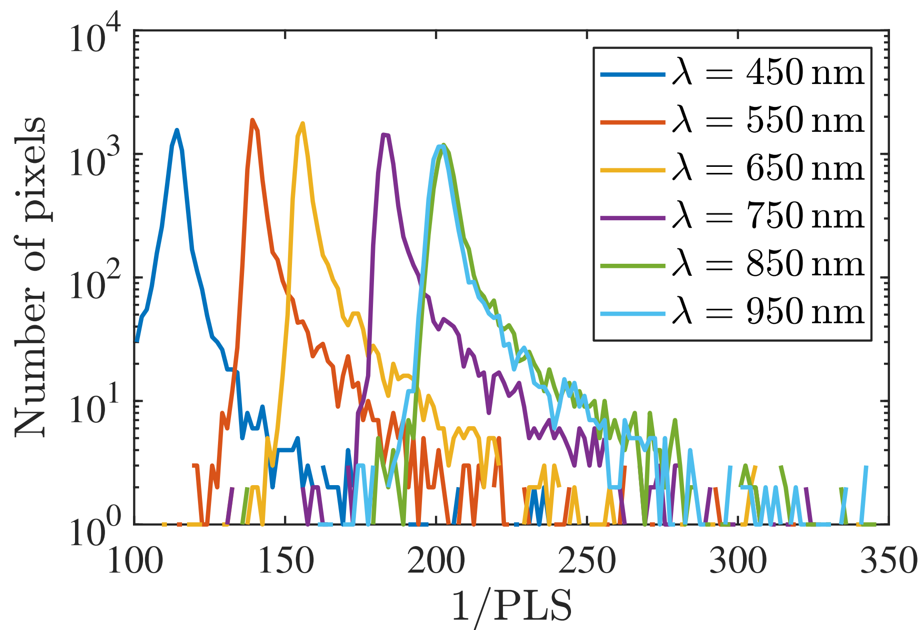


Figure 4.9: Distribution of Parasitic Light Hardness (1/PLS) as function of impinging wavelength, resulting from the measurements of the 5T Global Shutter CMOS Image Sensors.

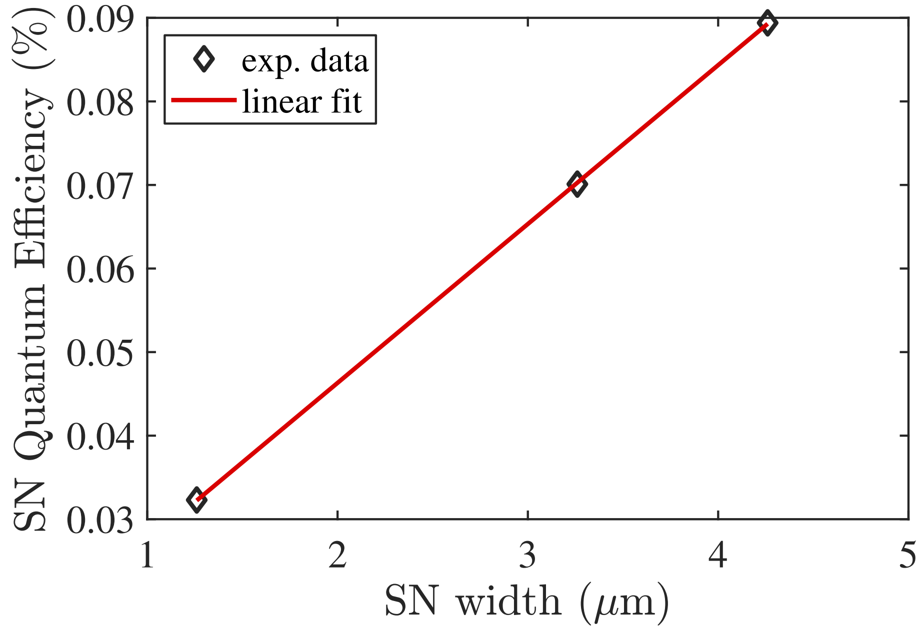


Figure 4.10: Display of the linear relation between the increase in the Storage Node width and the increase in the Storage Node Quantum Efficiency. Measurements have been performed at $\lambda = 650\,\text{nm}$.

4.2.1 Impact of Storage Node sizing

In order to evaluate the impact of the Storage Node dimensions, 3 different structures have been designed and measured. All 3 structures share the same layout, similarly to the one presented in Fig. 4.7, with the only difference being in the width of the Storage Node, shown in Fig. 4.7 as y_{SN}. The STI opening has been therefore tailored to accommodate the desired Storage Node width. A summary of the different structures performances is presented in table 4.1, for a wavelength of 650 nm. As expected, a larger Storage Node width corresponds to a higher mean Storage Node Quantum Efficiency. Though PhotoDiode shape and dimensions have been kept constant throughout the 3 structures, the PhotoDiode Quantum Efficiency slightly decreases at larger Storage Node width; this is probably due to the fact that a larger Storage Node "steals" some charges that would otherwise be collected by the PhotoDiode. As expected from the combination of PhotoDiode and Storage Node Quantum Efficiency, the Parasitic Light Hardness (1/PLS) decreases at larger Storage Node width.

Let us take a closer look to the relative variation of PhotoDiode and Storage Node Quantum Efficiency as well as Parasitic Light Hardness (1/PLS) as function of the Storage Node width, as depicted in table 4.2. There is one main outcome that needs to be pointed out: differently from what expected, the Storage Node Quantum Efficiency does not increase at the same rate as the increase in the Storage Node width, though still being linearly dependent, as shown by Fig. 4.10. This shows that the geometry correction factor presented in the modeling section, sec.2.6, has to be weighted by the slope of the linear regression shown in

SN width (µm)	PD QE (%)	SN QE (%)	1/PLS
1.26	20.0	0.03	620
3.26	19.4	0.07	276
4.26	19.1	0.09	215

Table 4.1: PhotoDiode Quantum Efficiency, Storage Node Quantum Efficiency and Parasitic Light Hardness (1/PLS) experimental results as function of the increase in the Storage Node width. Measurements have been performed at $\lambda = 650\,\text{nm}$.

Fig. 4.10 (approximately 0.427), in order to properly reproduce the 3D behavior.

SN width (µm)	SN width incr. (%)	PD QE incr. (%)	SN QE incr. (%)	1/PLS incr. (%)
1.26	REF	REF	REF	REF
3.26	159	-3	117	-55
4.26	238	-4	177	-65

Table 4.2: Increase in the PhotoDiode Quantum Efficiency, Storage Node Quantum Efficiency and Parasitic Light Hardness (1/PLS) as function of the Storage Node width. To estimate the impact of the Storage Node dimensions on the pixel performances, these values are correlated with the increase in the Storage Node width. Measurements have been performed at $\lambda = 650\,\text{nm}$.

Reasons behind this phenomenon can be found at different levels. From an optical point of view, the electric field distribution at the SiO_2 interface is not constant as one may expect. This has been shown previously in Fig. 3.5 exploiting 3D FDTD simulations. As an example, a particular electric field distribution pattern can be appreciated when taking a closer look to the PhotoDiode area. The pattern is the result of the often cited diffraction phenomena. Similarly, a space-variant optical generation in the Storage Node area is visible as well, due to light diffracting on the various metal interconnections and shields. A 2D simulation will not be able to reproduce the diffraction effect coming from the third dimensions, thus underestimating or overestimating the charge generation when the geometry correction factor is applied. From a transport phenomena point of view, charges generation is not uniform throughout the whole pixel and thus charge diffusion towards the nodes. An increase in size may not directly correspond in an equivalent increase in collected diffusing charges.

4.2.2 Choice of shielding metal layers

During sec. 3.3.1 we have shown the importance in the choice of shielding metal layers through use of the model developed. An appropriate choice of the shielding metal layer is especially needed when no specific optical shielding layers are available, as for example the WBLS, in the chosen technology.

Simulations have shown that the use of the lowest possible metal level for shielding purpose gives a higher advantage in terms of Parasitic Light Sensitivity improvement. Notably,

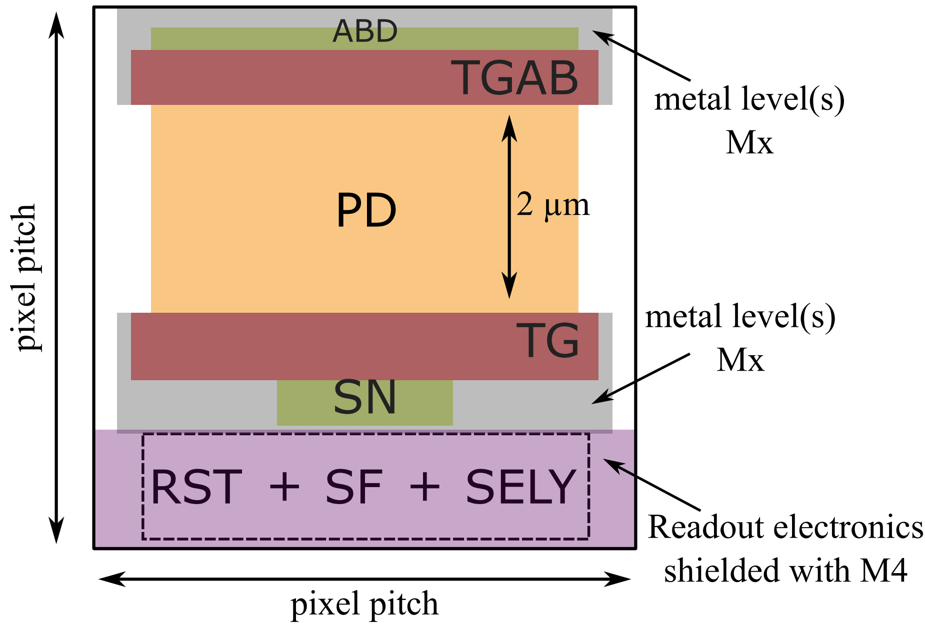
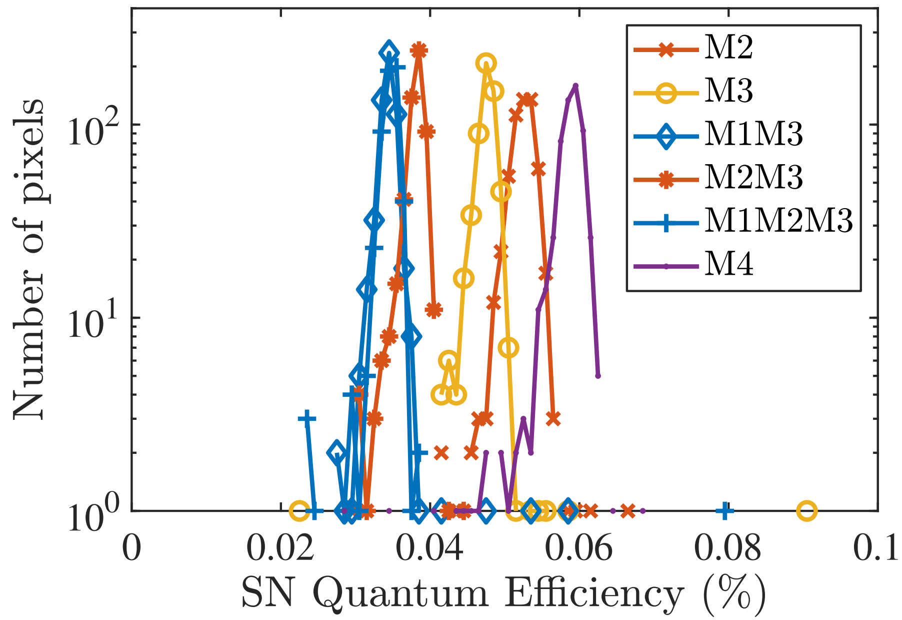


Figure 4.11: Pixel layout example of the test structures developed to measure Parasitic Light Sensitivity as function of the shielding metal levels. One or more metal levels are placed to shield the Storage Node and the TG, as well as the AB and its TGAB, leaving an aperture of 2 µm right above the PhotoDiode. In order to suppress any optical generation diffusing from the readout electronics region, a shielding metal level (M4) has been placed on top of this region.

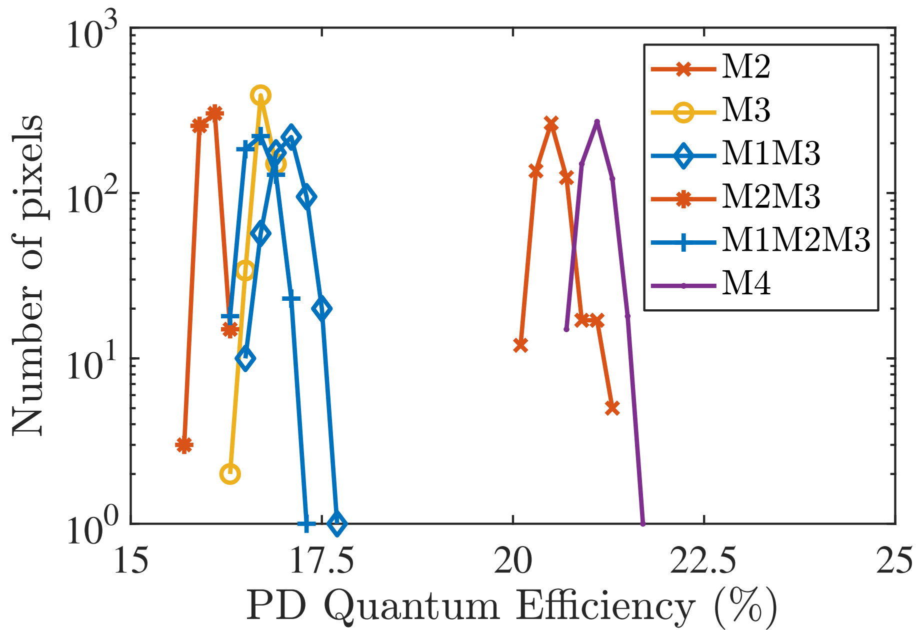
it has been shown that, even when using multiple metal levels for shielding purposes, the Parasitic Light Sensitivity performances are primary determined by the lowest metal level of the combination.

We have therefore developed different test structures to experimentally verify the assumptions given by the simulations. Fig. 4.11 shows a layout schematic of the designed test structures. Leaving an aperture of 2 µm right above the PhotoDiode, one or more metal levels have been placed to cover both the Storage Node and TG region and the AB and TGAB region. The metal level(s) exploited to cover the two regions are the same per each structure; multiple structures with different metal shielding levels have been designed. In order to ensure that the light is only allowed to enter the silicon in the PhotoDiode region, a shielding metal layer (level M4) has been exploited to cover the readout electronics region; this allows to accurately measure the impact of the different shielding levels, reducing parasitic light impinging from undesired regions.

A 192×256 7 µm pixel array has been designed and measurement for the previously state purpose. Different test structures have been placed in sub-regions of 32×32 pixels. Nevertheless, due to some complications in the development and constraints in the array size, it has not been feasible to integrate all the possible variations of the shielding metal levels combination; experimental results will therefore present a reduced subset of the shielding



(a)



(b)

Figure 4.12: Distribution of the (a) Storage Node and (b) PhotoDiode Quantum Efficiency at $\lambda = 650\,\mathrm{nm}$ for structures exploiting different metal levels to shield the Storage Node. Blue, red, yellow and violet represents structures exploiting respectively M1, M2, M3 and M4 as the lower metal shielding level.

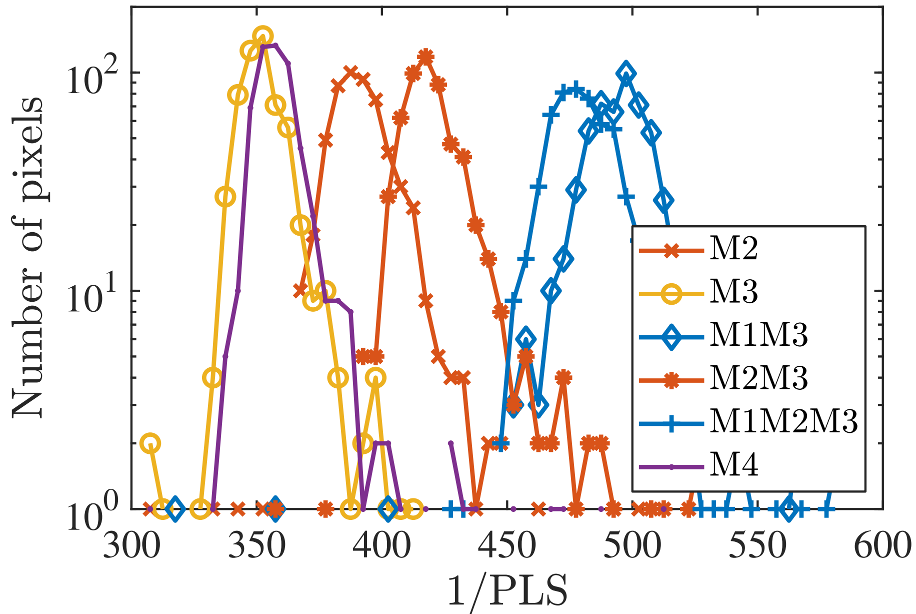


Figure 4.13: Distribution of Parasitic Light Hardness (1/PLS) at $\lambda = 650\,\text{nm}$ for structures exploiting different metal levels to shield the Storage Node. Blue, red, yellow and violet represents structures exploiting respectively M1, M2, M3 and M4 as the lower metal shielding level.

metal levels combinations.

Fig. 4.12a shows the experimental results of the Storage Node Quantum Efficiency on 5 different metal shielding levels combinations: M2, M3, M1+M3, M2+M3, M1+M2+M3 and M4. Measurements have been performed at different wavelengths, and present similar results. For simplicity, we show results at a wavelength of $\lambda = 650\,\text{nm}$; a histogram representation allows a better understanding of the sub-region performances. Different colors have been exploited to highlight the different structures and categorize them in subsets: the blue color represents the structures having M1 as the lowest shielding metal level, the red color represents the structures having M2 as the lowest shielding metal level, the yellow color represents the structures having M3 as the lowest shielding metal level and the violet color represents the structures having M4 as the lowest shielding metal level. As expected, the lower the shielding metal level, the lower the Storage Node Quantum Efficiency. The only exception to this rule is presented by the structure M2, where the Storage Node Quantum Efficiency seems to be higher than the structure M3 and right behind the structure M4; the reason behind this behavior remains unclear, though it can be noticed from Fig. 4.12b that the PhotoDiode Quantum Efficiency of the M2 structures appears higher as well.

Due to the apparent higher general sensitivity of the M2 structure, it is nevertheless expected that the Parasitic Light Sensitivity test results will follow the rule of the lowest shielding metal level. Fig. 4.13 shows the experimental results of the Parasitic Light Sensitivity

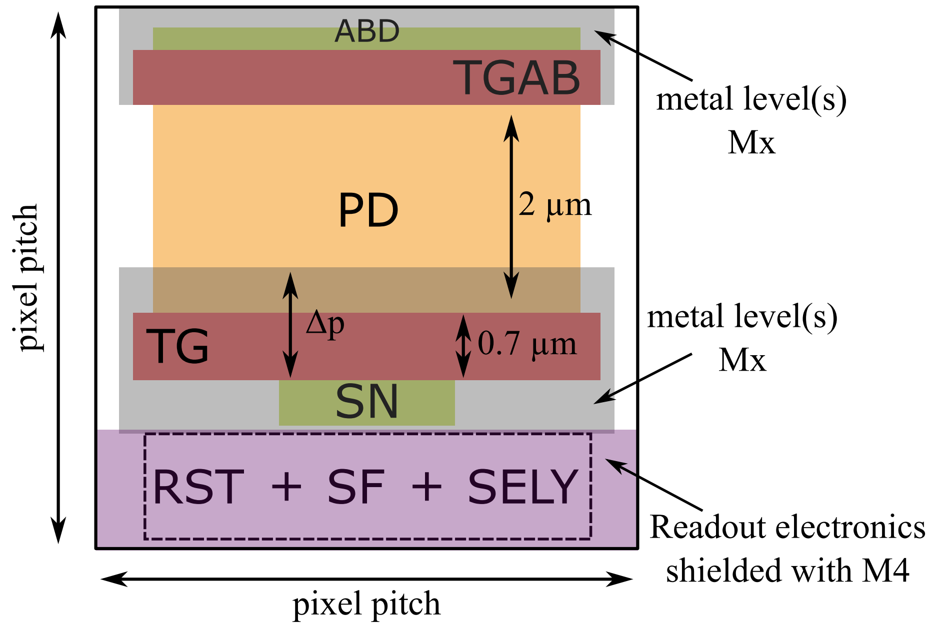


Figure 4.14: Pixel layout example of the test structures developed to measure Parasitic Light Sensitivity as function of the shielding metal positioning. One or more metal levels are placed to shield the Storage Node and the TG, as well as the AB and its TGAB. Δp defines the distance between the top border of the shielding metal layer(s) and the top border of the Storage Node. In order to suppress any optical generation diffusing from the readout electronics region, a shielding metal level (M4) has been placed on top of this region.

per each different structure. As expected, the results follow the lowest shielding metal level rule, thus validating the simulations previously presented and proving experimentally that diffraction is a crucial phenomenon to take into account when shielding of the Storage Node is required.

4.2.3 Positioning and sizing shielding metal layers

Similarly to what developed in the previous section, we aim to experimentally prove the results presented in sec. 3.3.2, where the positioning of the shielding metal layer with respect to the Storage Node is taken into account. Fig. 4.14 shows the basic layout schematic on which test structures have been designed; each structure has the same layout, except for the metal level shielding the Storage Node. Of each metal level, different Δp have been proposed. Each structure has been integrated in a 32×32 sub-region of the 192×256 7 µm pixel array.

Decreasing the size of the aperture above the PhotoDiode, we expect a reduction of both the PhotoDiode and Storage Node Quantum Efficiency; moreover, it is expected that Storage Node Quantum Efficiency is further reduced thanks to the fact that diffracting light will less and less impinging onto the SiO_2 of the Storage Node area. Fig. 4.15 indeed shows the decrease in the Quantum Efficiency of both PhotoDiode and Storage Node, for a structure exploiting

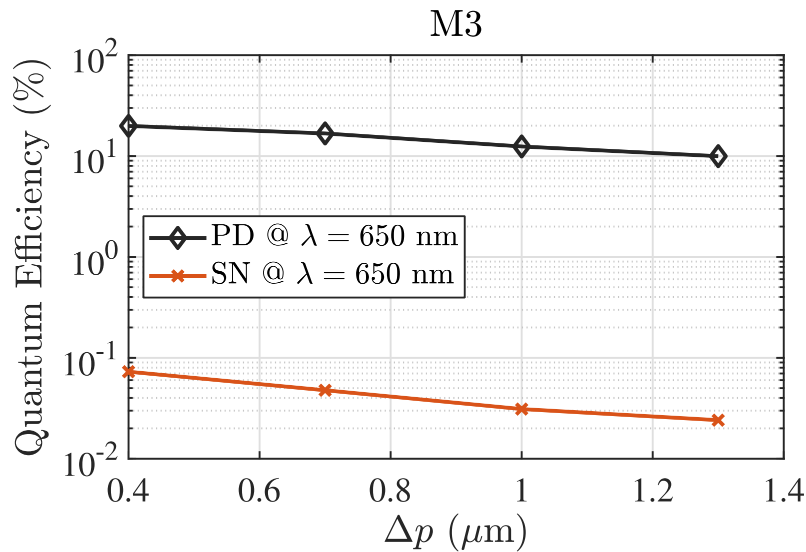


Figure 4.15: Decrease in the PhotoDiode and Storage Node Quantum Efficiency at as function of the parameter Δp representing the distance from the top edge of the shielding metal layer and the top edge of the Storage Node region. An increase in Δp means a reduction in the aperture above the PhotoDiode, thus leading to Quantum Efficiency reduction. Measurements have been conducted on a structure using M3 as the shielding metal level and at a wavelength of $\lambda = 650\,\text{nm}$.

M3 as the shielding metal level, as Δp increases. The Storage Node displays an increasingly small Quantum Efficiency, fraction of percentage, thus its precise measurement is difficult

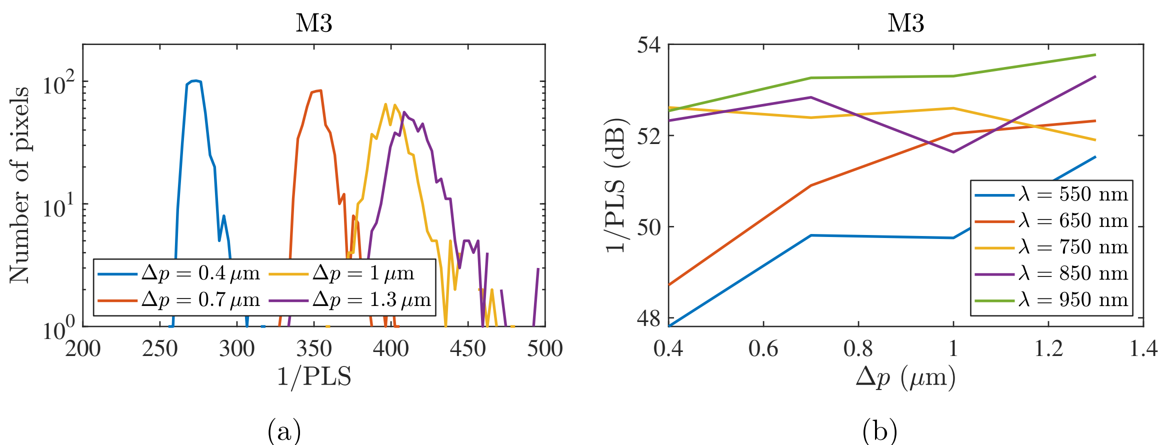


Figure 4.16: (a) Parasitic Light Sensitivity distribution as function of the distance between the top edge of the shielding metal layer and the top edge of the Storage Node (Δp) at $\lambda = 650\,\text{nm}$; (b) mean Parasitic Light Sensitivity (in dB) as function of Δp at different impinging wavelengths.

to be achieved. This results in a noisy Parasitic Light Sensitivity distribution, as shown in Fig. 4.16. A general increase in the Parasitic Light Hardness (1/PLS) characteristic with the shrinking of the aperture over the PhotoDiode area can be appreciated from Fig. 4.16b for different impinging wavelengths, except for $\lambda = 750\,\text{nm}$ where it seems to remain more or less constant. Improvement of the Parasitic Light Hardness (1/PLS) performance appear evident at shorter wavelengths ($\lambda = 550 - 650\,\text{nm}$), while it is smoothed out for longer wavelengths ($\lambda \geq 750\,\text{nm}$); this can be easily understood since shorter wavelengths generate a higher charge density at a shallower depth, thus the direct impinging light onto the Storage Node area results having an important impact.

Similar studies have been performed on structures exploiting M1 or M2 as the shielding metal level; results display a similar behavior in the Parasitic Light Sensitivity performances.

Usage of a "wider" metal shield coverage, i.e. positioning the metallic light shield beyond the boundaries of the Storage Node, is suggested when the image sensor has to be operated in the visible wavelength range. Having as a side effect the reduction of the PhotoDiode Quantum Efficiency, the amount of coverage must be chosen accordingly. On the other hand, if the image sensor is developed to operate in the NIR region, wider coverage of the Storage Node is not suggested.

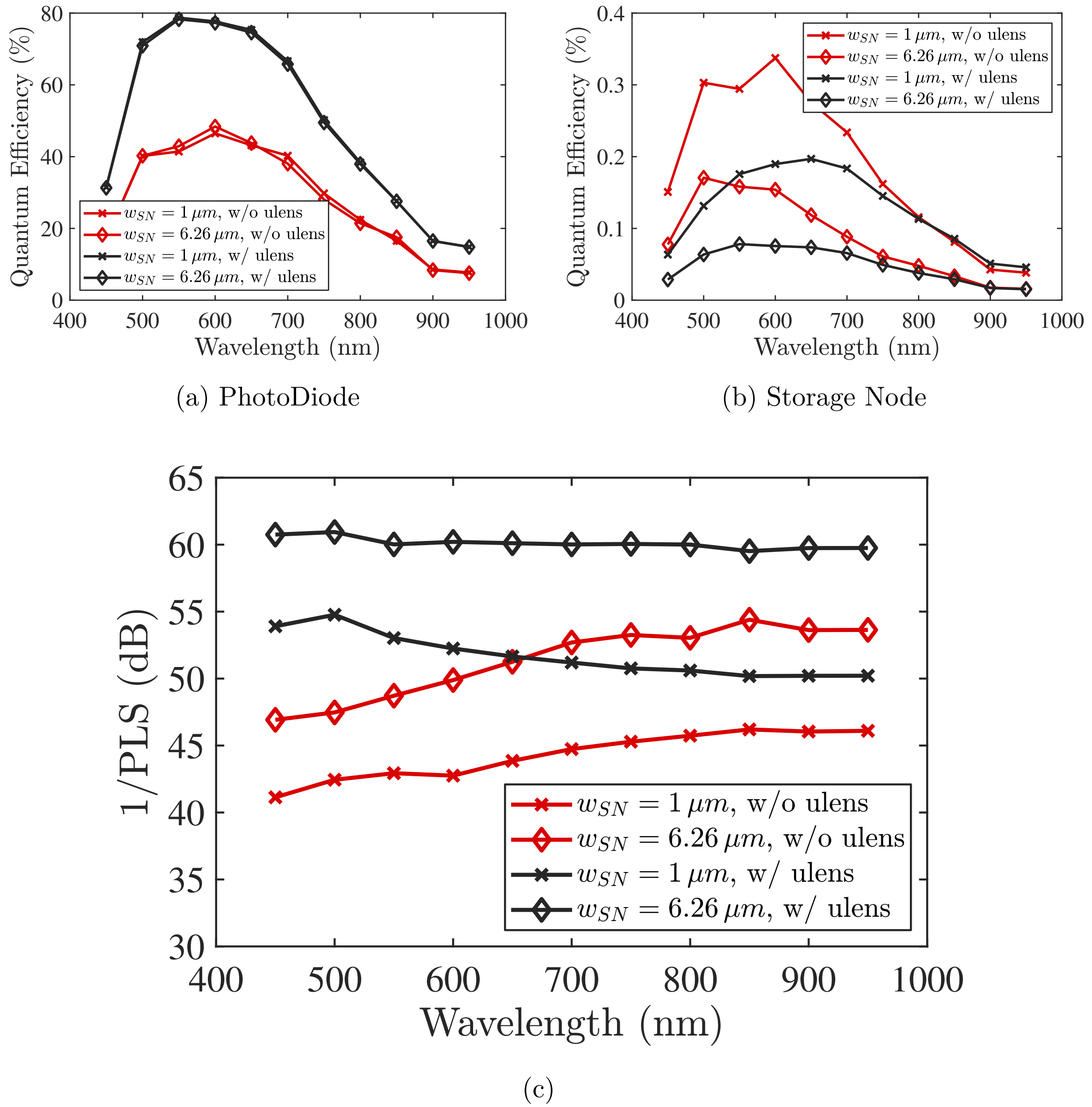


Figure 4.17: Experimental results of (a) PhotoDiode Quantum Efficiency, (b) Storage Node Quantum Efficiency and (c) Parasitic Light Sensitivity for four different structures. The black curves represent structures integrating a micro-lens, the red curves represent structures without the integration of a micro-lens. The cross marker curves represent structures having Storage Node width equal to 1 µm, the diamond marker curves represent structures having Storage Node width equal to 6.26 µm.

4.2.4 Impact of micro-lens presence

Finally, we would like to analyze the impact that the presence of a micro-lens has on the Parasitic Light Sensitivity performances of a Global Shutter CMOS Image Sensors. Due to

design and fabrication issues, only two Global Shutter pixel structures integrating micro-lens have been available for testing. The two Global Shutter pixels are differentiated by the Storage Node width y_{SN}, respectively of 1 µm and 6.26 µm and whose layout was presented in Fig. 4.7, are designed. Two versions not integrating micro-lens are equally available for comparison.

Fig. 4.17 shows the results of Quantum Efficiency for both PhotoDiode and Storage Node as well as Parasitic Light Sensitivity as function of wavelength for four different pixel types: red lines represent pixels without micro-lens, black lines represent pixels with integrated micro-lens, cross marker lines represent pixel with Storage Node width of 1 µm and diamond marker lines represent pixels with Storage Node width of 6.26 µm. As expected and represented by Fig. 4.17a, PhotoDiode Quantum Efficiency is strongly affected by the presence of micro-lens and almost insensitive of the Storage Node dimensions. Conversely, as shown by Fig. 4.17b, Storage Node Quantum Efficiency is heavily affected by both the presence of micro-lens and Storage Node dimensions. It is nevertheless of interest to notice that the effect of micro-lens is smoothed out in the near-infrared region ($\lambda \geq 800\,\text{nm}$), especially for the Storage Node Quantum Efficiency; reason behind this behavior is the change of the micro-lens focus as function of the wavelength, resulting in a smaller focusing capacity of the micro-lens at longer wavelengths.

Let us take a closer look to Fig. 4.17c, notably at two curves: the structure having smaller Storage Node dimensions and no micro-lens and the structure having higher Storage Node dimensions and integrating a micro-lens. Expectations are that integrating a micro-lens would definitely increase the performances of the image sensor, especially concerning the Parasitic Light Sensitivity; conversely, it appears clearly that the efficiency of the micro-lens is restrained to the visible range ($400-650\,\text{nm}$). Again, Parasitic Light Sensitivity performances of a Global Shutter CMOS Image Sensors are dominated by two main phenomena: direct impinging light onto the Storage Node region and free photo-generated charge diffusion. The first one is more important at shorter wavelengths, thus optical improvements (i.e. reduction of diffraction, presence of micro-lens, etc.) are critical if the image sensor have to be operated in this region. Conversely, dimensions and front-end design are to be taken into account when dealing with longer wavelengths, where charge diffusion is the main contribution to Parasitic Light Sensitivity.

Following what given by sec. 3.4.1, the desire would have also been to design test structures having different micro-lens center positioning. Due to some design and fabrication issues, these structures could have not been tested. Therefore, statements presented in sec. 3.4.1 have to be confirmed by successive measurements.

4.3 Comforting simulations with experimental results

So far, we have used the 2D method for simulating Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors as a comparative tool to guide towards a better design. Following the simulation results, test structures have been developed and tested; experimental results have

proved moving in the same direction dictated by the simulations.

Hereafter, we would like to comfort the 2D simulation results that have been obtained in chapter 3 with the experimental results withdrawn from the designed test structures. In a first step, Parasitic Light Sensitivity performances will be compared; consequently, Quantum Efficiency for both PhotoDiode and Storage Node will be presented.

Two test structures have been modeled and simulated; both structures are 5T 7 µm pitch Global Shutter pixels, similar to the one presented in Fig. 4.7, integrating a PhotoDiode, a TG, an Floating Diffusion exploited as Storage Node, a TGAB with its ABD and the readout electronics (RST, SF and SELY transistors). The only difference between the two structures is the Storage Node width; structure *REF* has an Storage Node width equal to 6.26 µm, structure *VAR* has an Storage Node width equal to 1 µm. The two structures have been fabricated with a commercially available 0.18 µm CMOS Image Sensor process.

Due to limited knowledge in the BEOL process, the pixel model used for the FDTD simulations may present some discrepancies with the actual behavior of the real pixel.

4.3.1 Modeling Parasitic Light Sensitivity of a real CMOS Image Sensor

We have seen in sec. 4.2.1 that the Quantum Efficiency does not increase at the same rate as the Storage Node width, which would be expected in case the Storage Node width results as a multiplicative constant, as stated by the expression given in (2.57) that we briefly recall hereafter for the Storage Node case

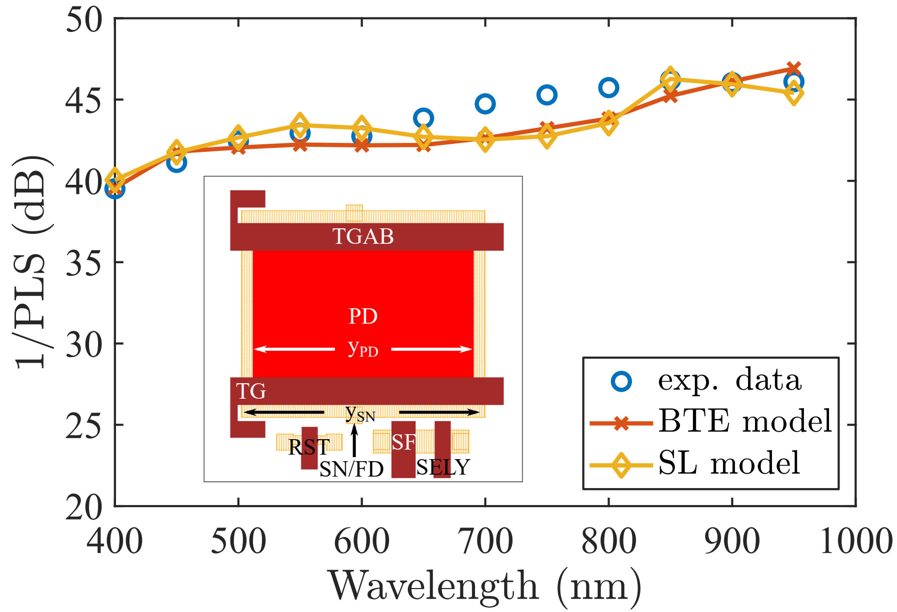
$$\begin{aligned} QE_{SN} &= \frac{\iiint G_{opt}(x,y,z)\cdot W_{SN}(x,y,z)\cdot dV}{\iint \Re\{\vec{S}_{source}\}\cdot d\Sigma} \\ &= \frac{y_{SN}\ \iint G_{opt}(x,z)\cdot W_{SN}(x,z)\cdot dxdz}{p\int \Re\{\vec{S}_{source}\}\cdot dx}. \end{aligned} \tag{4.3}$$

Therefore, the geometrical correction factor presented in the simulated Quantum Efficiency expression has been slightly modified to adjust the result. The coefficient y_{SN} has been substituted with the linear regression shown by Fig. 4.10;

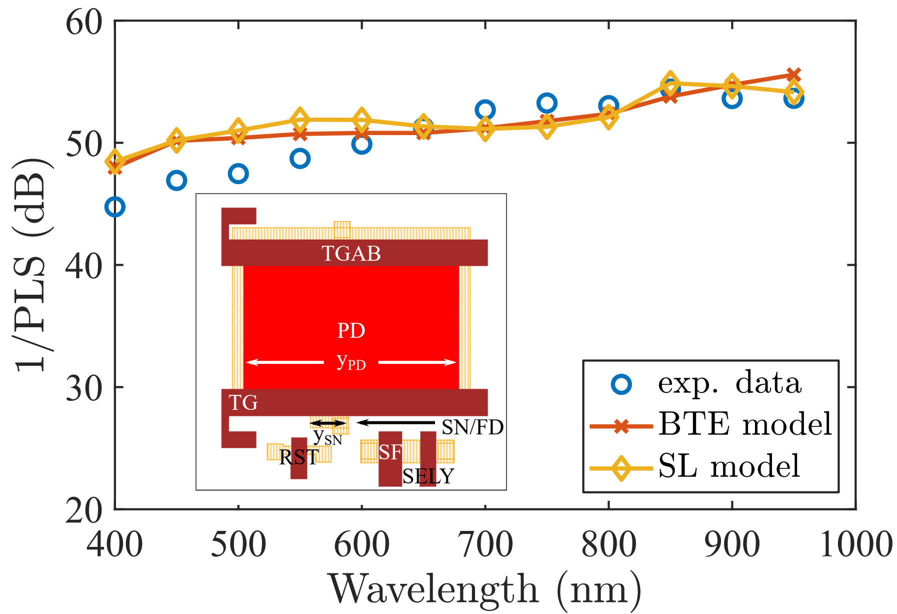
Similarly for the PhotoDiode, we suppose that the PhotoDiode Quantum Efficiency increase linearly with y_{PD} but not with the same rate. No structures with different PhotoDiode width were available so no measurements could have been performed. y_{PD} has therefore been adjusted in order to fit the experimental data and it is not retrieved by measurements on different PhotoDiode widths.

Fig. 4.18 present the Parasitic Light Hardness (1/PLS) modeling as function of wavelength of both structured REF and VAR. Given that both structures have an identical PhotoDiode, the same coefficient has been used in calculating PhotoDiode Quantum Efficiency. The simulations reproduce a similar behavior compared to the experimental one in both cases, though underestimating around 700 nm for the REF structure and overestimating at

shorter wavelengths for the VAR structure. Fluctuations and errors in the Parasitic Light Hardness (1/PLS) modeling can be understood given the important impact that the Storage Node Quantum Efficiency modeling has, being the denominator of the fraction; a small variation of the latter may cause an important variation of the modeled Parasitic Light Hardness (1/PLS). Moreover, the simplistic approach exploited either to built the electric field map, for the Boltzmann Transport Equation model, or the Straight Line model (see sec. 2.4) may lead to imperfections on the estimation of the Collection Probability weighting function and result in estimation errors of the overall Parasitic Light Hardness (1/PLS). Nevertheless, the Parasitic Light Hardness (1/PLS) behavior as function of wavelength seems to be reproduced for both cases.



(a) REF



(b) VAR

Figure 4.18: Modeling of Parasitic Light Hardness (1/PLS) of real Global Shutter CMOS Image Sensors with the use of both developed models as function of wavelength. Blue circles represent the experimental data; red cross curves represent the Boltzmann Transport Equation model; yellow diamond curves represent the Straight Line model. (a) shows modeling of Parasitic Light Hardness (1/PLS) for the REF structure, whose layout is shown at the bottom left corner; (b) shows modeling of Parasitic Light Hardness (1/PLS) for the VAR structure, whose layout is shown at the bottom left corner.

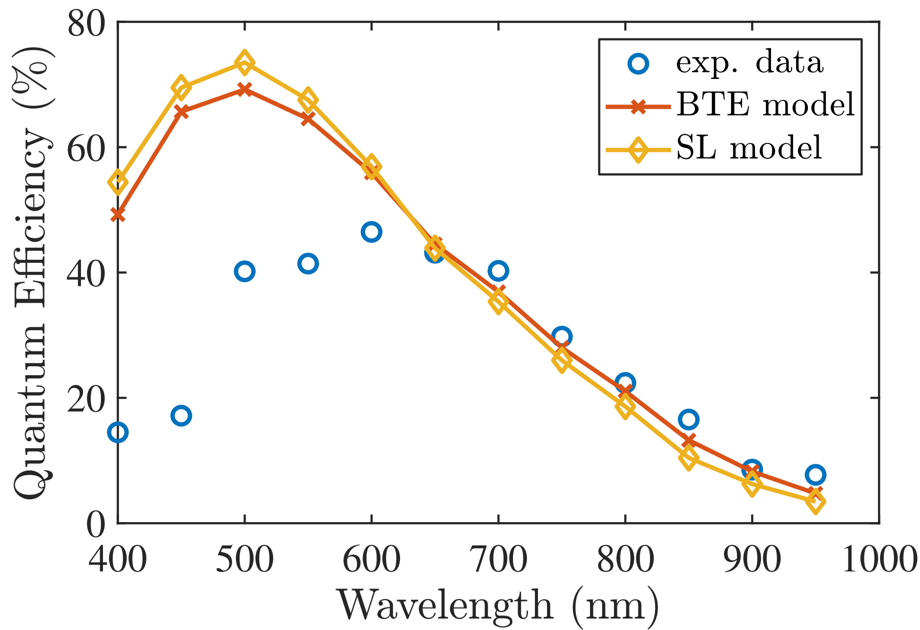
4.3.2 Modeling Quantum Efficiency of a real CMOS Image Sensor

It is now important to take a closer look to the Quantum Efficiency modeling for both PhotoDiode and Storage Node; for this purpose, only the REF structure will be analyzed. Fig. 4.19 shows modeling of the (a) PhotoDiode and (b) Storage Node Quantum Efficiency as function of wavelength, using both Boltzmann Transport Equation and Straight Line model. Quantum Efficiency behavior is not accurately reproduced for both PhotoDiode and Storage Node, especially at shorter wavelengths. The accuracy of the model seems to be increased when going towards longer wavelengths. Inaccuracy of the Quantum Efficiency modeling is probably due to lack of knowledge in the BEOL process. Anti-Reflection (AR) coating not been included, wavelength-independent refractive index of the oxides (Pre-Metal Dielectric and Inter-Layer Dieletric) can play important role in accurately modeling the number of photons impinging onto the SiO_2 surface.

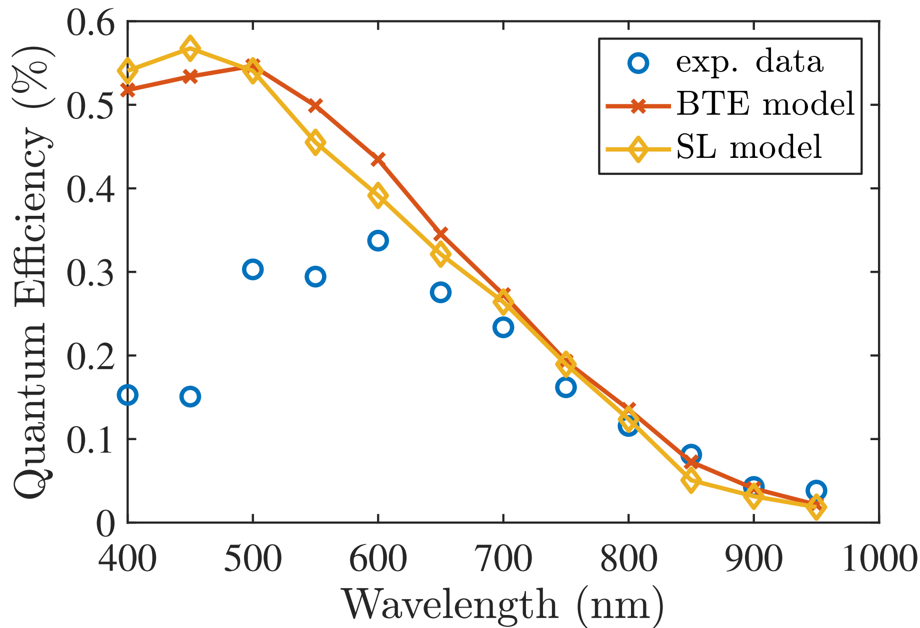
In order to prove this last statement, one further simulation of the real pixel has been performed, replacing the constant refractive index oxide with a wavelength-dependent refractive index oxide. Notably, BoroPhosphoSilicate Glass (BPSG) and FluoroSilicate Glass (FSG) refractive index models have been retrieved [Ref] and exploited to model respectively the Pre-Metal Dielectric and the Inter-Layer Dieletric. Though the retrieved models may not represent the actual behavior of the deposited oxides during the fabrication process, since they have been taken from optical lenses database, they can still be useful to appreciate their impact on optical simulations. Both BPSG and FSG refractive indexes show an important absorption (refractive index imaginary part) around at shorter wavelengths (400 to 500 nm) and a slowly varying real part.

Fig. 4.20 shows the impact of the presence of the modeled BoroPhosphoSilicate Glass and FluoroSilicate Glass when estimating (a) the PhotoDiode Quantum Efficiency and (b) the Storage Node Quantum Efficiency. The presence of a refractive-index varying material modifies the shape of the modeled PhotoDiode Quantum Efficiency; peak Quantum Efficiency is shifted from 500 nm to 550 nm and the overestimation of the Quantum Efficiency value in the visible wavelength region is now contained. A more pronounced decrease in the Storage Node Quantum Efficiency is visible at longer wavelength as well as an overall decrease of the Quantum Efficiency. On the other hand, it can be seen from (c) how the Parasitic Light Hardness (1/PLS) has remained similar to what previously presented, following the behavior of the experimental data. The presence of wavelength-dependent refractive index oxides equally impacts the PhotoDiode and Storage Node Quantum Efficiency, thus canceling out at the ratio.

It has been shown how the developed model can be extremely sensitive to modeling of the BEOL, especially regarding the Quantum Efficiency. Being the Parasitic Light Hardness (1/PLS) computed as a ratio, the uncertainties of the BEOL model may sometimes cancel out, as seen with the wavelength-dependent refractive index of the oxide. Nevertheless, for a better modeling accuracy, a precise modeling of the BEOL is required.

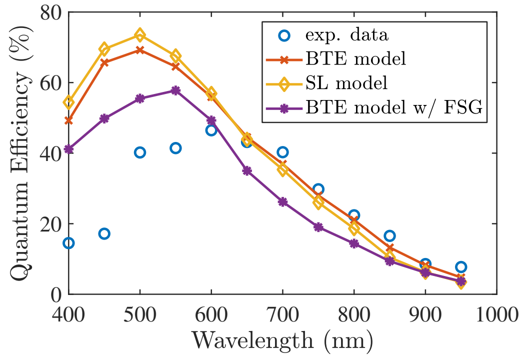


(a) PhotoDiode

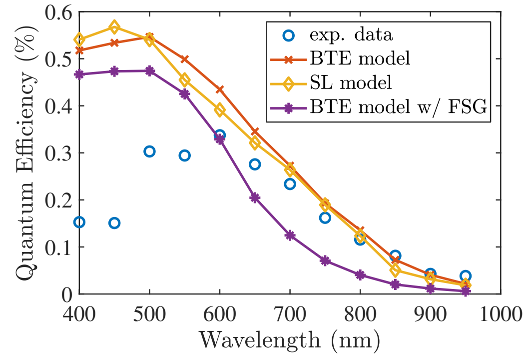


(b) Storage Node

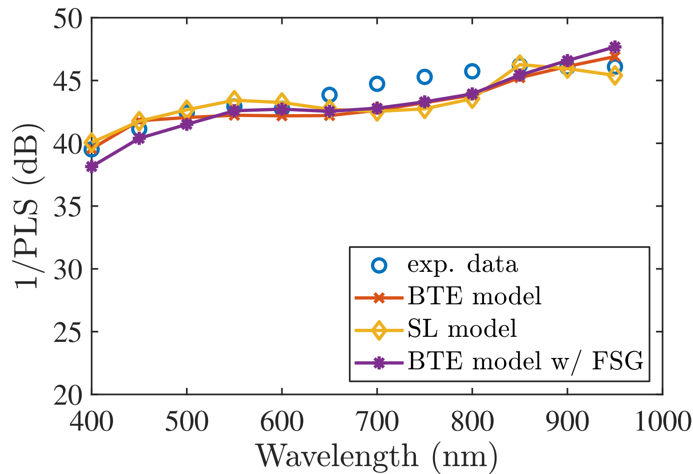
Figure 4.19: Modeling of Quantum Efficiency of real Global Shutter CMOS Image Sensors with the use of both developed models as function of wavelength. Blue circles represent the experimental data; red cross curves represent the Boltzmann Transport Equation model; yellow diamond curves represent the Straight Line model. (a) shows modeling of PhotoDiode Quantum Efficiency for the REF structure, whose layout is shown at the bottom left corner; (b) shows modeling of Storage Node Quantum Efficiency for the REF structure, whose layout is shown at the bottom left corner.



(a) PhotoDiode Quantum Efficiency



(b) Storage Node Quantum Efficiency



(c) Parasitic Light Hardness (1/PLS)

Figure 4.20: Modeling of (a) PhotoDiode Quantum Efficiency, (b) Storage Node Quantum Efficiency and (c) Parasitic Light Hardness (1/PLS) of real Global Shutter CMOS Image Sensors with the use of both developed models with a wavelength independent oxide refractive index (red and yellow curve respectively for the Boltzmann Transport Equation and Straight Line model) and with a wavelength-dependent refractive index oxide, FluoroSilicate Glass (FSG), (purple curve, only Boltzmann Transport Equation model). Blue circles represent the experimental data.

4.4 Development of methods for mitigating Parasitic Light Sensitivity in a post-process fashion

So far, we have given a phenomenological understanding of the Parasitic Light Sensitivity, with the help of simulations, models and experimental data; this study helps in giving guidelines to improve the design and process fabrication of Global Shutter CMOS Image Sensors. We desire to bring the discussion a step up, leading to the understanding of the signal induced by the non-negligible Parasitic Light Sensitivity of the image sensor when operated in Global Shutter mode. A model of the Parasitic Light Sensitivity induced signal could help in developing a method for mitigating Parasitic Light Sensitivity in a post-process fashion.

Few studies can be found in literature on mitigation of Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors through post-process methods, despite resulting as an appealing low-cost solution. Two main studies have to be cited on this matter, one exploiting in-pixel consecutive multiple frame subtraction and requiring a triggered external laser source [Ge+19] and another presenting multi-frame temporal domain correction as well as single-frame spatial correction [SJI19]. For our discussion, the first paper will not be taken into account, due to the external source required. The second paper has been served as a basis and a reference on which to build the different models that will be presented further on. In particular, the second paper presents an estimation of the parasitic light induced signal, though the measurement is performed non simultaneously with the readout operations. Our models aim to overcome this issue and present alternatives to measure the parasitic light induced signal during the actual readout phase.

This section therefore aims in developing a model of the image sensor output when operated in Global Shutter mode, thus allowing for the analysis and development of diverse post-process methods to mitigate Parasitic Light Sensitivity.

A post-process correction method aims in processing an acquired frame through use of an algorithm, often to enhance the quality of the acquired image, but not only. In our case, we aim in developing and analyzing post-process corrections methods to mitigate the appearance of an additional signal caused by the non-negligible Parasitic Light Sensitivity that characterize Global Shutter CMOS Image Sensors.

Before starting, it is important to give details on how Global Shutter CMOS Image Sensors are operated. Briefly presented in chapter 1, a Global Shutter CMOS Image Sensors can be operated in two Global Shutter modes: the Integrate Then Read and the Integrate While Read mode. Nowadays, the Integrate While Read mode is the preferred operating mode. We therefore aim to develop different corrections methods to be applied in the Integrate While Read mode.

Fig. 4.21 shows an example of the time diagram to operate Global Shutter CMOS Image Sensors in the Integrate While Read mode; the integration of frame N+1 starts during frame N readout and ends correspondingly. Frame N+1 readout starts soon after. The minimum frame rate is set by the frame readout time.

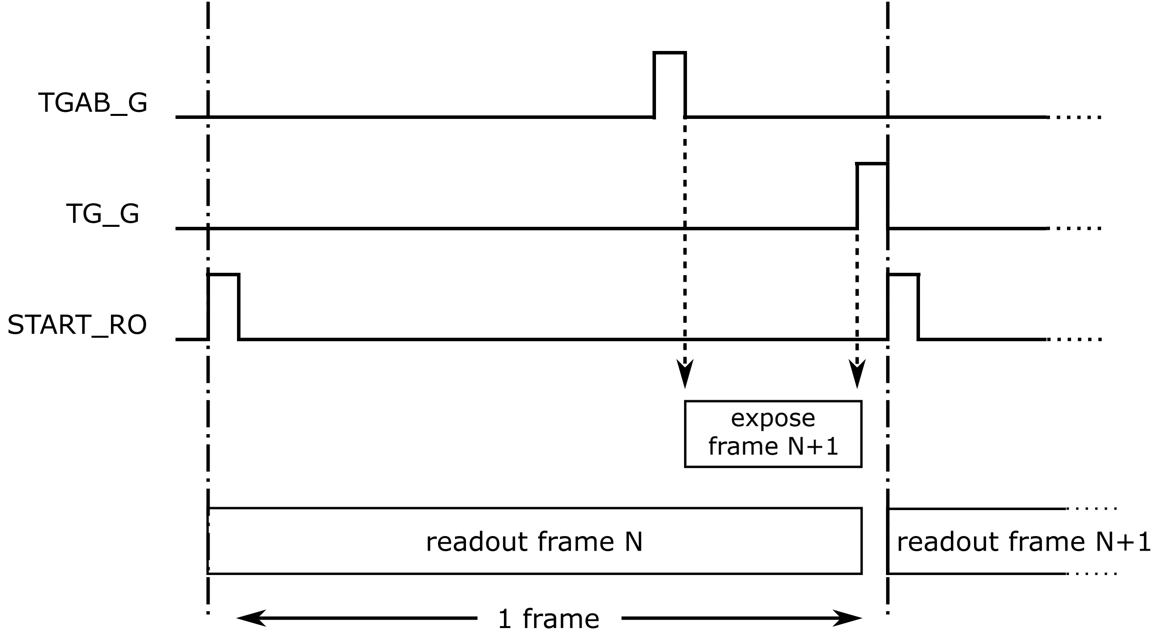


Figure 4.21: Time diagram of a Global Shutter CMOS Image Sensor operated in Integrate While Read (ITR) mode. TGAB_G command determines the beginning of the array integration phase, its end is set by command TG_G. Exposure of frame N is performed during readout of frame N+1. Readout phase starts with the help of the START_RO command. The frame length is determined by the length of readout phase.

4.4.1 Developing a method for modeling the output voltage of CMOS Image Sensors in Global Shutter mode

Before digging into post-process methods for mitigating Parasitic Light Sensitivity, it is important to develop an analytical model of the image sensor output when operated in Global Shutter mode. A definition of the image sensor output is therefore required; Fig. 4.22 shows an example of a generic Global Shutter pixel and its column readout. It can be clearly appreciated that $V_{out} = V_{REF} - V_{SIG}$, V_{REF} and V_{SIG} being respectively the voltages sampled and hold thanks to the SHR and SHS command for the dual sampling operation. TGAB_G and TG_G are the signals exploited to determine the start and stop of the array integration phase. In a first approximation, it is possible to model V_{out} for the $(i-th, j-th)$ pixel, with i and j being respectively the row and column number, as function of the number of electrons collected by the PhotoDiode, $N_{el_{PD}}$, and transferred to the Storage Node (supposing that all charges are successfully transferred) and the number of electrons collected by the Storage Node, $N_{el_{SN}}$, as given by

$$V_{out}(i,j) = A(i,j) \cdot [N_{el_{PD}}(i,j) + N_{el_{SN}}(i,j)] = V_{PD}(i,j) + V_{PLS}(i,j), \tag{4.4}$$

where $A(i,j)$ is a parameter containing the buffer gain (generally the gain of the SF) and the conversion gain; it is known that both conversion gain and SF gain may vary on a pixel-to-

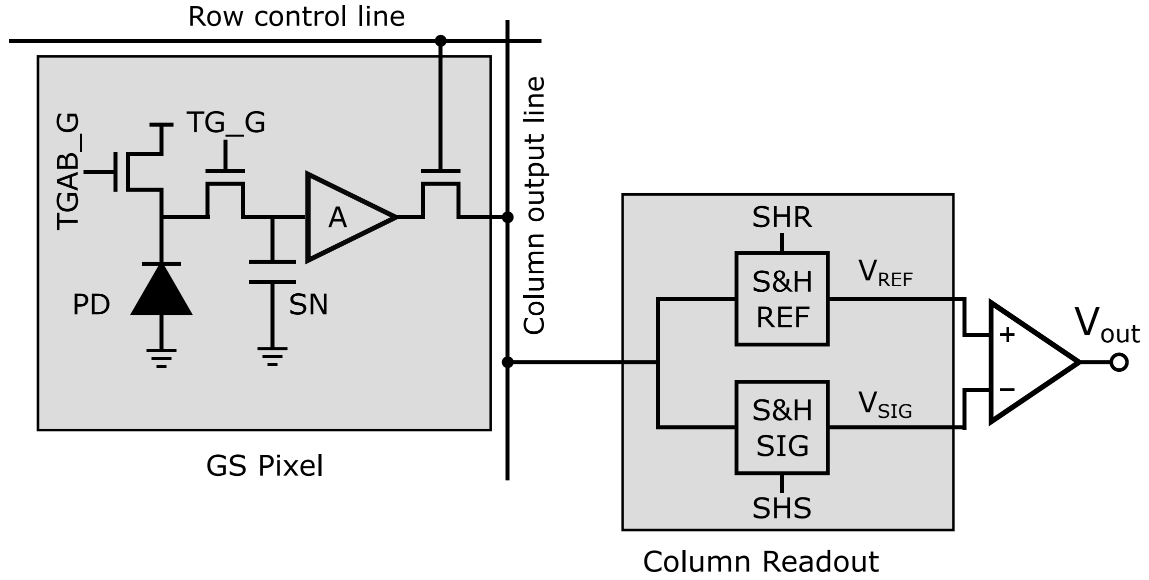


Figure 4.22: Schematics of a generic Global Shutter CMOS Image Sensors. The pixel consists of a PhotoDiode, represented by a reverse-biased diode, an in-pixel amplifier of gain A, a row selector transistor, an Storage Node and two transistors determining the integration start (TGAB_G) and stop (TG_G). The pixel output passes through the column output line reaching the column readout, where the pixel reference (V_{REF}) and signal V_{SIG} voltages are sampled and temporary stored in their respective Sample&Hold (S&H) exploiting the SHR and SHS command lines. The output signal V_{out} is the result of the difference between V_{REF} and V_{SIG}.

pixel basis, explaining the reason why the parameter has been indexed. We assume that the charges collected by the PhotoDiode alone would produce a voltage given by V_{PD} and the electrons collected by the Storage Node alone would produce a voltage given by V_{PLS}.

Let us first suppose that one frame is to be acquired, with an integration time of t_{int}; sequential readout operation requires separately readout of one row in a given time t_{rro}. Considering a time-invariant illumination of the image sensor, it is possible to define V_{PD} and V_{PLS} as given by Eqs. (4.5) and (4.6), where $\Gamma(i, j)$ represents the incoming photon rate per each pixel.

$$V_{PD}(i,j) = A(i,j) \cdot QE_{PD}(i,j) \cdot \Gamma(i,j) \cdot t_{int} \tag{4.5}$$

$$\begin{aligned} V_{PLS}(i,j) = & A(i,j) \cdot QE_{SN}(i,j) \cdot \Gamma(i,j) \cdot (i-1) \cdot t_{rro} + \\ & + A(i,j) \cdot DC_{SN} \cdot (i-1) \cdot t_{rro} \end{aligned} \tag{4.6}$$

It can be appreciated that Dark Current has been taken into account only for Storage Node (DC_{SN}), given that Global Shutter integration times are often very short and the Dark Current contribution of a pinned PhotoDiode is negligible. It has to be noticed that $V_{PLS}(1, j) = 0$; a reset operation is performed right before the end of the integration phase, thus suppressing all electrons acquired by the Storage Node during the integration period;

electrons contributing to V_{PLS} are therefore collected only during the readout phase. Readout of the second row is performed after the readout of the first row; the storage time is therefore equivalent to the readout time of the previous row. This scheme carries on for the entire array, thus explaining the $(i-1)$ factor in front of t_{rro}.

Definition of V_{PLS} as function of V_{PD} is possible through the following

$$\begin{aligned} V_{PLS}(i,j) = V_{PD}(i,j) \cdot PLS(i,j) \cdot \frac{(i-1)\cdot t_{rro}}{t_{int}} + \\ + A(i,j) \cdot DC_{SN}(i,j) \cdot (i-1) \cdot t_{rro}. \end{aligned} \tag{4.7}$$

The output signal can be finally resumed as:

$$\begin{aligned} V_{out}(i,j) = V_{PD}(i,j) \cdot \left[1 + PLS(i,j) \cdot \frac{(i-1)\cdot t_{rro}}{t_{int}}\right] + \\ + A(i,j) \cdot DC_{SN}(i,j) \cdot (i-1) \cdot t_{rro}, \end{aligned} \tag{4.8}$$

where $(i-1)\cdot t_{rro}$ represents the *i-th* row Storage Node storage time.

In order to ensure the validity of (4.8), measurements have been performed on a Global Shutter CMOS Image Sensors with 5T pixels at a fixed wavelength of $\lambda = 650\,\text{nm}$. Notably, to appreciate variations in the row-by-row output, low Parasitic Light Sensitivity image sensor as well as long row storage time are required. Row storage time has been chosen to be 50 ms, due to equipment constraints. It is possible to exploit TGAB to increase the time at which the entire matrix is under light (i.e. the time during which the Storage Node is found in storage mode) while blocking the PhotoDiode collection avoiding blooming or overflow. Fig. 4.23 details the timing diagram for this particular measurement.

The image sensor has been exposed to time-invariant flat field illumination, $\Gamma(i,j) = \Gamma$, it is therefore supposed that V_{PD} is time and space-invariant. Moreover, Parasitic Light Sensitivity has been considered uniform throughout the array, comforted by results shown in Fig. 4.24, where 80% of the pixels Parasitic Light Sensitivity fall into a narrow band close to the mean value.

It is possible to differentiate Eq. 4.8 with respect to row number obtaining Eq. 4.9, thus showing a linear increase in the output signal as function of the row number at constant impinging photon rate.

$$\frac{\partial V_{out}(i,j)}{\partial i} = V_{PD} \cdot PLS \cdot \frac{t_{rro}}{t_{int}} + A \cdot DC_{SN}(i,j) \cdot t_{rro} \tag{4.9}$$

Consequently, knowing that the measurement can be performed at different luminous intensities, i.e. impinging photon rate, it is possible to differentiate Eq. (4.9) with respect to photon rate Γ, as shown in Eq. (4.10), again showing a linear behavior.

$$\frac{\partial}{\partial \Gamma}\left(\frac{\partial V_{out}(i,j)}{\partial i}\right) = A \cdot QE_{PD} \cdot PLS \cdot t_{rro} \tag{4.10}$$

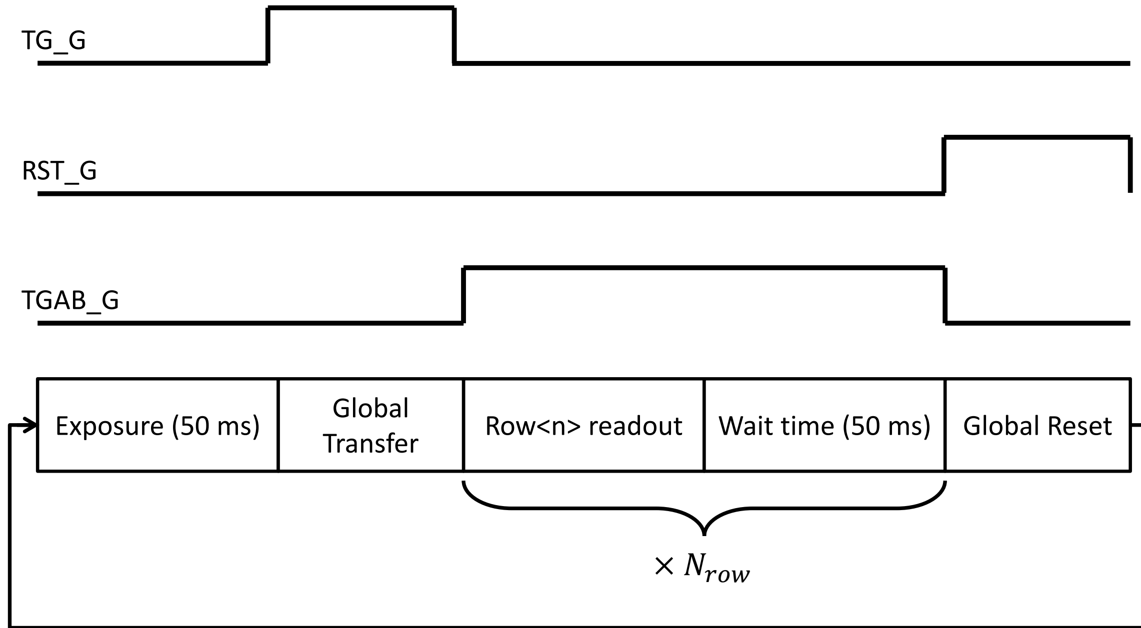


Figure 4.23: Time diagram used for validation measurement. Firstly, in order to operate the image sensor in normal conditions, an integration of 50 ms is performed and the charges integrated in the PhotoDiodes are globally transferred to the Storage Nodes after node reset. First row readout begins and then a waiting time is applied in order to achieve total row storage time of 50 ms. A long row storage time is required in order to appreciate the parasitic light induced signal at static conditions. This action is repeated for as many rows in the image sensor array. At the end of this procedure, a Global reset is performed and the cycle starts back again.

Fig. 4.25 represents the output signal as function of row number per different per-pixel incoming photon rates; V_{out} is actually the result of a spatial average on the columns. It can be appreciated that linear regression accurately fits all four measurements, thus confirming Eq. (4.9) and the assumption that the Storage Node parasitic signal is linearly dependent on row number. Furthermore, from Fig. 4.26 it is possible to appreciate that the slopes of linear regression previously performed are linearly related to incoming photon rate, confirming Eq. (4.10). Finally, Fig. 4.27 shows the output signal $\mathrm{V_{out}}$ of the array. The image has been taken at time-invariant flat-field illumination at $\lambda = 650\,\mathrm{nm}$ and the Dark Current contribution has been suppressed to allow appreciation of the Parasitic Light Sensitivity induced signal. The signal gradient as function of the row is evident, thus showing the impact of Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors. The dark blue spots represent hot pixel, i.e. pixels with such a high dark current bringing them to saturation.

In a first approximation, it is supposed light intensity is time-invariant. The output of

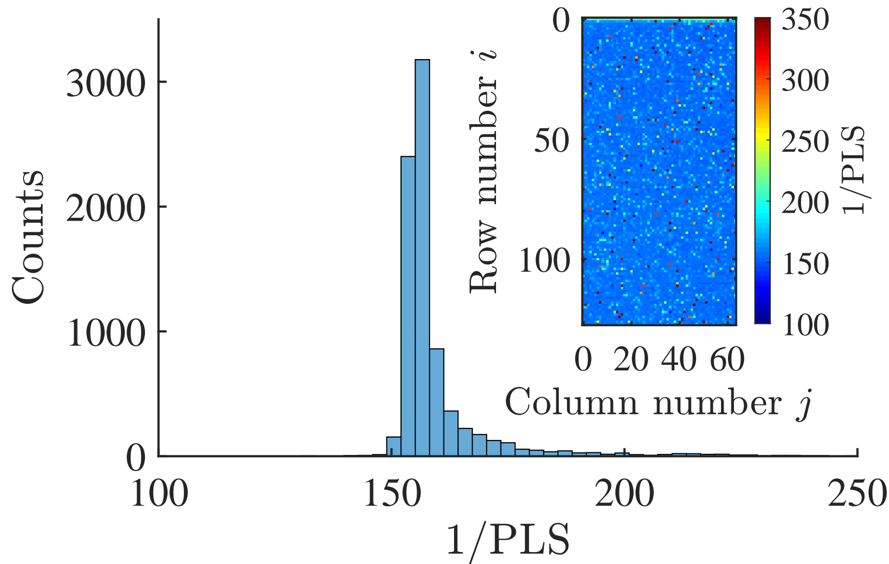


Figure 4.24: Distribution of the per-pixel Parasitic Light Hardness (1/PLS) at a wavelength of $\lambda = 650\,\text{nm}$ for the Global Shutter CMOS Image Sensors exploited for the analysis. The top-right plot aims to display the per-pixel Parasitic Light Hardness (1/PLS) non-uniformity where each square represents one pixel.

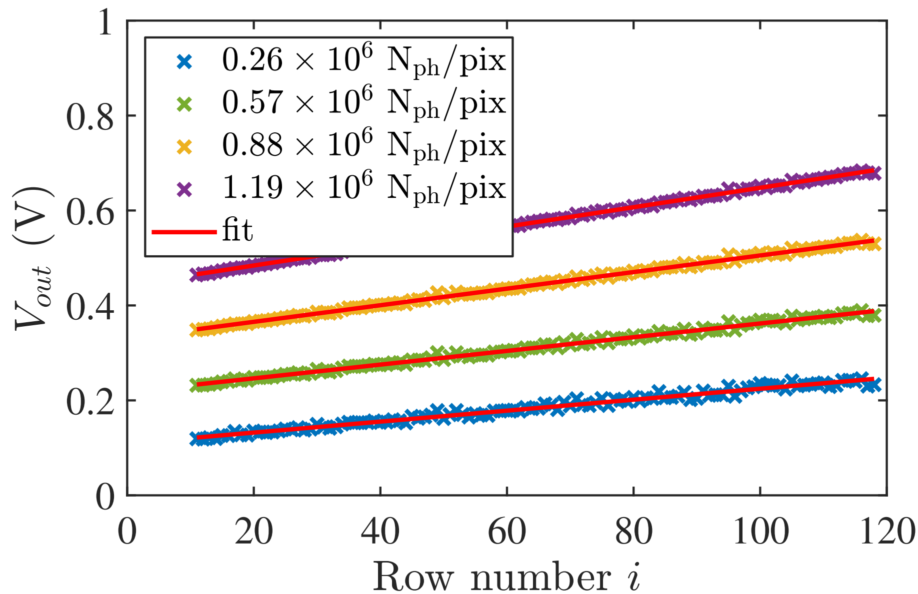


Figure 4.25: Output voltage as function of row number. Four curves are presented at different sphere irradiances, corresponding to different impinging photon rate levels. First order interpolation are presented with straight lines, noise is due to discrepancies in pixel-to-pixel Dark Current (DC), which has not been suppressed.

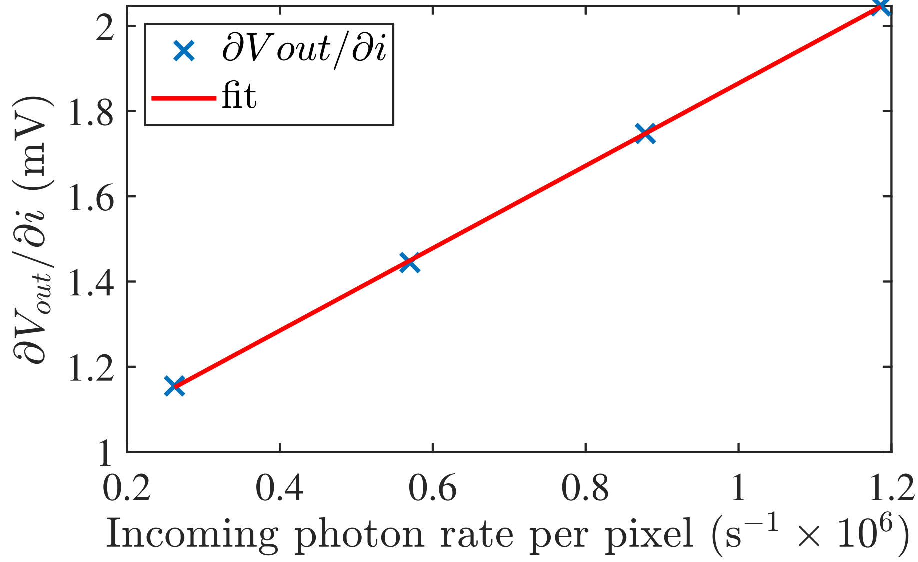


Figure 4.26: $\partial V_{out}/\partial i$ extracted from Fig. 4.25 as function of the incoming photon rate. Linear interpolation of $\partial V_{out}/\partial i$ is shown with a straight line.

the $(i-th, j-th)$ pixel will be given, exploiting Eq. (4.8), by the following:

$$\mathrm{V_{out}}(i,j) = V_{PD}(i,j) \cdot \left[1 + PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}}\right] \tag{4.11}$$

where

$$t_{strg}(i) = (i-1) \cdot t_{rro} \tag{4.12}$$

defines the row storage time. Please note that Dark Current contribution has voluntarily been forgotten since it can be considered as a storage time-dependent offset; this assumption allows simplification in the equations to be treated. From Eq. (4.11), it is possible to calculate V_{PD} (being the voltage not including Parasitic Light Sensitivity induced signal) through simple knowledge of the per-pixel measured PLS(i,j), the integration time t_{int} and the row readout time t_{rro} as given by the following:

$$V_{PD}(i,j) = \mathrm{V_{out}}(i,j) \cdot \left[1 + PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}}\right]^{-1} \tag{4.13}$$

The presented correction might not be valid when the scene to image is continuously changing, thus the illumination is time-variant. The readout period may undergo different light conditions with respect to the actual exposure, thus the parasitic signal integrated by the Storage Node would be function of time. Defining the beginning ($t = 0$) and the end

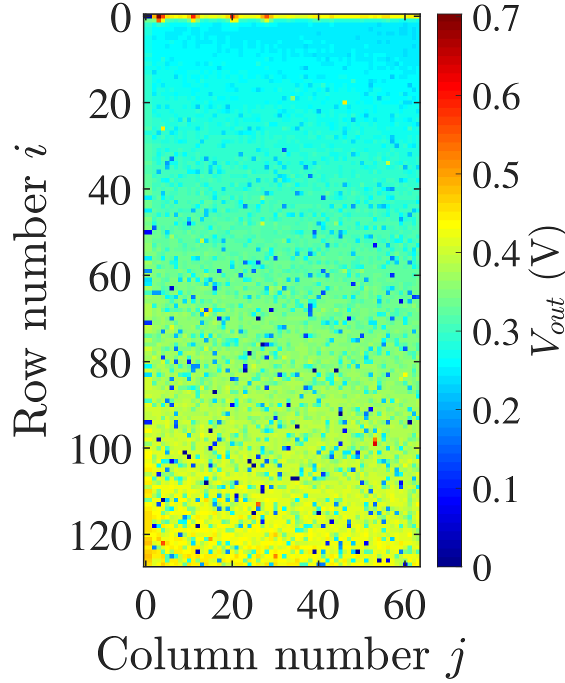


Figure 4.27: Output frame of the image sensor with row storage time equal to 50 ms. The output frame is the result of charge transfer from PhotoDiode to Storage Node after integration plus parasitic charges accumulated during readout, as function of the row number. DC_{SN} has been suppressed in post-treatment to allow appreciation of the Parasitic Light Sensitivity induced signal.

(t_{int}) of integration phase and the beginning of readout phase (t_r), the V_{out} would read

$$\begin{aligned} \mathrm{V_{out}}(i,j) = A(i,j) \cdot QE_{PD}(i,j) \cdot \int_0^{t_{int}} \Gamma(i,j,t)\, dt + \\ + A(i,j) \cdot QE_{SN}(i,j) \cdot \int_{t_r}^{t_r + t_{strg}(i)} \Gamma(i,j,t)\, dt. \end{aligned} \tag{4.14}$$

To further simplify the equations, we choose to approximate the integral of $\Gamma(i,j,t)$ over time as the following:

$$\int_{t_1}^{t_2} \Gamma(i,j,t)\, dt = \overline{\Gamma}_{t_1 t_2}(i,j) \cdot (t_2 - t_1), \tag{4.15}$$

where $\overline{\Gamma}_{t_1 t_2}(i,j)$ represents the mean photon rate in that interval of time. The image sensor output voltage will be finally modeled as given by Eq. (4.16).

$$\begin{aligned} \mathrm{V_{out}}(i,j) = A(i,j) \cdot QE_{PD}(i,j) \cdot \overline{\Gamma}_{t_{int}}(i,j) \cdot t_{int} + \\ + A(i,j) \cdot QE_{SN}(i,j) \cdot \overline{\Gamma}_{t_{strg}}(i,j) \cdot t_{strg}(i) \end{aligned} \tag{4.16}$$

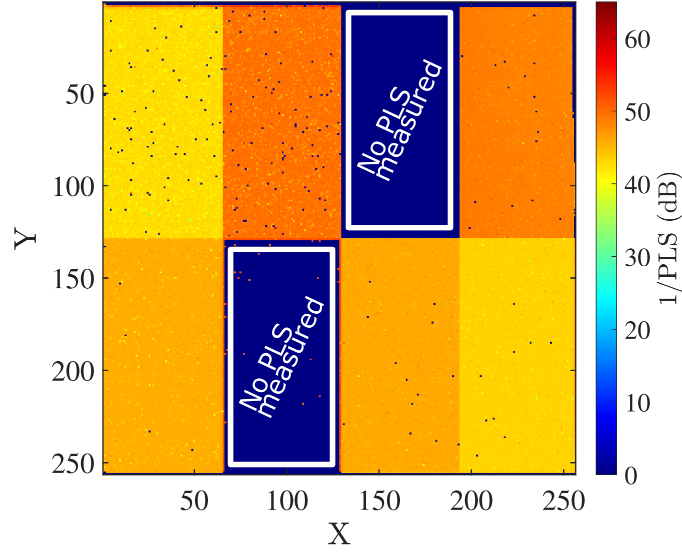


Figure 4.28: 2D cartography of Parasitic Light Hardness (1/PLS) of the tested sensor with 8 different zones. On the highlighted two zones, Parasitic Light Sensitivity measurement has not been possible.

Once the equation modeling V_{out} in Global Shutter CMOS Image Sensors has been fully developed, its exploitation may help to develop temporal domain post-process correction methods to mitigate Parasitic Light Sensitivity.

4.4.1.1 Testing correction in time-invariant approximation

In order to prove the efficiency of the equation in mitigating Parasitic Light Sensitivity, we have decided to test the equations for correcting a frame suffering from Parasitic Light Sensitivity in time-invariant conditions, meaning that incoming light intensity is constant through frame integration and readout. To this purpose, we will therefore exploit Eq. (4.11).

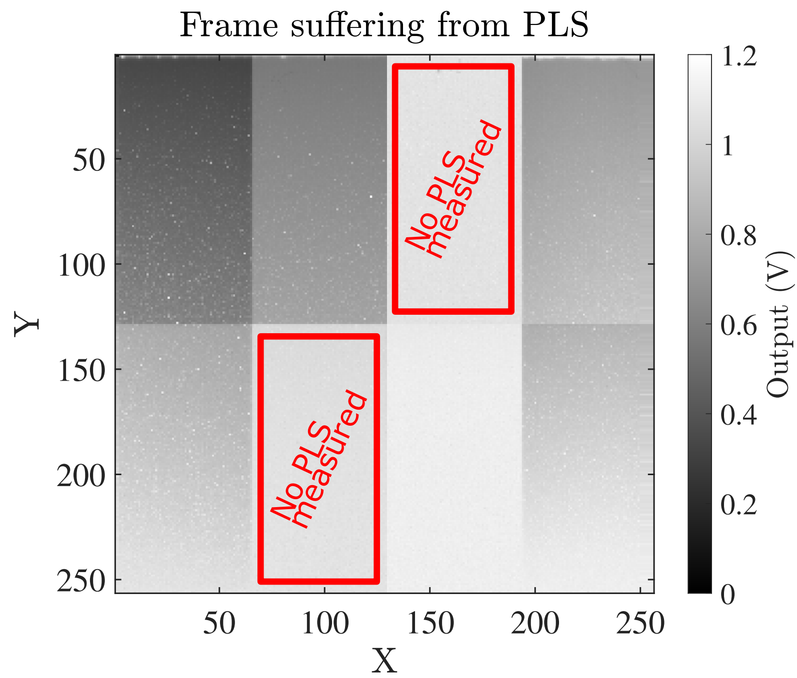
In order to increase the visibility of the Parasitic Light Sensitivity phenomena, row readout has been increased to 50 ms exploiting the same scheme presented in Fig. 4.23. The frame integration time is set to 50 ms, while the total readout time is 12.8 s considering an image sensor of 256 rows. The frame has been grabbed from a Global Shutter CMOS Image Sensor presenting 8 zones with different characteristics, thus showing different Parasitic Light Sensitivity. This latter has been measured pixel per pixel throughout the whole array (with the exception of two zones on which the measurement was not possible) and the result is shown in Fig. 4.28. The dark blue pixels (PLS = 0 dB) represent pixels on which the Parasitic Light Sensitivity measurement could not be performed (often "hot" pixels due to high Storage Node Dark Current). Parasitic Light Sensitivity measurement and frame grabbing are both performed at $\lambda = 650$ nm. Exploitation of a sensor with different zones aims to prove the correction methodology for various Parasitic Light Sensitivity on the same capture

frame.

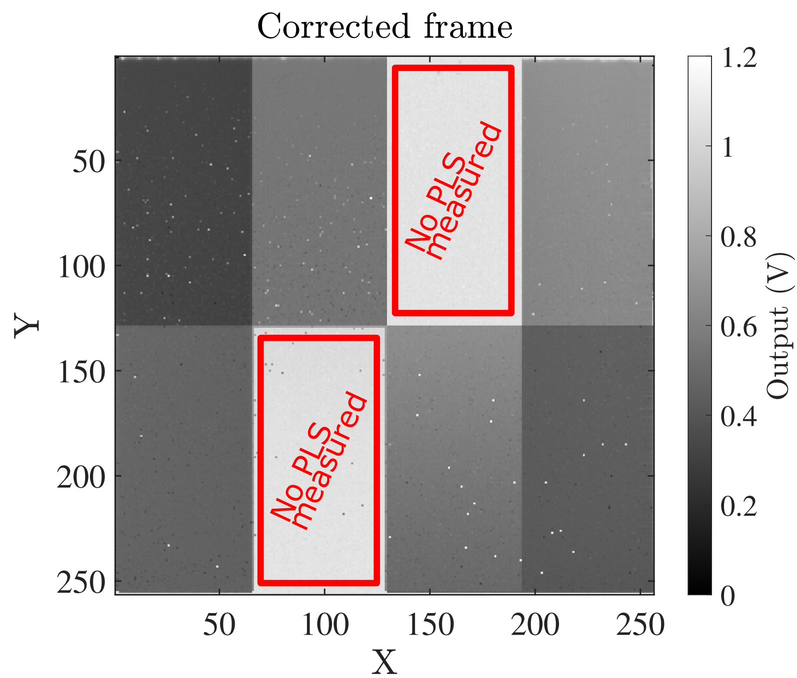
Fig. 4.29a shows the sensor output under constant strong light conditions at the given integration and readout times. Per-pixel correction as function of row number as given by Eq. (4.11) has been applied to this frame and the resulting correction is shown in Fig. 4.29b. It can be clearly seen how the correction has heavily reduced the parasitic light signal, thus making more 'flatted' per-zone response as it would be expected. Please note that Storage Node Dark Current signal has not been suppressed, and this can be appreciated on the corrected frame (a gradient of hot pixels is still present from the top to the bottom of the image).

To better appreciate the correction efficiency, Fig. 4.30 shows the pixel output as function of row number for both main frame (in black) and corrected frame (in red) for the marked zone. The bold lines represent the output mean of pixels on the same row. Aside from border effects (on the first rows), the efficiency of the correction can be appreciated in the "flattening" of the sensor response in comparison with the non-corrected frame having an important gradient as function of row number due to the Parasitic Light Sensitivity. A slight over-correction is nevertheless appreciable, as the red curve seem to decrease as function of the row number. Reason behind this "over-correction" is still under investigation.

These latter results show the importance of post-process correction methods in the temporal domain and the feasibility in exploiting the method shown for their development.



(a) Frame with Parasitic Light Sensitivity issue



(b) Corrected frame

Figure 4.29: (a) Main frame showing important deterioration due to Parasitic Light Sensitivity. (b) Frame resulting after Parasitic Light Sensitivity correction.

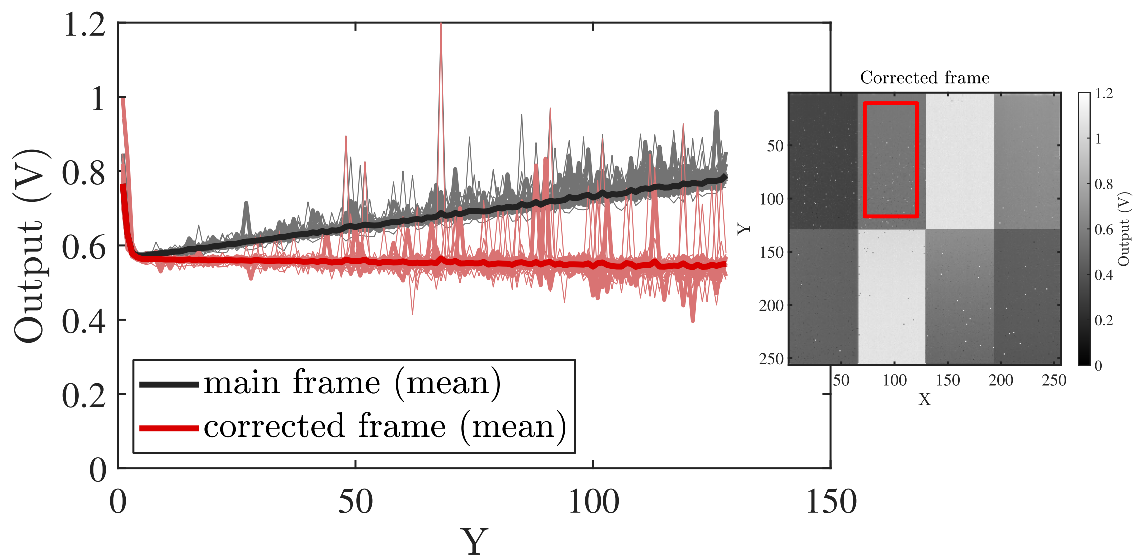


Figure 4.30: Per-pixel output as function of the row number for both main frame (in black) and corrected frame (in red). The solid lines represent the per-row outout mean. The inset shows the zone from which the pixels are considered. Storage Node Dark Current has not been suppressed.

4.4.2 Post-process correction methods in the temporal domain

This section aims to develop different methods for mitigating Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors using a temporal correction scheme. Nowadays, almost every Global Shutter CMOS Image Sensors is operated in the Integrate While Read mode; we will therefore only focus on this operating mode to develop schemes for Parasitic Light Sensitivity mitigation.

The Integrate While Read is intended for high speed imaging at strong illumination conditions. Differently from the Integrate Then Read mode, the PhotoDiode is in use during frame readout. It is therefore crucial to develop a correction method that allows integration on the PhotoDiode while the correction frame is being acquired.

4.4.2.1 Successive frames correction method

The most direct method that can be applied to mitigate Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors when operated in the Integrate While Read mode, without any need in modifying the frame structure adding a correction frame thus reducing the frame rate, is to use the successive frames to correct the previous one. This method is developed from the principle that frame N+1 is exposed during the readout of frame N, thus containing information on the scene that may cause the addition of parasitic light induced signal on frame N.

For the time being, we will consider that light intensity does not change during readout of frame N+1. It is therefore possible to compute $V_{PD,N+1}$, starting from Eq. (4.11), as follows:

$$V_{PD,N+1}(i,j) = \frac{V_{out,N+1}(i,j)}{1 + PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}}} \tag{4.17}$$

$$V_{PD,N+1}(i,j) = A(i,j) \cdot QE_{PD}(i,j) \cdot \overline{\Gamma}_{N+1}(i,j) \cdot t_{int} \tag{4.18}$$

From this, it is easy to find the equivalence between the frame N+1 output and the parasitic signal integrated on frame N since they share the same mean photon rate $\overline{\Gamma}_{N+!}$. We can redefine $V_{PLS}(i,j)$, following Eq. (4.6) and neglecting the Dark Current current, as:

$$V_{PLS,N}(i,j) = A(i,j) \cdot QE_{SN}(i,j) \cdot \overline{\Gamma}_{N+1} \cdot t_{strg}(i) \tag{4.19}$$

remembering that $t_{strg}(i)$ had been defined in Eq. (4.12). Mixing Eqs. (4.18) and (4.19) it

results that:

$$
\begin{aligned}
V_{PLS,N}(i,j) &= V_{PD,N+1}(i,j) \cdot \frac{QE_{SN}(i,j)}{QE_{PD}(i,j)} \cdot \frac{t_{strg}(i)}{t_{int}} \\
&= V_{PD,N+1}(i,j) \cdot PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}}
\end{aligned} \tag{4.20}
$$

$$
V_{PLS,N}(i,j) = \frac{V_{out,N+1}(i,j)}{1 + PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}}} \times PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}} \tag{4.21}
$$

It is therefore possible to correct frame N through combination of Eq. (4.16) and (4.18):

$$
V_{PD,N}(i,j) = V_{out,N}(i,j) - V_{PLS,N}(i,j) \tag{4.22}
$$

$$
V_{PD,N}(i,j) = V_{out,N}(i,j) - V_{out,N+1}(i,j) \cdot \frac{PLS \cdot \frac{t_{strg}(i)}{t_{int}}}{1 + PLS \cdot \frac{t_{strg}(i)}{t_{int}}}. \tag{4.23}
$$

In simple words, V_{PLS} of the N-th frame can be retrieved from V_{out} of the N+1-th frame, given the adaptation in time ($t_{strg}(i)/t_{int}$) and Quantum Efficiency ($PLS = QE_{SN}/QE_{PD}$).

When considering that light intensity may vary during readout of frame N+1, iterative frame correction may be required in order to be able to better correct the parasitic light induced signal on the N-th frame. $V_{PD,N+2}$ is adapted in time and Quantum Efficiency to retrieve $V_{PLS,N+1}$, that is then used to retrieve $V_{PD,N+1}$ through subtraction. $V_{PD,N+1}$ is adapted in time and Quantum Efficiency to retrieve $V_{PLS,N}$, that is then used to retrieve $V_{PD,N}$. This is better explained as follows:

$$
\begin{aligned}
V_{PLS,N+2}(i,j) &= \frac{V_{out,N+3}(i,j)}{1 + PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}}} \cdot PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}} \\
&= V_{PD,N+3} \cdot PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}}
\end{aligned} \tag{4.24}
$$

$$
V_{PD,N+2}(i,j) = V_{out,N+2}(i,j) - V_{PLS,N+2}(i,j) \tag{4.25}
$$

$$
V_{PLS,N+1}(i,j) = V_{PD,N+2}(i,j) \cdot PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}} \tag{4.26}
$$

$$
V_{PD,N+1}(i,j) = V_{out,N+1}(i,j) - V_{PLS,N+1}(i,j) \tag{4.27}
$$

$$
V_{PLS,N}(i,j) = V_{PD,N+1}(i,j) \cdot PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}} \tag{4.28}
$$

$$
V_{PD,N}(i,j) = V_{out,N}(i,j) - V_{PLS,N}(i,j) \tag{4.29}
$$

Reconstructing $V_{PD}(i,j)$ we have:

$$
\begin{aligned}
V_{PD,N}(i,j) &= V_{out,N}(i,j) - V_{PLS,N}(i,j) \cdot PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}} \\
&= V_{out,N}(i,j) - \Big(V_{out,N+1}(i,j) - V_{PLS,N+1}(i,j)\Big) \cdot PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}} \\
&= V_{out,N}(i,j) - \left(V_{out,N+1}(i,j) - V_{PD,N+2}(i,j) \cdot PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}}\right) \times \\
&\quad \times PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}} \\
&= V_{out,N}(i,j) - \Big(V_{out,N+1}(i,j) - [V_{out,N+2}(i,j) - V_{PLS,N+2}(i,j)] \times \\
&\quad \times PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}}\Big) \cdot PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}} \\
&= V_{out,N}(i,j) - V_{out,N+1}(i,j) \cdot PLS(i,j) \frac{t_{strg}(i)}{t_{int}} + \\
&\quad + V_{out,N+2}(i,j) \cdot \left(PLS(i,j) \frac{t_{strg}(i)}{t_{int}}\right)^2 + \\
&\quad - V_{out,N+3}(i,j) \cdot \frac{\left(PLS(i,j) \frac{t_{strg}(i)}{t_{int}}\right)^3}{1 + PLS(i,j) \frac{t_{strg}(i)}{t_{int}}}
\end{aligned}
\tag{4.30}
$$

The correction process results to be iterative and follows Eq. (4.31), considering using (M-N) frames to correct frame N. The integration time of each frame is considered constant and equal to t_{int}.

$$
\begin{aligned}
V_{PD,N}(i,j) = &\sum_{k=N}^{M-1} (-1)^{k-N} \cdot V_{out,k}(i,j) \cdot \left(PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}}\right)^{k-N} + \\
&+ (-1)^{M-N} \cdot V_{out,M}(i,j) \cdot \frac{\left(PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}}\right)^{M-N}}{1 + PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}}}
\end{aligned}
\tag{4.31}
$$

The equation is obtained iterating the process described by Eqs. (4.18) and (4.23). It can be seen that if $M = N + 1$ the Eqs. (4.31) and (4.23) are equivalent. For $M = N + 3$, Eq. (4.31) is equivalent to Eq. (4.30).

The presented method has though various drawbacks. It is worth of notice that higher the number of frames used for correction, higher the impact on final frame noise (given that linear operation with frames leads to the square root of the sum of the squares of the noises),

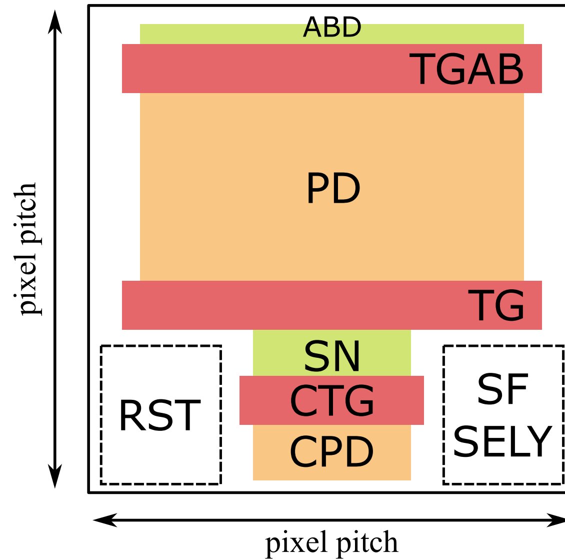


Figure 4.31: Schematic layout of a pixel that can be exploited for successive frame correction in the Integrate While Read mode. PhotoDiode (PD), TG, Storage Node (SN), TGAB and ABD are present as in a standard 5T Global Shutter pixel. A second PhotoDiode is added (CPD) and connected to the Storage Node through an additional transfer gate (CTG). Readout electronics is then placed (RST, SF and SELY).

thus leading to a decrease in SNR. Moreover, it is believed that the parasitic light induced signal on the last frame used for correction (frame M) remains uncorrected, thus disturbing a proper correction of the frame. Nevertheless, experimental tests should be performed to prove this last assumption.

4.4.2.2 Sequential frame correction method

Successive frames correction is limited by the fact that the last frame exploited for correction contains itself parasitic light induced signal that has not been suppressed. The method will therefore add parasitic light induced signal of the last frame onto the frame that is required to be corrected. To improve Parasitic Light Sensitivity mitigation when a Global Shutter CMOS Image Sensors is operated in the Integrate While Read, a sequential correction frame is required. The addition of a correction frame would though have an impact on the minimum frame rate, halving the latter due to the presence of a second frame.

As previously said, it is crucial to be able to measure the intensity of the impinging light during the readout phase. This could be performed on a node in parallel with the Storage Node. Usage of the PhotoDiode for the integration of a correction frame is impossible, as the PhotoDiode needs to be exploited for the following frame integration. Taking the example of a 5T Global Shutter pixel where the Floating Diffusion acts as the Storage Node, there exist no alternative nodes on which to integrate the sequential correction frame. An adjustment to the pixel structure can be thought for this purpose adding a supplementary pinned diffusion,

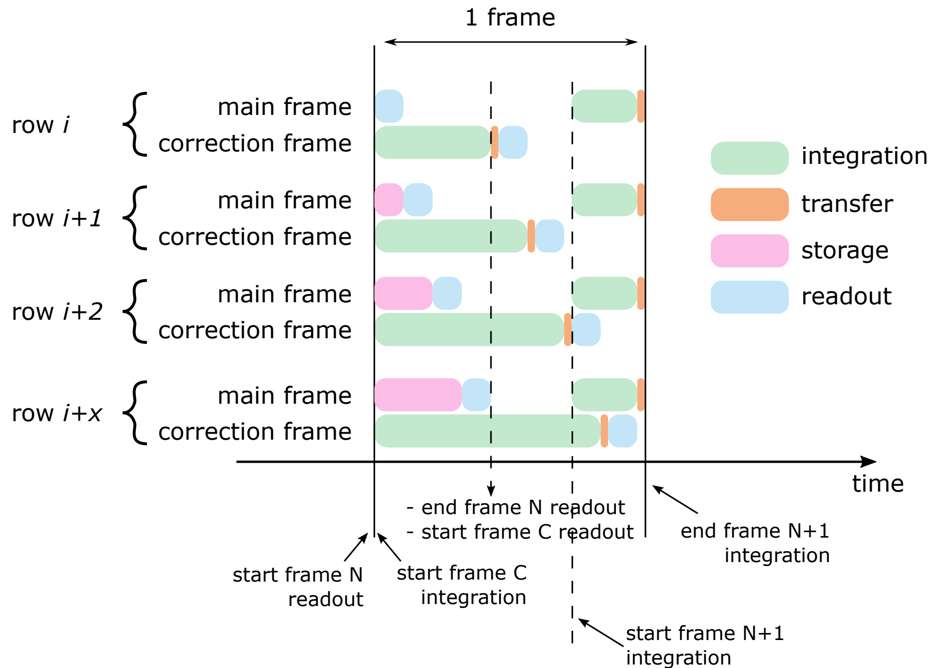


Figure 4.32: Timing diagram showing the sequence of frame N (Global Shutter frame) and frame C (correction frame) as exploited in the sequential frame correction method. Frame C integration starts at the end of frame N global transfer on the newly added Correction PhotoDiode (CPD). Frame N readout is performed; soon after, frame C readout is performed. During frame C readout, the PhotoDiode is made available to start its integration when required.

called Correction PhotoDiode (CPD) on which to integrate the correction frame, as shown in Fig. 4.31. The Correction PhotoDiode will be connected to the Floating Diffusion through a supplementary transfer gate (CTG), through which it can be reset. Its aim is to integrate parasitic photons to estimate the intensity of the impinging light during readout. Due to the strong illumination conditions to which Global Shutter CMOS Image Sensors are often subject, the Correction PhotoDiode needs to have a limited Quantum Efficiency in order to not be driven to saturation, thus altering the measurement. Limited Quantum Efficiency is achieved through shielding, though it is not required to be perfect as it is important to be able to collect few charges. A reduced Quantum Efficiency allows to design a smaller Correction PhotoDiode with respect to the main PhotoDiode, thus reducing the fill factor loss. Correction PhotoDiode readout noise should be as lower as possible, to reduce the impact of noise on the main frame. With the addition of a supplementary node Correlated Double Sampling operation is again available, thus allowing for suppression of the kTC noise on the Floating Diffusion.

Fig. 4.32 shows the time diagram of the sequential correction method applied to the Integrate While Read mode. Once frame N integration is terminated, frame N readout begins as well as frame C integration. Once frame N readout is terminated, frame C readout begins; frame N+1 integration can easily start during frame C readout, thus the frame rate is only

reduced by a half.

Because of the presence of Correction PhotoDiode, we define a new ratio PLS_C as:

$$PLS_C = \frac{QE_{SN}}{QE_{CPD}}. \tag{4.32}$$

The addition of a new ratio nevertheless implies supplementary measurements for the correct application of the model. Exploiting the pixel output model previously developed, we can derive the equations to model the correction frame, to which we will refer as frame C from now on:

$$V_{out,C}(i,j) = A(i,j) \cdot QE_{CPD}(i,j) \cdot \overline{\Gamma}_C(i,j) \cdot t_{int,C}(i) \tag{4.33}$$

$$t_{int,C}(i) = N_{row} \cdot t_{rro} + (i-1) \cdot (t_{rro} + t_{trans}) \tag{4.34}$$

where $\overline{\Gamma}_C(i,j)$ represents the mean per-pixel photon rate during the integration of frame C, t_{trans} is the time required to transfer charges from the PhotoDiode to the Storage Node or from the Correction PhotoDiode to Storage Node and N_{row} is the total number of rows of the image sensor. The integration window of the correction frame starts right at the beginning of the main frame readout. Frame C readout starts right after frame N readout. This means that frame C integration time, $t_{int,C}$ has a minimum time equal to the time required to readout the first frame ($N_{row} \cdot T_{rro}$). It is moreover row dependent, as each row readout ends the frame C integration on that row. The difference in time between row readouts is represented by the time required to transfer the charges from Correction PhotoDiode to Storage Node, t_{trans}, and the time required to actually readout one row, t_{rro}.

Frame C can therefore be applied to correct output in the main frame, also called frame N; the final corrected frame output V_{PD} can be retrieved in Eq. (4.35) with the help of Eq. (4.14).

$$V_{PD}(i,j) \approx V_{out,N}(i,j) - V_{out,C}(i,j) \cdot PLS_C(i,j) \cdot \frac{t_{strg}(i)}{t_{int,C}(i)} \tag{4.35}$$

Note that the equality symbol may stand only if the integral is correctly approximated by the formula given in (4.15), thus implying that the incoming photon rate is time-invariant during the whole frame C exposition. If the latter is not true, frame correction would provide an approximation of the Parasitic Light Sensitivity induced signal and thus of the desired value.

4.4.2.3 Correction frame on 6T Global Shutter pixels

Modern Global Shutter CMOS Image Sensors are built with 6T pixels, where charge storage is performed on a pinned diode and Correlated Double Sampling is made available. A schematic of a 6T pixel is shown in Fig. 4.33. As it can be seen, Storage Node and Floating Diffusion are now two different entities. In normal Global Shutter operations, the Floating Diffusion has no storage obligations; it can therefore be exploited as the node on which to integrate the correction frame.

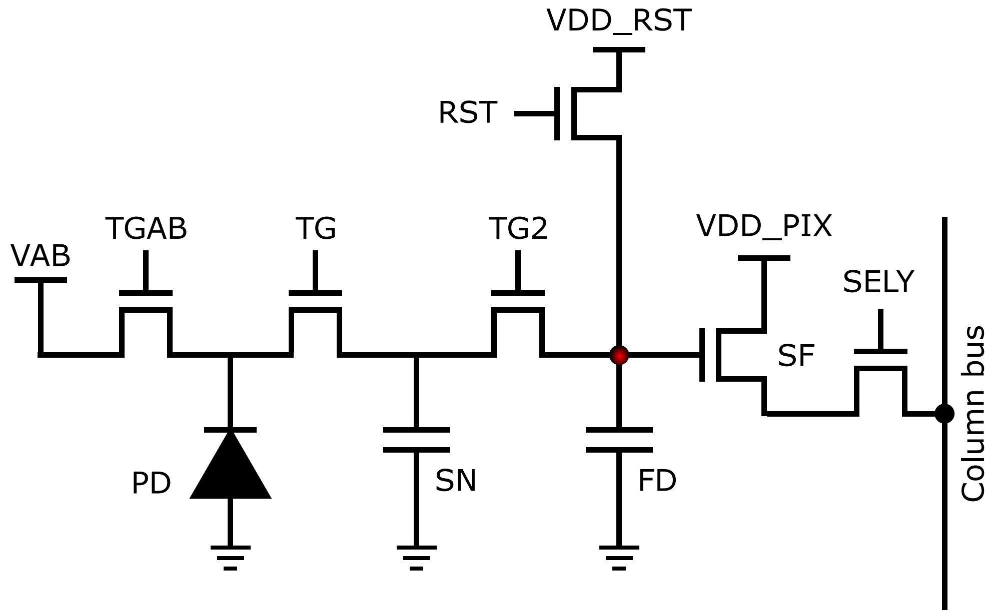


Figure 4.33: Schematic of a charge storage 6T Global Shutter pixel. Differently from the 5T pixel, the Storage Node is built separately from the Floating Diffusion and connected via another transfer gate, TG2.

A possible time diagram of the readout of both main and correction frame is shown in Fig. 4.34. Differently from what commonly seen, there is an additional command signal called SHC. This signal is exploited to sample the correction voltage level that has been integrated on the Floating Diffusion. In order to do so, a supplementary Sample&Hold circuit has to be added at the column level.

The main concept of this correction relies on the fact that the Floating Diffusion is used as both the node on which to integrate the correction frame as well as the node on which the voltage levels are sampled. Three samplings are sequentially performed per each row:

1. Sampling of the voltage level on the Floating Diffusion; it represents the voltage level due to the integration of correction frame $V_{CORR}(i, j)$.
2. Sampling of the voltage level on the Floating Diffusion after the reset operation; it represent the reference voltage $\mathrm{V_{REF}}$.
3. Sampling of the voltage level on the Floating Diffusion after the transfer operation via TG2; it represent the signal voltage $\mathrm{V_{SIG}}$.

The output voltage of the main frame is retrieved $V_{out,N}(i, j) = \mathrm{V_{REF}}(i, j) - \mathrm{V_{SIG}}(i, j)$, while the output voltage of the correction frame is retrieved as $V_{out,C}(i, j) = \mathrm{V_{REF}}(i, j) - V_{CORR}(i, j)$. It can be appreciated as only one $\mathrm{V_{REF}}$ sampling is exploited for both main and correction frame. Though it may seem interestingly quick, analog to digital conversion is

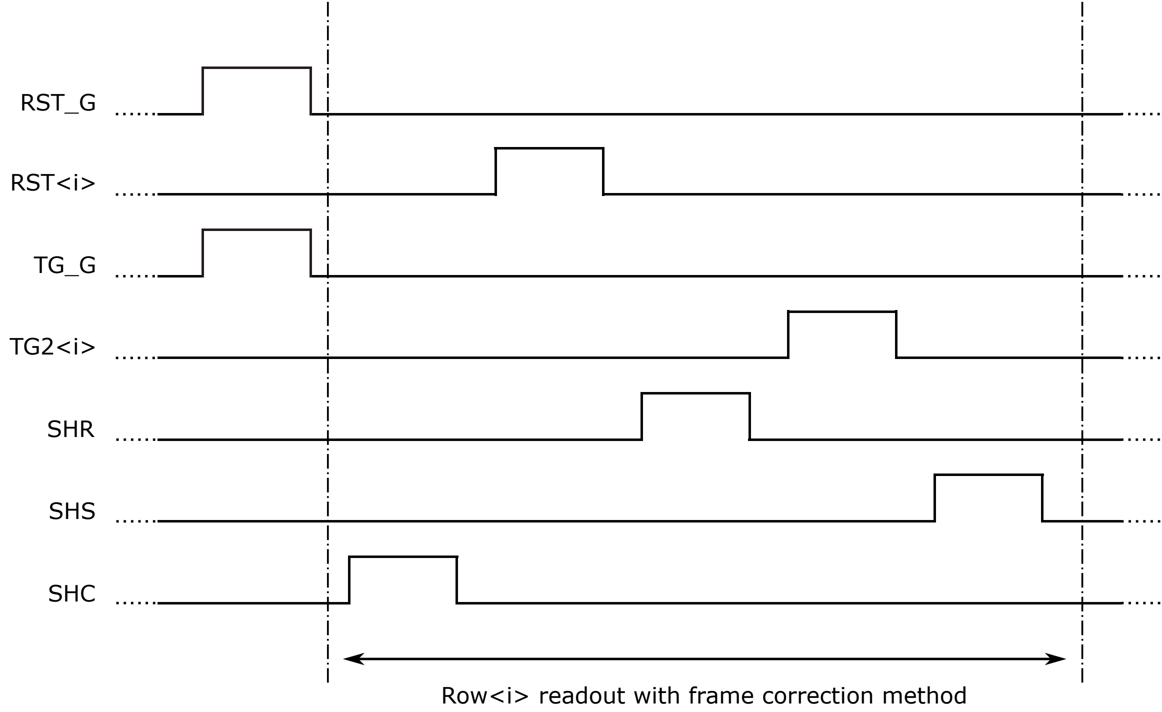


Figure 4.34: Time diagram of the readout sequence of the main and correction frame on a 6T pixel. Global transfer is performed and at the same time a global reset operation is performed on all Floating Diffusions. After the global transfer, each row is sequentially readout. First, the signal integrated on the Floating Diffusion is acquired with the command SHC. A reset operation is performed through RST and the reference level is sampled through the SHR command. Transfer from the Storage Node to the Floating Diffusion is performed exploiting TG2 and the integrated signal sampled through the SHS command.

required for both correction and main frame, thus there are no advantages in terms of timing with respect to the other techniques. Drawback of this technique is that the correction frame will carry kTC noise due to the intrinsic Non-Correlated Double Sampling operation to readout the Floating Diffusion node.

Again exploiting the pixel output model previously developed, we can give a modeling of frame C output as function of the pixel position:

$$V_{out,C}(i,j) = A(i,j) \cdot \overline{\Gamma}_C(i,j) \cdot QE_{FD} \cdot (i-1) \cdot t_{rro}. \tag{4.36}$$

In a similar manner, we can give a modeling of the frame N output as function of the pixel position:

$$V_{out,N}(i,j) = V_{PD}(i,j) + A(i,j) \cdot \overline{\Gamma}_C(i,j) \cdot QE_{SN} \cdot \left[(i-1) \cdot t_{rro} + t_x\right], \tag{4.37}$$

where t_x represents the time to perform the SHS, RST and SHR operations. Given Eqs. (4.36)

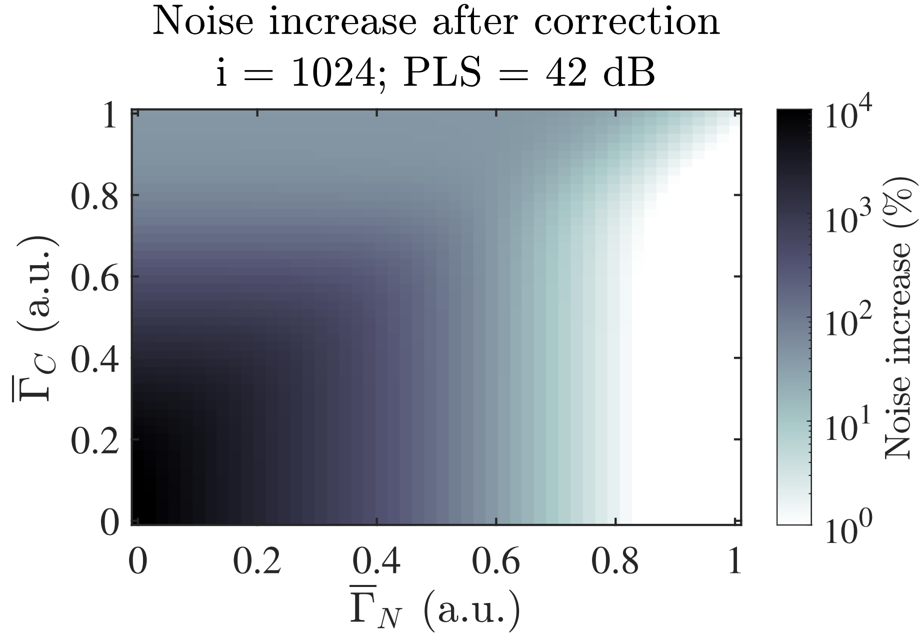


Figure 4.35: Simulation of noise increase after correction, as function of the scene illumination. $\overline{\Gamma}_N$ and $\overline{\Gamma}_C$ represents respectively the mean per-pixel incoming photon rate during frame N and frame C integration. The simulation has been performed with a constant image sensor Parasitic Light Sensitivity value of 42 dB and at row $i = 1024$.

and (4.37) it is easy to retrieve V_{PD}:

$$V_{PD}(i,j) = V_{out,N}(i,j) - \frac{QE_{FD}(i,j)}{QE_{SN}(i,j)} \cdot \left[1 + \frac{t_x}{(i-1) \cdot t_{rro}}\right] \cdot V_{out,C}(i,j), \tag{4.38}$$

where we have decided to keep the ratio $\frac{QE_{FD}}{QE_{SN}}$ as it is to avoid confusion. Similarly, no storage time t_{strg} has been exploited in the modeling to avoid confusion, since it is slightly different to the one presented before due to the time diagram exploited and presented in Fig. 4.33.

Differently from what presented before, the time window on which the correction frame is integrated on the Floating Diffusion is almost equivalent to the time window on which the main frame is stored on the Storage Node. This results in an improved estimation of the parasitic light induced signal and a better performance of the correction technique.

In order to appreciate the impact of the use of a correction frame, noise analysis have been performed through the development of a noise model. Four main sources of noise are considered: photon shot noise ($\sigma_{ph}(i,j)$), Dark Current shot noise of Floating Diffusion ($\sigma_{DC_{FD}}(i,j)$) and kTC noise ($\sigma_{kTC}(i,j)$) and quantization noise ($\sigma_q(i,j)$). Readout chain noise will not be taken into account in our modeling; similarly, Dark Current shot noise on PhotoDiode and Storage Node will not be considered being at least two orders of magnitudes lower than the one on Floating Diffusion as this latter is not pinned. Let us focus on shot noise in the two frames acquisition previously presented. Supposing that $\overline{\Gamma}_N$ and $\overline{\Gamma}_C$ are respectively the

mean per-pixel incoming photon rate during frame N and frame C integration, three main photon shot noise sources appear: $\sigma_{ph_{PD}}$ related to the number of electrons collected by the PhotoDiode during frame N exposition and described by Eq. (4.39); $\sigma_{ph_{SN}}$ related to the number of electrons collected by the Storage Node during the frame N storage phase and described by Eq. (4.40); $\sigma_{ph_{FD}}$ related to the number of electrons collected by the Floating Diffusion during frame C exposition and described by Eq. (4.41).

$$\sigma_{ph_{PD}}(i,j) = A(i,j) \cdot \sqrt{QE_{PD}(i,j) \cdot \overline{\Gamma}_N(i,j) \cdot t_{int}} \tag{4.39}$$

$$\sigma_{ph_{SN}}(i,j) = A(i,j) \cdot \sqrt{QE_{SN}(i,j) \cdot \overline{\Gamma}_C(i,j) \cdot [(i-1) \cdot t_{rro} + t_x]} \tag{4.40}$$

$$\sigma_{ph_{FD}}(i,j) = A(i,j)\sqrt{\cdot QE_{FD}(i,j) \cdot \overline{\Gamma}_C(i,j) \cdot (i-1) \cdot t_{rro}} \tag{4.41}$$

Dark Current shot noise on Floating Diffusion is described as

$$\sigma_{DC_{FD}}(i,j) = A(i,j) \cdot \sqrt{DC_{FD}(i,j) \cdot (i-1) \cdot t_{rro}} \tag{4.42}$$

For a rightful calculation of final noise after subtraction $\sigma_{PD}(i,j)$, frame N output noise $\sigma_{out,N}(i,j)$ and frame C output noise $\sigma_{out,C}(i,j)$ are modeled and shown respectively in Eqs (4.43) and (4.44). No kTC noise is associated to the frame N readout since Correlated Double Sampling operation is performed. On the other hand, kTC noise in frame C has been taken into account twice due to Non-Correlated Double Sampling operation. Following Eq. (4.38), the total output noise voltage after the two frames subtraction is given by Eq. (4.45).

$$\sigma^2_{out,N}(i,j) = \sigma^2_{ph_{PD}}(i,j) + \sigma^2_{ph_{SN}}(i,j) + \sigma^2_q(i,j) \tag{4.43}$$

$$\sigma^2_{out,C}(i,j) = \sigma^2_{ph_{FD}}(i,j) + \sigma^2_{DC_{FD}}(i,j) + 2\,\sigma^2_{kTC}(i,j) + \sigma^2_q(i,j) \tag{4.44}$$

$$\sigma^2_{PD}(i,j) = \sigma^2_{out,N}(i,j) + \frac{QE_{FD}(i,j)}{QE_{SN}(i,j)} \cdot \left[1 + \frac{t_x}{(i-1) \cdot t_{rro}}\right] \cdot \sigma^2_{out,C}(i,j) \tag{4.45}$$

Fig. 4.35 shows the increase in output noise at row number $i = 1024$ as function of mean per-pixel incoming photon rate during frame N and frame C. The following data has been taken into account in our calculations: $QE_{PD} = 45\%$, $QE_{SN} = 0.3\%$ and so $1/PLS = 42\,dB$, $QE_{FD} = 0.1\%$, $t_{rro} = 10\,\mu s$, $t_{int} = 2\,ms$. Calculations show an increase in readout noise due to the correction operation. As expected, frame subtraction has an important impact at low light conditions (bottom left corner of the figure), where frame noises are dominated by kTC and quantization noise. Moreover, the correction suffers sudden dark-to-bright changes in the illumination (upper left corner of the figure), where noise increase is also high, though not as much as in both low lights conditions. Calculations have demonstrated that a reduction (or suppression) of the kTC noise may drastically improve the noise performances of the method. As a summary, the presented method can help in mitigating Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors at the cost of an increase in noise and thus a reduction

in the SNR. This latter reduction is more important in case of dark-to-bright changes in the illumination condition, while its importance rapidly drops in brighter illumination conditions.

Let us now closer analyze the key points of this correction technique. It has been previously said that the problem of temporal correction technique presented in [SJI19] relies on the fact that the integration of the parasitic light induced signal is performed after the readout phase; this may lead to an incorrect evaluation of the parasitic light induced signal during the actual readout phase. Moreover, the integration and readout of a supplementary correction frame on the same Storage Node reduces the frame rate of more than a half. On the other hand, there is no need for a complete mapping of the Parasitic Light Sensitivity over the array. The correction technique developed for 6T pixels aims to solve the critical issues of frame rate, that is only halved, and estimation of the parasitic light induced signal, which is being measured during the actual readout phase. On the other hand, the presented correction method may add additional noise due to the correction frame carrying kTC noise, as well as requiring mapping of both Storage Node and Floating Diffusion Quantum Efficiencies.

In conclusion, various methods for mitigating Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors operated in the Integrate While Read mode have been presented, exploiting the equations developed to model the output voltage as function of the parasitic light induced signal, that have been validated through experimental data. A supplementary correction frame has often been introduced to allow detection of the parasitic light induced signal during the readout phase. The addition of a correction frame reduces the minimum frame rate of the image sensor, often being a limiting factor in the Integrate While Read mode. Following two types of Global Shutter pixels, two methods have been presented. Exploiting 5T pixels, a supplementary pinned diffusion has to be integrated in the pixel to allow integration of the correction frame, thus further limiting the pixel fill factor. Reason behind the choice of a pinned diffusion as a supplementary node lies on the fact that pinned diffusions can be completely emptied, thus avoiding additional kTC noise [FH14]. On the other hand, exploitation of 6T pixels do not require the addition of any supplementary diffusion; the advantage is though compensated by the introduction of kTC noise on the correction frame. All developed methods requires mapping of Parasitic Light Sensitivity (to be more specific, of different Quantum Efficiencies) to correctly operate.

4.5 Conclusion

Experimental results are crucial to verify the validity of developed models and to test that the designed devices behave in the desired way. The first part of this chapter has therefore been devoted to the characterization of Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors, from the development of a metric to the actual testing of structures.

A standard metric for measuring Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors has been developed, giving that no guidelines exist in the EMVA 1288 standard. The metric is based on a classical Quantum Efficiency measurement on the PhotoDiode plus the development of a Quantum Efficiency measurement on the Storage Node. In order to

avoid any interference of the Dark Current, it has been chosen to perform the Quantum Efficiency measurements for both PhotoDiode and Storage Node as function of the illumination conditions, thus acting on the light intensity instead of the integration time. The time diagrams associated with the two measurements have been presented, related to the measurement of an array of 5T pixels. Nevertheless, it has been shown the possibility of applying the metric for any type of Global Shutter (voltage or charge domain, different charge storage nodes, etc.) slightly modifying the timing diagrams to the requirements. Finally, a 5T pixels Global Shutter array has been characterized exploiting the developed metrics; experimental results show the possibility to accurately measure Parasitic Light Sensitivity as function of wavelength.

The developed metric has been successively exploited to test different structures that have been designed following previously presented simulation guidelines. Test structures provided with different Storage Node width have been characterized, showing a linear behavior of the Storage Node Quantum Efficiency as function of the Storage Node width. As expected, a smaller Storage Node width leads to a smaller Quantum Efficiency, allowing for improved Parasitic Light Hardness (1/PLS) performances. Nevertheless, it has been appreciated that the Quantum Efficiency and the Storage Node width do not grow at the same rate, indicating a more complex dependence of the Quantum Efficiency with the node's dimensions that needs to be further investigated.

Different structures have been developed to analyze the impact of diffraction on the Parasitic Light Sensitivity performances of Global Shutter CMOS Image Sensors, as previously reported by simulations; exploitation of different shielding metal levels has allowed to design and fabricate structures for this purpose. Experimental results withdrawn from measurements of these test structures have led to similar conclusions to what has been given with simulation results: diffraction plays an important role in modeling Parasitic Light Sensitivity performances of CMOS Image Sensor and lower metal levels are best suited to properly shield the Storage Node from parasitic light.

Similarly, some other structures have been developed to analyze the impact of the positioning of metal layers shielding the Storage Node. It has been experimentally demonstrated that increasing the distance between the Storage Node edges and the shielding metal edges helps reducing the Storage Node Quantum Efficiency; nevertheless, careful attention has to be payed to the PhotoDiode Quantum Efficiency, that can be increasingly reduced if partially shielded by the metal layer. As a general rule, it can be stated that light shielding has to be carefully taken into account when the Global Shutter CMOS Image Sensors is being designed to operate in the visible wavelength range. Exploiting the lowest metal level for shielding is preferred, coupled with its extension "beyond" the Storage Node area, slightly covering the PhotoDiode as well; reduction in the PhotoDiode Quantum Efficiency is limited for small extensions but largely effective for reduction of Storage Node Quantum Efficiency and thus improving Parasitic Light Hardness (1/PLS). The optimal metal extension has to be tailored on the technology (distance of metal levels to the SiO_2 surface) and the pixel design. The NIR wavelength range is impacted as well by the metal level exploited, the lowest possible one being always preferred. On the other hand, shielding metal extension has a weaker impact

with respect to the visible range and is not suggested in the NIR wavelength range.

The impact of micro-lens on Parasitic Light Sensitivity has been finally stated. A better focus of impinging light onto the PhotoDiode helps increasing the generation of charges in the PhotoDiode region and reduce the generation of charges in the Storage Node region, thus improving the Parasitic Light Hardness (1/PLS) performances. It has been realized that micro-lenses have a more important impact at shorter than at longer wavelengths and, differently from what expected, a pixel integrating no micro-lens and having a small dimensions Storage Node performs better at longer wavelength compared to a pixel integrating micro-lens but having a Storage Node with important dimensions. When operating at longer wavelengths, this result has to be taken into account when designing a Global Shutter CMOS Image Sensors.

Finally, experimental results of two pixel structures have been compared to simulation results previously presented. Some parameter corrections have been applied to the model in order to correctly fit the experimental results. Parasitic Light Hardness (1/PLS) behavior as function of wavelength is fairly well reproduced for both pixel structures, though some inaccuracies are present. Moreover, both PhotoDiode and Storage Node Quantum Efficiency have been compared. The comparison highlights the need in better knowledge of the BEOL process to model the pixel in the FDTD simulations, given the important discrepancies of the Quantum Efficiency results.

The second part of this chapters deals with measurements exploited to develop an analytical model of the CMOS Image Sensor output when operated in the Global Shutter mode, thus taking into account the added signal induced by the non-negligible Parasitic Light Sensitivity. Once developed and validated through ad hoc experimental measurements, the analytical model has been exploited to analyze and develop some post-process methods to mitigate the effect of Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors. Post-process methods have been developed for the commonly used Integrate While Read mode.

In the Integrate While Read mode, frame rate is crucial. Maintaining a high frame rate requires no addition of supplementary frames. Thanks to the use of the analytical model, it has been tried to develop a correction method using successive frames; the efficiency of this method for mitigating Parasitic Light Sensitivity should be tested and verified on a real Global Shutter CMOS Image Sensors, given that the parasitic light induced signal on the last correcting frame may impact the whole correction. A second method has been presented, exploiting 5T Global Shutter pixels. This method requires a modification in the pixel structure through the addition of a supplementary PhotoDiode (Correction PhotoDiode). Correction frame is then integrated on the Correction PhotoDiode while the successive main frame can be integrated on the main PhotoDiode. The addition of a supplementary frame though reduces the frame rate by a half. A third method has also been presented, exploiting commonly used 6T charge storage Global Shutter pixels. Correction frame integration is performed on the Floating Diffusion and simultaneously with the main frame readout phase, allowing for a simpler readout scheme, though carrying additional kTC noise.

Post-process correction methods seem to be an interesting alternative to pixel improve-

ment by process. It is now crucial to validate these theoretical methods through experimental results.

Conclusion and outlook

This thesis presents a study on Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors for high speed applications. Notably, the work was focused on the understanding of the phenomena leading to non-negligible Parasitic Light Sensitivity through the use of both simulations and measurements.

The Image Sensors market has been pushing towards the development of Global Shutter CMOS Image Sensors, with the aim in reducing spatial distortions that are caused by a non-synchronous integration of the sensor pixel array. Global Shutter CMOS Image Sensors are therefore better suited for imaging fast-moving object with respect to their counterpart, the Rolling Shutter CMOS Image Sensors; in this light, Global Shutter CMOS Image Sensors are demanded for a wide variety of applications, as for example industrial machine vision, automotive, facial and motion recognition and Earth imaging from space [LMR13]; [Mey14]; [Vel+16]. Applications like facial and motion recognition often require near infrared detection, thus both visible and near infrared range performances are highly desired [Miz+20].

Nevertheless, non-negligible Parasitic Light Sensitivity remains one big issue limiting the exploitation of Global Shutter CMOS Image Sensors, especially in applications under strong illumination. Parasitic Light Sensitivity is caused by the collection of parasitic charges on the in-pixel Storage Node, during the frame storage and readout phase. Inserted in this framework, the research work has been focused on the development of a method to model Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors, aiming in understanding the main phenomena related to the non-negligible light sensitivity of charge storage nodes and enhancing the pixel design through improvements of the storage node shielding at both visible and near infrared spectrum.

A method for modeling Parasitic Light Sensitivity has been presented in the second chapter of this work. The method is based on the resolution of the optical propagation of light into the pixel structure and the propagation of the photo-generated charges towards the PhotoDiode and the Storage Node trough the use of simulations. Both optical and charge transport problems are solved at steady-state, allowing for a parallel run of the simulations and thus an independent generation of their solution. The choice of the optical simulation has been driven by the need to take into account the light diffraction phenomenon; FDTD simulations on the Lumerical suite have therefore been chosen, allowing for an accurate and computationally efficient resolution of the Maxwell's equations. The simulation result is represented by the steady-state charge generation rate in the silicon epitaxial layer at a given impinging wavelength and at a given pixel structure.

Resolution of the charge transport problem has been developed with the aim in building a Collection Probability weighting function that determines the probability of either the PhotoDiode or the Storage Node to collect charges generated at a given point in space. Two descriptions of the charges motion in Silicon have been exploited for this purpose: a single-particle Boltzmann Transport Equation and a simplified straight line motion taking

into account electric field barrier overcome probability. In order to reproduce the behavior of a 3D structure with 2D simulations, it has been shown that a geometry correction factor is required. Nodes' sensitivities are therefore corrected with the missing third dimension information, which has been found through experimental data to increase linearly with the nodes' width. Sensitivities of both PhotoDiode and Storage Node are consequently exploited to compute the Parasitic Light Sensitivity of the given pixel structure.

Thanks to the use of the developed model, it has been shown how light impinging onto the Storage Node region leads to the photo-generation of charges that directly contribute to the Parasitic Light Sensitivity of the sensor. In FrontSide Illuminated (FSI) CMOS Image Sensors, direct light collection has an important impact at shorter wavelengths, where a greater density of charges is generated in a shallow region close to the Si/SiO_2 interface and thus inside the Storage Node volume. Simple shielding of the Storage Node area exploiting the interconnection metallic layers may not be as trivial as it seems. Given the increasing reduction of feature dimensions in CMOS Image Sensors, light diffraction appears to play a crucial role; light shielding layers do not produce a perfectly shadowed zone, thus a non-negligible amount of light may impinge onto the Storage Node region.

On the other hand, it has been shown that free charges may as well affect the light sensitivity of the Storage Node, thus leading to performance degradation in Global Shutter CMOS Image Sensor due to an increase of the Parasitic Light Sensitivity. Charges can be photo-generated in neutral regions, i.e. regions without the presence of an electric field, as for example deeper in the epitaxial layer. Given a diffusion length that is generally higher than the pixel dimensions at given epitaxial layer doping concentration of $10^{15}\,\mathrm{cm}^{-3}$ (or even lower) at standard temperature, these charges can randomly diffuse and being collected by the Storage Node. This phenomenon is particularly important at longer wavelengths, since charges photo-generation deeper in the epitaxial layer. Diffusion barriers like the PWELL are generally exploited to block charges from diffusing towards certain areas, but their efficiency may be reduced given the energy of the diffusing charge and the strength of the barrier electric field. These results aim to lead the imaging community towards promoting Parasitic Light Sensitivity characterization at multiple wavelengths, as it has been shown that the pixel Parasitic Light Sensitivity is strongly function of the impinging wavelength, also given its dual nature dominated by the optical generation in the visible range and by charge diffusion in the NIR range.

TCAD simulations coupled with FDTD simulations have been exploited to similarly model the Parasitic Light Sensitivity. Based on the drift-diffusion model, TCAD simulations require previous knowledge on the charge photo-generation, differently from the two models presented. Coupled TCAD-FDTD simulations have been compared to both developed models, showing similar behavior. The advantage of the developed models over coupled TCAD-FDTD simulations lies in the reduced computational time required to generate results when dealing with multiple illumination conditions on the same structure, as allowed by the independence criteria. When N different illumination conditions have to be reproduced, coupled FDTD-TCAD simulations would require N FDTD simulations and N TCAD simulations, for a total of $2N$ simulations. On the other hand, the developed model would require only one transport

simulation in addition to the FDTD simulations, for a total of $N + 1$ simulations.

The developed model has moreover been compared to experimental results, showing a good reproduction of the Parasitic Light Hardness (1/PLS) behavior with respect to impinging wavelength. On the other hand, the modeled PhotoDiode and Storage Node Quantum Efficiencies show substantial differences with the experimental result in the short wavelength domain. Reasons behind this difference have been found in the poor availability of the technological process details, notably in the modeling of the Back End Of Line layers, thus leading to approximation of light propagation and charge photo-generation that are highly dependent on the refractive index and thickness of the mentioned layers.

Aim of the developed model is to serve as a fast tool for pixel designers to exploit to improve the Parasitic Light Sensitivity performances of Global Shutter CMOS Image Sensors in a more efficient way with respect to the use of TCAD simulations. Nevertheless, the developed model has its limitations, as for example the requirement for an accurate build-up of the electric field map (for the Boltzmann Transport Equation model) or the modeling of the electric field barrier overcome probability (for the Straight Line model) which may require additional work for setting-up the model for a new technology. In addition, calibration of the model with experimental results may also be required, given its 2D nature. Further on, the method has been developed with the aim in modeling Parasitic Light Sensitivity when the PhotoDiode is not in saturation; in this latter case, charges may spillover towards the Storage Node thus leading to an apparent increase in its light sensitivity. The developed model is not able to describe this situation, so TCAD simulations must be exploited for a more comprehensive analysis.

In the third chapter of this work the Straight Line model has been used to quantify the impact of design elements on the image sensor Parasitic Light Sensitivity. The role of light shielding through use of metallic interconnection layers has been investigated. In accordance with the Fresnel theory of diffraction, it has been shown that the Parasitic Light Sensitivity performances are dominated, especially at shorter wavelengths ($\lambda < 650\,\text{nm}$), by the lowest metal shielding level; the addition of supplementary metal shielding levels is often negligible. At longer wavelengths, the impact of direct light collection caused by light diffraction is mitigated by the deeper charge generation; the choice of the shielding metal layer shows therefore a milder impact. Mitigation of diffraction impact on the Storage Node light sensitivity has been sought via the positioning of the metal shielding layer over the Storage Node. It has been shown that a large coverage of the Storage Node, i.e. designing a shielding layer of bigger dimensions with respect to those of the Storage Node helps in reducing the light sensitivity of the latter. It is nevertheless important to pay attention to the coverage of the shielding metal layers, since coverage of the PhotoDiode will lead to a reduction of the PhotoDiode light sensitivity thus setting an upper limit to the convenience of Parasitic Light Sensitivity improvement via metallic layer coverage. The application of these rules of thumb for improvements in the Global Shutter Efficiency performances are nevertheless limited by the exploited technology. It has been widely shown in literature that the Tungsten Buried Light Shield (WBLS) is the preferred choice for an improved Stoarge Node shielding, limiting the application of the metal interconnection layers as light shields to technologies that do not

allow for the integration of a WBLS.

The impact of micro-lens on Parasitic Light Sensitivity performances have been analyzed, given their ability to convey light towards a focal point and thus increase the PhotoDiode light sensitivity. Simulations have shown that the presence of micro-lens not only increases the light impinging onto the PhotoDiode region, but it further reduces the amount of light impinging onto the Storage Node region. Furthermore, simulations have been carried on the shift of micro-lens center, in the aim of further reducing the photo-generation of charges in the surrounding area of the Storage Node; it has been shown that a slight shift in the micro-lens center helps in achieving this effect, nevertheless the PhotoDiode light sensitivity may be affected up to a point where it drastically drops, thus limiting the improvements on the Parasitic Light Sensitivity performances. A precise positioning of the micro-lens center may nevertheless help the pixel designer to fine tune both Parasitic Light Sensitivity and PhotoDiode light sensitivity to requirements. The presence impact of micro-lens has been experimentally proven. It has been shown that the micro-lens drastically improves the performances, especially at short wavelengths. Nevertheless, performance improvements at longer wavelengths are mitigated, given the weaker focusing power; in the longer wavelength region the Storage Node size has proven to be of crucial importance with respect to the micro-lens presence. Nevertheless, studies in literature have presented improved light confinement through the coupled use of micro-lens and light guide. In this latter case, the exploitation of the micro-lens center shift may be limited, and thus reduced to technologies not allowing for a light guide integration.

In the fourth chapter of this work, a standard metric for measuring Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors has been developed, giving no existing guidelines in the EMVA 1288 standard for this scope. The metric is based on a classical Quantum Efficiency measurement on the PhotoDiode plus the development of a Quantum Efficiency measurement on the Storage Node. It results easily applicable to every type of charge storage Global Shutter as well as voltage storage ones. The developed metric has been tested on a 5T pixels Global Shutter array; experimental results show the possibility to accurately measure the Parasitic Light Sensitivity as function of wavelength.

The second part of the fourth chapters of this work aims to develop a model of the output of CMOS Image Sensor operated in the Global Shutter mode, thus taking into account the signal induced by the non-negligible Parasitic Light Sensitivity. Validity of the model has been proven via experimental measurements, thus showing linear behavior with respect to the row number and the illumination conditions.

Given the linear behavior of the model, different frame post-process correction methods have been foreseen in order to mitigate the effect of Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors. Post-process correction methods are exploited as a cost-effective way to mitigate te problem of Parasitic Light Sensitivity in Global Shutter CMOS Image Sensor, without the need to explore the expensive route of technological process improvement. Correction methods have been developed for a 6T charge based storage Global Shutter CMOS Image Sensor, given the impossibility of exploiting 5T pixels for both Global Shutter Integrate While Read operation and correction. Nevertheless, given the use of a supplementary

correction frame, the minimum sensor frame rate is halved with respect to normal operation. The advantage of the developed correction methods with respect to existing methods in literature lies in the fact that they are especially developed to sample light intensity during the storage & readout phase, thus allowing to retrieve the amount of parasitic charges that have reached the Storage Node during this phase. As a drawback, these methods require an accurate characterization of the per-pixel Parasitic Light Sensitivity all over the sensor; the use of per-pixel Parasitic Light Sensitivity may lead to correction inaccuracies when dealing with polychromatic illumination and pixels not integrating color filters, as the Parasitic Light Sensitivity varies as function of wavelength. Nevertheless, the developed methods show promising results, making them an interesting cost-effective alternative to pixel Global Shutter Efficiency improvement by process, though it remains crucial to validate these theoretical methods through experimental results.

Outlook

This work has presented a comprehensive understanding of the phenomena related to Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors. Nevertheless, there are some parameters that still remain to be characterized. Future works may seek a better understanding of the behavior of Parasitic Light Sensitivity as function of the operating temperature; this would require a slight modification of the model to include scattering, which is known to be temperature dependent. A complete simulation and characterization of the pixel response to light impinging angle in both vertical and horizontal directions may be sought; simulations would allow to test the different pixel structures at different impinging angles in order to choose the most suited design for the required application. Finally, future works may seek for the behavior of Parasitic Light Sensitivity at different doping concentrations, as for example exploiting a high-resistive epitaxial layer to increase the PhotoDiode space charge region and thus improving the PhotoDiode light sensitivity, or exploring the various PWELL doping concentrations to improve the understanding on the potential barrier efficiency at different wavelengths.

The optical and transport simulations presented in this work have been performed in 2D. Two-dimension modeling of structure can be satisfactory when no variations are appreciable in the third dimension. Nevertheless, when more complex structures have to be taken into account and modeled, as for example the accurate modeling of micro-lenses, the non-rectangular shapes of the PhotoDiode or the Storage Node, 3D simulations are mandatory. The development of a 3D charge transport model are therefore required. 3D simulations may also be exploited to validate the 2D simulations and the geometrical correction factor previously presented. 3D simulations are extremely time consuming, thus requiring high computing power. Nevertheless, they are becoming a viable option given the continuous shrinkage in the pixel pitch. The 3D model would inherit the steady-state nature of the 2D model, thus having an advantage in terms of simulation time with respect to coupled FDTD-TCAD simulations when different illumination conditions have to be modeled.

It has been shown that optical simulations, especially the ones exploiting the FDTD method, are extremely sensitive to the material modeling, as for example thickness and refractive index; an approximate knowledge of the material properties can lead to approximate simulation results and thus inaccuracies in the pixel modeling. It is widely known that foundries are reluctant to unveil information on their technological process; a better knowledge of the material properties as well as the different deposited layers to produce the pixel array would allow to improve the modeling accuracy.

Finally, post-process correction methods have been presented for both operation modes of Global Shutter CMOS Image Sensors, though the method efficiency has not yet been proven by experimentally. Future works may focus on the experimental application and test of the various post-process correction methods presented, thus characterizing their efficiency and the associated noise. Literature has shown post-process correction methods as a viable option with which to mitigate the Parasitic Light Sensitivity issue [SJI19]; [Ge+19]; validation of the presented post-process correction methods may result in an additional cost-effective way to improve Global Shutter CMOS Image Sensor performances.

Appendix A

Importing Lumerical Optical Generation data into Synopsis Sentaurus

Given the desire to use the Lumerical Inc. suite to perform FDTD simulations (being preferred to the FDTD solver integrated in the Synopsys suite), the Optical Generation profiles resulting from the latter must be imported into Synopsis Sentaurus to perform coupled FDTD+TCAD simulations. The code exploited for this purpose is a adaptation of the one presented in the Annex Michael Kelzenberg's thesis [Kel10]. The script has been rendered as a function for an easier access to different files in different folders. The resulting function is the following, in MATLAB© code:

```
1 function [  ] = Lumerical2Sentaurus( folderSEN, folderLUM, fileName_sen,
    fileName_lum )
2 %Lumerical2Sentaurus Lumerical2Sentaurus(folderSEN,folderLUM,...
3 %    fileName_sen,fileName_lum)
4
5 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
6 % MATLAB script for importing arbitrary profiles onto DF-ISE simulation
7 % grids for use with Sentaurus TCAD.
8 %
9 % Michael Kelzenberg, 2010
10 % Federico Pace, 2020
11 %
12 % This script reads a DF-ISE .dat file to determine the spatial coordinates of
13 % of each grid point. It then generates a new .dat file containing an
14 % OpticalGeneration profile that was calculated by FDTD. The key input/output
15 % settings and the mapping function are indicated by comments in the code.
16 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
17 %DAT file
18 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
19 %This should be a valid DF-ISE .dat file (i.e. generated by mesh or
20 %noffset3d). The meshing program must be scripted to store the x- and y-
21 %position of each vertex of the grid as "PMIUserField0" and
22 %"PMIUserField1", respectively.
23 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
24 datFile = [fileName_sen '.dat'];
25 grdFile = [fileName_sen '.grd'];
26 %FDTD MAT file %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
27 %This should be the Matlab MAT file generated by the Lumerical CAD script
28 %including:
29 % x_Pabs, y_Pabs -> specification of grid (m)
30 % wavelength -> Central wavelength of simulation (m)
31 % Pabs* -> Matrix of power absorption (W/m3)
32 % *these variables followed by '_pavg' corespond to partial spectral averaging
33 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
34 if nargin > 3
35     FDTDFile = fileName_lum;
36     if ~strcmp(FDTDFile(end-3:end),'.mat')
37         FDTDFile = [FDTDFile '.mat'];
38     end
39 else
40     FDTDFile = 'Lumerical_export_2D.mat';
41 end
42 light_speed = 299792458; % speed of light m/s
43 h_planck = 6.626e-34; % Planck constant J*s
44 
45 %Regions to process %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
46 %These are the regions to perform the optical generation mesh conversion.
47 %This must be a cell array of region names, including double-quotes (")
48 %around each region name!!!
49 % Example syntax: regionsToProcess = {'"Base_region"', "Emitter_region"' };
50 %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
51 % PROCESS ALL REGIONS
52 
53 %Number of data values to output per line in output DAT file
54 numperline = 10;
55 
56 % Check if folderSEN is acceptable
57 folderSEN = strrep(folderSEN,'\','/');
58 if ~strcmp(folderSEN(end),'/')
59     folderSEN = [folderSEN '/'];
60 end
61 
62 % Check if folderLUM is acceptable
63 folderLUM = strrep(folderLUM,'\','/');
64 if ~strcmp(folderLUM(end),'/')
65     folderLUM = [folderLUM '/'];
66 end
67 if ~strcmp(folderLUM(end-4:end),'DATA/')
68     folderLUM = [folderLUM 'DATA/'];
69 end
70 
71 disp(folderLUM);
72 
73 disp('');
74 disp('----------------------------------------------------------------');
75 disp('Lumerical2Sentaurus Version 1.0');
76 disp('(c) 2020 Federico Pace');
77 disp('ISAE-SUPAERO');
78 disp('----------------------------------------------------------------');
79 disp('');
80 
81 disp(['Opening DAT file ' datFile ]);
```

```
82
83 grd = fopen([folderSEN datFile]);
84 if (grd < 1)
85     error(['Error opening file ' datFile ' for reading.']);
86 end
87
88 if ( ~isequal( fgetl(grd), 'DF-ISE text'))
89     disp('Error with grid file format: It might not be a DF_ISE text file.');
90     disp('Please double-check input file. The first line should read:');
91     disp(' DF-ISE text');
92     error('File parse error');
93 end
94 fln = 1;
95
96 verts = [];
97 regions = {};
98
99 nl = fgetl(grd); fln=fln+1;
100 while( isempty( regexp(nl, 'nb_vertices *= *[0-9]+', 'once') ) && ~feof(grd) )
101     nl = fgetl(grd); fln=fln+1;
102 end
103 tmp=regexp(nl, '[0-9]+','match');
104 numverts = str2num(tmp{1});
105 disp([' File reports ' num2str(numverts) ' vertices']);
106
107 nl = fgetl(grd); fln=fln+1;
108 while( isempty( regexp(nl, 'nb_edges *= *[0-9]+', 'once') ) && ~feof(grd) )
109     nl = fgetl(grd); fln=fln+1;
110 end
111 tmp=regexp(nl, '[0-9]+','match');
112 numedges = str2num(tmp{1});
113 disp([' File reports ' num2str(numedges) ' edges']);
114
115 nl = fgetl(grd); fln=fln+1;
116 while( isempty( regexp(nl, 'nb_elements *= *[0-9]+', 'once') ) && ~feof(grd) )
117     nl = fgetl(grd); fln=fln+1;
118 end
119 tmp=regexp(nl, '[0-9]+','match');
120 numelems = str2num(tmp{1});
121 disp([' File reports ' num2str(numelems) ' elements']);
122
123 nl = fgetl(grd); fln=fln+1;
124 while( isempty( regexp(nl, 'nb_regions *= *[0-9]+', 'once') ) && ~feof(grd) )
125     nl = fgetl(grd); fln=fln+1;
126 end
127 tmp = regexp(nl, '[0-9]+','match');
128 numregions = str2num(tmp{1});
129 disp([' File reports ' num2str(numregions) ' regions']);
130
131 %Advance to data section of file...
132 nl = fgetl(grd); fln=fln+1;
133 while( isempty( regexp(nl, 'Data.*\{', 'once') ) && ~feof(grd) )
134     nl = fgetl(grd); fln=fln+1;
135 end
136
```

```
137 if feof(grd)
138     disp('Unexpected end-of-file, no data processed.');
139     disp(['Line: ' num2str(fln)]);
140     error('File parse error.');
141 end
142
143 regionArray = [];
144 disp(' ');
145 disp('Reading data points...');
146
147 %Main reading loop. Look for PMIUserField 0 or 1 data sets...
148 while ~feof(grd)
149
150     nl = fgetl(grd); fln=fln+1;
151     while ( isempty( regexpi(nl,'\s*function\s*=\s*PMIUserField[01]','once'))...
152             && ~feof(grd) )
153         nl = fgetl(grd); fln=fln+1;
154     end
155
156     if feof(grd)
157         break;
158     end
159
160     tmp = regexp(nl, '[01]','match');
161     axisNumber = str2num(tmp{1});
162
163     nl = fgetl(grd); fln=fln+1;
164     while ( isempty( regexpi(nl, '\s*validity\s*=\s*\[\s*".*"\s*\]', 'once'))...
165             && ~feof(grd) )
166         nl = fgetl(grd); fln=fln+1;
167     end
168
169     if (feof(grd))
170         error(['File Parse Error near line ' num2str(fln)]);
171     end
172     tmp = regexp(nl, '".*"','match');
173     regionName = tmp{1};
174     nl = fgetl(grd); fln=fln+1;
175     while ( isempty( regexpi(nl, '\s*Values\s*\(\s*[0-9]+\s*\)', 'once') )...
176             && ~feof(grd) )
177         nl = fgetl(grd); fln=fln+1;
178     end
179
180     if (feof(grd))
181         disp(['File Parse Error near line ' num2str(fln)]);
182         break;
183     end
184
185     tmp = regexp(nl, '[0-9]+','match');
186     numElems = str2num(tmp{1});
187
188     dataPoints = [];
189     while (1)
190         nl = fgetl(grd); fln = fln+1;
191         if(isempty(regexp(nl,'[0-9]+', 'once') ) )
```

```
192             break;
193         else
194             thisline = regexp(nl,'[\.\-\e\E\+0-9][\s\.\-\e\E\+0-9]*','match');
195             thisline = thisline{1};
196             dataPoints = [dataPoints str2num(thisline)];
197         end
198         if ( ~isempty(regexp(nl,'}','once') ))
199             break;
200         end
201     end
202 
203     disp([' Region ' regionName ' read ' num2str(length(dataPoints)) '/' ...
204         num2str(numElems) ' elements for axis ' num2str(axisNumber) ]);
205 
206     %Error if data points disagree with number stated in header
207     if ( numElems ~= length(dataPoints) )
208         disp('Error: number of data points does not match file header');
209         disp(['Parse error near line ' num2str(fln)]);
210         error(['File structure error in region ' regionName]);
211     end
212 
213     existingRegion = 0;
214     for n=1:length(regionArray)
215         canRegion = regionArray{n};
216         if (isequal(regionName,canRegion.name))
217             existingRegion = n;
218         end
219     end
220 
221     if (existingRegion)
222         if (axisNumber == 0)
223             regionArray{existingRegion}.xdata = dataPoints;
224         else
225             regionArray{existingRegion}.ydata = dataPoints;
226         end
227 
228         if ~isequal( length(regionArray{existingRegion}.xdata), ...
229                 length(regionArray{existingRegion}.ydata) )
230             disp(['Error: number of x data points does not match number of ' ...
231                 'y data points']);
232             error(['File structure error in region ' regionName ]);
233         end
234 
235     else
236         newRegion.name = regionName;
237         if (axisNumber == 0)
238             newRegion.xdata = dataPoints;
239             newRegion.ydata = [];
240         else
241             newRegion.ydata = dataPoints;
242             newRegion.xdata = [];
243         end
244         newRegion.gdata = zeros(size(dataPoints));
245         regionArray{end+1} = newRegion;
246     end
```

```
247
248 end
249
250 for n=1:length(regionArray)
251     if ~isequal( length(regionArray{n}.xdata), length(regionArray{n}.ydata) )
252         disp(['Error: number of x data points does not match number of '...
253             'y data points']);
254         error(['File structure error in region ' regionArray{n}.name ]);
255     end
256 end
257
258 disp(' ');
259 disp('Completed reading DAT file');
260 disp([' Read ' num2str(length(regionArray)) ' region(s)']);
261 disp(' ');
262 fclose(grd);
263
264 % Load MAT file containing the Optical Generation output from Lumerical
265 disp(' ');
266 disp(['Loading MAT file ' FDTDFile ]);
267 if length(FDTDFile) > 20
268     add_name = FDTDFile(17:end-4);
269 end
270 % Use external function OptGenLumerical to easily load Optical Generation
271 % and the axis
272 [x_Pabs,y_Pabs,wavelength,OptGen] = OptGenLumerical(folderLUM,'name',add_name);
273
274 x_Pabs = x_Pabs - min(x_Pabs); % Bring the minimum to zero to match with
    Sentaurus structure
275
276 wavelength = [wavelength;0]; % add 0 for null Optical Generation rate
277
278 for i_wav = 1:length(wavelength)
279     %The output dat and grd files are used for monochromatic-illumination device
280     % physics simulations (the next step in this experiment).
281     outputFile = ['nLUM_wav' num2str(wavelength(i_wav)*1e9) '_optgen.dat'];
282     outputGrid = ['nLUM_wav' num2str(wavelength(i_wav)*1e9) '_optgen.grd'];
283
284     E_photon = h_planck*light_speed/wavelength(i_wav); % photon energy
285     if wavelength(i_wav) == 0
286         optGenMatrix = zeros(size(OptGen(:,:,1))); % null Generation rate
287     else
288         optGenMatrix = OptGen(:,:,i_wav)/E_photon*1e-6; % conversion from W/m^3
          to #/(cm^3*s^1) (using photon energy)
289     end
290     %
      %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

291     %Mapping function:
292     newoptgen = @(xi, yi) interp2(x_Pabs,y_Pabs, optGenMatrix, xi*1e-6,yi*1e-6,'
      linear',0 );
293     %
      %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

294     % Now ready to write the output data file...
```

```
295     disp(['Opening output file ' outputFile ]);
296     ogo = fopen([folderSEN outputFile],'w');
297     if (ogo < 1)
298         error(['Error opening file ' outputFile ' for writing.']);
299     end
300
301     fprintf(ogo, 'DF-ISE text\n\n');
302     fprintf(ogo, ...
303         'Info {\n version = 1.0\n type = dataset\n dimension = 2\n');
304     fprintf(ogo, ' nb_vertices = %d\n nb_edges = %d\n nb_faces = 0\n',...
305         numverts, numedges);
306     fprintf(ogo, ' nb_elements = %d\n nb_regions = %d\n datasets = [ ',...
307         numelems, numregions);
308     for n=1:length(regionArray)
309         fprintf(ogo,'"OpticalGeneration" ');
310     end
311     fprintf(ogo, ']\n functions = [ ');
312     for n=1:length(regionArray)
313         fprintf(ogo,'OpticalGeneration ');
314     end
315
316     fprintf(ogo, ']\n}\n\nData {\n\n');
317     for n=1:length(regionArray)
318         reg = regionArray{n};
319         disp( ['Proessing Optical Generation for region ' reg.name '...'] );
320         fprintf(ogo,['Dataset ("OpticalGeneration") {\n function = '...
321             'OpticalGeneration\n type = scalar\n dimension = 1\n'...
322             'location = vertex\n validity = [ ' reg.name ' ]\n' ] );
323         fprintf(ogo, ' Values (%d) {\n', length(reg.xdata) );
324         gdata = zeros(size(reg.xdata));
325         nl = 1;
326         for nv=1:length(reg.xdata)
327             ogi = newoptgen(reg.xdata(nv), reg.ydata(nv));
328             fprintf(ogo, ' %22e', ogi);
329             gdata(nv) = ogi;
330             nl = nl + 1;
331             if (nl > numperline)
332                 fprintf(ogo, '\n');
333                 nl = 1;
334             end
335         end
336         if (nl > 1)
337             fprintf(ogo,'\n');
338         end
339         fprintf(ogo, ' }\n}\n\n');
340         disp( [' ' num2str(length(reg.xdata)) ' processed'] );
341         regionArray{n}.gdata = gdata;
342     end
343
344     fprintf(ogo,'\n\n}');
345     fclose(ogo);
346     disp(['Finished writing output file ' outputFile ]);
347     disp(' ');
348     disp(['Copying from grid file: ' grdFile]);
349     copyfile([folderSEN grdFile],[folderSEN outputGrid]);
```

```
350     disp(['To grid file: ' outputGrid]);
351     disp(' ');
352     disp(['Processing file ' num2str(i_wav) ' complete!']);
353
354 end
355
356 disp('Total processing complete!');
357
358 end
```

Hereafter the MATLAB© code of the highlighted function on line 272.

```
1 function [ x0, y0, wavelength, Pabs, SourceIntensity, SourcePower] =
    OptGenLumerical( folderID, varargin )
2 %OptGenLumerical This function integrates the optical generation extracted
3 %from Lumerical
4 %   [ x0, y0, lambda, Pabs, source_intensity, source_power] = OptGenLumerical(
    folderID, varargin )
5 %      gives as output the intensity of the source in W/m2
6 %   [ x0, y0, lambda, Pabs] = OptGenLumerical( folderID, 'name', appendixName )
7 %      add an appendix to the required OpticalGeneration file
8
9 % Start with preset values, modify them in case needed;
10 mirror = 0;
11 add_name = '';
12
13 for i = 1:round(length(varargin)/2)
14     switch varargin{2*i-1}
15         case 'mirror'
16             mirror = varargin{2*i};
17         case 'name'
18             add_name = varargin{2*i};
19         otherwise
20             error('Check again the inputs.');
21     end
22 end
23
24 % Check if folderID is acceptable
25 if ~(strcmp(folderID(end),'\') || strcmp(folderID(end),'/'))
26     folderID = [folderID '/'];
27 end
28
29 % Load exported file from Lumerical
30 fileID = [folderID 'Lumerical_export' add_name '.mat'];
31 fid = fopen(fileID);
32 if fid ~= -1
33 %     M = importdata(fileID); % old import type. With two structures in the
34 %     file it is impossible to use it
35     S = load(fileID); % M is loaded, SP also if existing
36     if isfield(S,'M')
37         M =  S.M;
38     else
39         M = [];
```

```
40      end
41      if isfield(S,'SP')
42          SP = S.SP;
43      else
44          SP = [];
45      end
46
47      % Get simulation data
48      if length(M.x) == 1 % for 3D simulations
49          x0 = reshape(M.y,[],1);
50          y0 = reshape(M.z,[],1);
51      else
52          x0 = reshape(M.x,[],1);
53          y0 = reshape(M.y,[],1);
54      end
55      y0 = -flipud(y0);
56      wavelength = reshape(M.wavelength,[],1);
57
58      % Check if Pabs* data exists and grab it
59      field_names = fieldnames(M);
60      find_pabs = [];
61      for i = 1:length(field_names)
62          if strncmp(field_names{i},'Pabs',4)
63              find_pabs = i;
64              break;
65          end
66      end
67 %      find_pabs = cellfun(@(c1) strncmp(c1,'Pabs',4),field_names);
68      if isempty(find_pabs)
69          error('Error: no Pabs* data have been found.')
70      end
71      Pabs_temp = M.(field_names{find_pabs});
72
73      % Reshape and turn the image in order to fit MATLAB standards: (Y,X,others)
74      sizePabs = size(Pabs_temp);
75      Pabs_temp = reshape(Pabs_temp,[length(x0) length(y0) sizePabs(3:end)]);
76      Pabs = rot90(Pabs_temp);
77      if mirror
78          Pabs = fliplr(Pabs);
79          x0 = -flipud(x0);
80      end
81
82      index_y = find(y0 >= 0);
83      Pabs = Pabs(index_y,:,:);
84      y0 = y0(index_y);
85
86      % Insert given source intensity to output variables
87      SourceIntensity = [];
88      if isfield(M,'source_intensity')
89          SourceIntensity = M.source_intensity'*1e-2; % conversion from uW/cm2 to W
            /m2
90      end
91
92      % Insert simulated source power to output variables
93      SourcePower = [];
```

```
94      if ~isempty(SP)
95          SourcePower = reshape(SP.source_power,[],1); % it should be already in W/
              m
96      end
97
98      % close file
99      fclose(fid);
100
101 else
102     error(['OptGenLumerical error: file Lumerical_export' ...
103         add_name '.mat not found in ' folderID]);
104 end
105
106
107 end
```

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[1] Federico Pace, Olivier Marcelot, Philippe Martin-Gonthier, Olivier Saint-Pé, Michel Breart de Boisanger, Rose-Marie Sauvage, Pierre Magnan "Modeling of Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors." In: *Proc. 2019 16th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD)*, Jul. 2019, pp. 101-104.

[2] Federico Pace, Olivier Marcelot, Philippe Martin-Gonthier, Olivier Saint-Pé, Michel Breart de Boisanger, Rose-Marie Sauvage, Pierre Magnan "An Efficient Method for Modeling Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors." In: *Proc. 2019 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, Sept. 2019.

[3] Federico Pace, Olivier Marcelot, Philippe Martin-Gonthier, Olivier Saint-Pé, Michel Breart de Boisanger, Rose-Marie Sauvage, Pierre Magnan "A Fast Method for Modeling and Optimizing Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors." In: *Proc. 49th European Solid-State Device Research Conference (ESSDERC)*, Sept. 2019, pp.230-233.

THÈSE

En vue de l'obtention du

DOCTORAT DE L'UNIVERSITÉ DE TOULOUSE

Délivré par l'Institut Supérieur de l'Aéronautique et de l'Espace

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Présentée et soutenue par

Federico PACE

Le 21 janvier 2021

Développement d'une méthode pour modéliser, caractériser et atténuer la sensibilité à la lumière parasite dans les imageurs CMOS à obturation globale

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Ecole doctorale : **GEETS - Génie Electrique Electronique,Télécommunications et Santé : du système au nanosystème**

Spécialité : **Photonique et Systèmes Optoélectronique**

Unité de recherche :
ISAE-ONERA OLIMPES Optronique, Laser, Imagerie Physique et Environnement Spatial

Thèse dirigée par
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Introduction

L'imagerie à haute-vitesse sans distorsions spatiales est devenue cruciale pour un large éventail d'applications telles que la vision industrielle, l'automobile, la reconnaissance faciale et de mouvement et l'imagerie de la Terre depuis l'espace [LMR13] ; [Mey14] ; [Vel+16]. Même si les performances des capteurs d'images CMOS (CIS) ont considérablement augmenté au fil des ans grâce aux efforts de l'industrie et de la recherche, permettant d'obtenir une plage dynamique (DR) élevée, une grande sensibilité et un faible bruit, le fonctionnement typique en obturation déroulante (RS) de ces capteurs limite la qualité de l'image des objets en mouvement rapide : l'exposition non synchrone de l'ensemble de la matrice de pixels, en mode d'obturation déroulante, est en effet la principale cause des distorsions spatiales. Les imageurs CMOS à obturation globale ont donc été développés pour résoudre ce problème. Un élément de stockage dans le pixel a été ajouté afin de permettre une séparation entre la phase d'exposition et la phase de lecture, permettant une exposition globale synchrone de la matrice de pixels [Tak+07]. Il est donc possible d'obtenir une imagerie sans distorsion, mais l'insertion d'un élément de stockage dans le pixel pose de nouveaux problèmes à résoudre tel que la sensibilité non négligeable de l'élément de stockage à la lumière parasite, en particulier dans le cas où un élément en stockage de charge est utilisé. Les faibles performances de suppression de la lumière parasite limitent fortement l'utilisation des capteurs d'images CMOS à obturateur global dans des environnements à haute vitesse et à forte luminosité.

La sensibilité à la lumière parasite (PLS) a été définie comme la figure de mérite pour évaluer l'efficacité des imageurs CMOS à obturation globale à supprimer la lumière parasite pouvant induire une perturbation indésirable dans l'ensemble du réseau. Diverses études ont été présentées dans le but de réduire la sensibilité à la lumière parasite et d'améliorer ainsi les performances des imageurs CMOS à obturation globale par des améliorations technologiques ou de conception. Néanmoins, peu d'études présentent un modèle de sensibilité à la lumière parasite, certaines ne présentant que des résultats simulés sans donner aucun détail sur le modèle exploité [Yok+18] et d'autres ne développant un modèle que pour un type spécifique de pixels [Roy+19]. De plus, un manque général de spécificité et de modélisation de la sensibilité à la lumière parasite en fonction de la longueur d'onde incidente a été constaté. Cela devient particulièrement important lorsqu'on sait que des applications telles que la reconnaissance faciale et la reconnaissance de mouvements nécessitent souvent une détection proche infrarouge (NIR) (850 - 950 nm), alors qu'il est courant sur le marché de ne caractériser les performances de la sensibilité à la lumière parasite qu'à une longueur d'onde de 550 nm.

L'un des objectifs de ce travail est de développer un cadre permettant d'améliorer les performances des imageurs CMOS à obturation globale grâce à une compréhension approfondie de la collection de la lumière parasite par le nœud de stockage. La base de ce travail est le développement d'une méthode de modélisation de la sensibilité à la lumière parasite des imageurs CMOS à obturation globale, de la longueur d'onde et de paramètres de conception de pixels donnés en entrée. Le chapitre 1 est axé sur l'explication des phénomènes à l'origine de la sensibilité non négligeable à la lumière parasite des imageurs CMOS à obturation globale

et de leur modélisation. Une méthode efficace en régime permanent est présentée, exploitant les simulations dans le domaine temporel aux différences finies (FDTD) pour modéliser les propriétés électromagnétiques de la lumière à l'intérieur des structures de pixels. Les propriétés de transport de charge à l'intérieur de la région active du silicium sont modélisées par l'équation de transport de Boltzmann à une seule particule, mise en œuvre dans MATLAB®, et avec le modèle de dérive-diffusion utilisant des simulations TCAD pour comparaison.

Dans le chapitre 2, le modèle développé est exploité comme un outil rapide pour réduire la sensibilité à la lumière parasite des capteurs d'images CMOS à obturateur global. Différentes conceptions de pixels sont modélisées et comparées, dans le but de donner des lignes directrices pour une conception efficace des pixels à obturation globale. Une partie importante de ce chapitre est notamment consacrée à la compréhension des propriétés d'écrantage de la lumière des couches d'interconnexion métalliques et à leur exploitation optimale pour protéger l'élément de stockage dans le pixel contre la lumière parasite incidente directe. Pour prouver les résultats de la simulation, des structures de test ont été développées et caractérisées dans le chapitre 3.

Bien qu'elle soit traitée comme une figure de mérite, il n'existe pas de méthode standard pour mesurer la sensibilité à la lumière parasite des capteurs d'images CMOS à obturateur global. Certaines techniques de mesure ont été présentées dans la littérature [Mey+11], bien qu'elles puissent ne pas s'appliquer pour une caractérisation générale de chaque pixel de la matrice. Le chapitre 3 présente un développement d'une métrique standard pour la mesure de la sensibilité à la lumière parasite des imageurs CMOS à obturation globale qui peut être appliquée à la grande variété d'imageurs CMOS à obturation globale sur le marché. Cette mesure s'appuie sur les mesures d'efficacité quantique (QE), qui sont largement connues dans la communauté des capteurs d'images et bien normalisées. La métrique permet une caractérisation par pixel à différentes longueurs d'onde et à différents angles d'incidence, permettant ainsi une caractérisation plus complète de la sensibilité à la lumière parasite des capteurs d'images CMOS à obturateur global.

Un effort important a été consacré à l'amélioration des performances des capteurs d'images CMOS Global Shutter grâce à des améliorations technologiques. Inversement, peu d'études ont été réalisées sur les méthodes de correction en post-traitement pour atténuer le problème de la sensibilité à la lumière parasite [SJI19] ; [Ge+19]. Bien qu'elles limitent souvent le nombre de trames par seconde, les méthodes de correction en post-traitement peuvent constituer un moyen rentable de réduire la sensibilité à la lumière parasite, en particulier lorsque l'amélioration technologique n'est pas une option viable. Dans le chapitre 3, différentes méthodes de correction en post-traitement sont présentées en tenant compte des différents modes de fonctionnement de l'obturation blobale (déclenché, également appelé Integrate Then Read (ITR) ou pipeline, également appelé Integrate While Read (IWR)). L'augmentation du panel de méthodes de correction en post-traitement permet à l'utilisateur de choisir celle qui convient le mieux vis à vis des applications requises.

Chapitre 1

Développement d'une méthode de modélisation de la sensibilité à la lumière parasite

La sensibilité à la lumière parasite (PLS) définit la sensibilité du capteur pendant la phase d'intégration par rapport à la sensibilité du capteur pendant la phase de lecture. En d'autres termes, la sensibilité à la lumière parasite définit la quantité de lumière, autrement dite lumière parasite, que le capteur "voit" pendant la phase de lecture par rapport à la quantité de lumière que le capteur "voit" pendant la phase d'intégration. Apparaissant pendant la phase de stockage et de lecture, la lumière parasite représente la quantité de lumière collectée par l'élément de stockage ; inversement, pendant la phase de fonctionnement, la lumière est collectée sur l'élément photosensible principal (la photodiode). On peut donc modéliser la sensibilité à la lumière parasite comme suit :

$$PLS = \frac{\mathscr{S}_{SN}}{\mathscr{S}_{PD}} = \frac{QE_{SN}}{QE_{PD}} \tag{1.1}$$

où $\mathscr{S}_{SN}$ et $\mathscr{S}_{PD}$ sont respectivement la sensibilité à la lumière du nœud de stockage et de la photodiode. Il peut être facilement démontré que la sensibilité à la lumière et l'efficacité quantique (QE) sont liées entre elles par une constante multiplicative, les deux façons de définir la sensibilité à la lumière parasite sont donc équivalentes.

La course constante à la réduction des dimensions des pixels complexifie la question de la sensibilité à la lumière parasite (PLS) des imageurs CMOS à obturation globale ; l'amélioration de la collection des charges par la photodiode (PD) est devenue de plus en plus difficile ainsi que le guidage du flux de photons vers des endroits spécifiques, en particulier dans les pixels de petites dimensions. De plus, même si la question de la sensibilité à la lumière parasite est largement connue dans la communauté scientifique et industrielle des capteurs d'images, son comportement concernant les paramètres de la lumière incidente reste assez flou ; la compréhension et la modélisation de la sensibilité à la lumière parasite sont donc nécessaires, fournissant des lignes directrices pour une amélioration efficace et rentable des capteurs d'images CMOS à obturateur global.

Il a déjà été démontré que la sensibilité à la lumière parasite est le résultat du rapport de deux efficacités quantiques. Nous savons que l'efficacité quantique définit le nombre d'électrons collectés sur le nœud considéré par rapport au nombre de photons incidents sur le pixel. Ce

paramètre peut être séparé en deux : η_o, qui est l'efficacité quantique optique, représentant le nombre de charges photo-générées dans la zone active du semi-conducteur, c'est-à-dire la couche épitaxiale sur laquelle le pixel est fabriqué, sur le nombre total de photons incidents (en considérant qu'un photon est capable de générer une paire électron-trou) ; η_i, qui est l'efficacité quantique interne, représentant le nombre de charges collectées sur le nombre de charges photo-générées.

Il y a deux mécanismes principaux à l'origine de la collection parasite :
— la lumière touchant directement le nœud de stockage, générant ainsi un certain nombre de paires électron-trou à l'intérieur même du nœud de stockage qui est fonction de la longueur d'onde de la lumière incidente ;
— des charges qui sont photo-générées ailleurs mais qui ont la possibilité et la capacité d'atteindre le nœud de stockage.

1.1 Photo-génération de charges

La modélisation commence par de la photo-génération de charges à l'intérieur de la couche épitaxiale de Silicium, en connaissant la longueur d'onde, l'angle d'incidence et son intensité lumineuse. Afin de choisir le meilleur outil pour modéliser la lumière incidente et la photogénération de charges, quelques éléments doivent être pris en compte :
— la diffraction de la lumière doit être modélisée avec précision par l'outil ;
— La densité de puissance de la lumière incidente dans la région du silicium, en fonction de l'intensité de l'onde incidente, doit être donnée comme résultat de l'outil. Nous voulons être en mesure de calculer la densité de charge photo-générée à l'intérieur du silicium, ce qui nécessite le calcul de la densité de photons incidents au moyen de la densité de puissance lumineuse ;
— l'outil doit être adapté aux dimensions de la structure que l'on veut modéliser. Notamment, l'objectif de l'outil de simulation sera de modéliser la lumière incidente sur un pixel, de quelques dizaines de microns carrés (pour les simulations 2D) ;
— les conditions limites périodiques sont nécessaires, en particulier si la modélisation d'une matrice de pixels est requise.

La méthode des différences finies dans le domaine temporel (FDTD) utilise les différences finies comme approximations des dérivées spatiales et temporelles qui apparaissent dans les équations de Maxwell. La résolution des équations de Maxwell garantit l'inclusion du phénomène de diffraction.

1.1.1 Simulation de la propagation de la lumière dans les structures de pixels

Dans une première approche, nous modéliserons la propagation des ondes lumineuses dans une structure de pixels en 2D. La Fig. 1.1 donne un exemple de la géométrie des pixels qui a été utilisée : la couche épitaxiale de silicium de 5 µm d'épaisseur ; les grilles en polysilicium

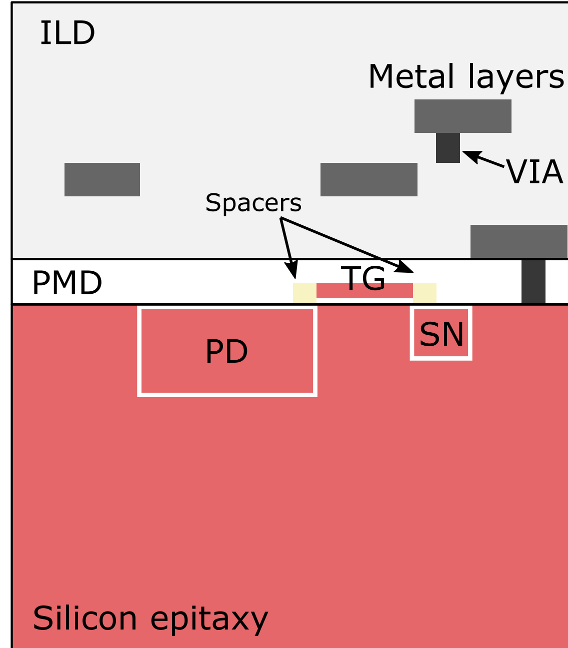

FIGURE 1.1 – Schéma d'une structure de pixels qui peut être modélisée dans des simulations FDTD, en suivant les spécifications connues d'une technologie sélectionnée, comme pour le diélectrique inter-couches (ILD), le diélectrique pré-métallique (PMD), les couches métalliques et les épaisseurs de la TG. La présence de la photodiode et du nœud de stockage est simplement symbolique pour une compréhension visuelle de leur emplacement.

avec leurs oxyde de grille SiO_2 et espaceurs en nitrure ; le pré-métal-diélectrique (PMD), qui est un oxyde spécifique déposé avant le dépôt de la première couche métallique ; le diélectrique inter-couches (ILD), qui est un oxyde spécifique déposé entre les couches métalliques ; et les éléments métalliques, comme les VIAs, en tungstène (W) et les couches métalliques, en Al.

1.1.2 Extraction des résultats : la carte de la densité du taux de génération optique

Des simulations optiques sont nécessaires pour extraire la densité du taux de photo-génération des charges G_{abs} à l'intérieur du volume de silicium. En général, les semi-conducteurs se comportent comme des absorbeurs et des émetteurs de rayonnement, bien que ce dernier soit négligeable dans le Silicium en raison de la bande interdite indirecte du matériau et de la recombinaison dominée par les pièges [SN06]. Par conséquent, le taux de photogénération peut être déterminé à partir de la divergence du vecteur de Poynting et exprimé en termes de magnitude du champ électrique $|\vec{E}|$ et de la partie imaginaire de la permittivité du matériau $\epsilon = \epsilon_0\, \epsilon_r$, comme indiqué par Eq. (1.2) [SN06] ; [PFC97], où E_{ph} est l'énergie du photon en fonction de la longueur d'onde, $\vec{S}$ est le vecteur de Poynting et $\Re\{\cdot\}$, $\Im\{\cdot\}$ représentent

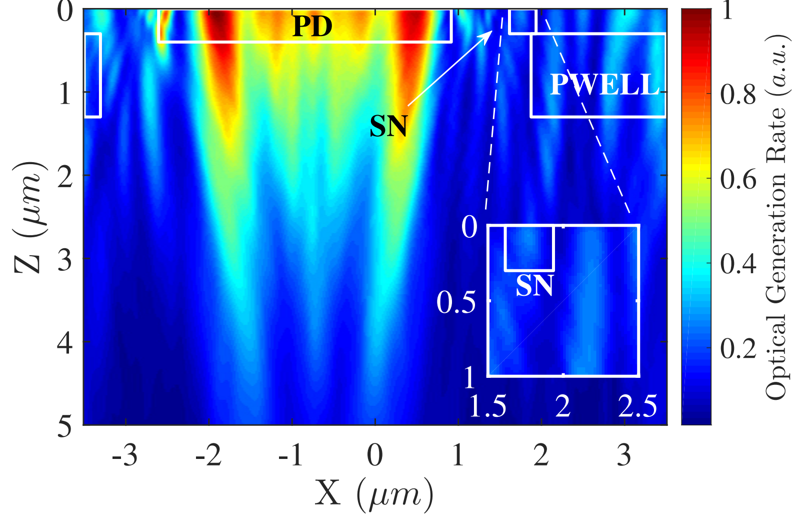

FIGURE 1.2 – Densité du taux de génération optique (G_{abs}) de la structure de pixels donnée dans la Fig. 1.1, résultat d'une simulation FDTD. Les emplacements de la photodiode, du nœud de stockage et du PWELL sont mis en évidence en blanc dans le seul but de donner une compréhension de la structure des pixels. Un agrandissement est présenté pour mettre en évidence la génération optique non négligeable dans la région du nœud de stockage malgré la présence d'une couche métallique pour protéger optiquement le nœud.

respectivement la partie réelle et la partie imaginaire.

$$G_{abs} = \frac{1}{E_{ph}} P_{abs} = \frac{1}{2\,E_{ph}} \Re\{\nabla \cdot \vec{S}\} = \frac{\pi f}{E_{ph}} \,|\vec{E}|^2 \,\Im\{\epsilon\} \tag{1.2}$$

La réponse en régime permanent du système permet d'obtenir un résultat de la photo-génération indépendant du temps ; $G_{abs}(x, y)$ représente les charges phot-générées par unités de temps et d'espace, également définies comme *densité de taux de génération optique*. Un exemple de G_{abs} dans l'espace peut être apprécié dans la Fig. 1.2, sur une couche épitaxiale de silicium de 5 µm d'épaisseur. Le grandissement montre qu'il y a une génération optique non négligeable à l'intérieur de la zone du nœud de stockage, malgré le fait que celui-ci soit protégé par une couche métallique, ce qui justifie l'intérêt de notre modélisation.

1.2 Modélisation du transport des charges

Compte tenu des conditions de séparabilité des phénomènes optiques et de transport, nous visons à développer une fonction qui pourrait tracer le comportement des charges photo-générées en un point de l'espace à l'intérieur de la couche épitaxiale en fonction de la distribution de son champ électrique ; pour être plus spécifique, le souhait est de développer une

méthode permettant de calculer la probabilité qu'un électron photo-généré en un point puisse être collecté par la région souhaitée, comme par exemple la PhotoDiode ou le Storage Node. Nous appellerons cette fonction *probabilité de collection*, qui représente essentiellement une fonction de pondération W.

L'efficacité quantique interne du nœud souhaité $\eta_{i,node}$ représente le nombre de charges photo-générées qui sont collectées par le nœud souhaité. Une intégration spatiale du produit entre G_{abs} et W_{node} donnerait comme résultat le nombre total de photo-électrons générés dans la couche épitaxiale qui peuvent atteindre le nœud souhaité, $N_{coll-node}$, comme indiqué dans l'équation suivante :

$$N_{coll,node} = \iiint G_{abs} \cdot W_{node} \cdot dV \tag{1.3}$$

où V est le volume de la couche épitaxiale. En d'autres termes, il serait possible de calculer l'efficacité quantique interne au moyen de l'équation suivante :

$$\eta_{i,node} = \frac{N_{coll,node}}{N_{abs}} = \frac{\iiint G_{abs} \cdot W_{node} \cdot dV}{\iiint G_{abs} \cdot dV} \tag{1.4}$$

dans laquelle nous avons utilisé l'Eq. (1.3) et le nombre total de charges photo-générées (dont nous rappelons qu'il est supposé être égal au nombre total de photons absorbés N_{abs}) comme donné par ce qui suit :

$$N_{abs} = \iiint G_{abs} \cdot dV. \tag{1.5}$$

1.2.1 L'équation du transport de Boltzmann

Une approche simplifiée de la solution de l'équation de transport de Boltzmann [JR83] ; [Hes12] a été choisie pour modéliser la propagation de la charge et créer la fonction de pondération souhaitée.

Pour effectuer la simulation, il faut donner l'energie initiale des charges E_{ini}. Il est possible de supposer que l'énergie initiale des charges dépendra de l'onde lumineuse incidente qui les a générées. Nous donnerons deux autres hypothèses pour modéliser l'énergie initiale des charges :

- après la photo-génération, l'énergie des photons est répartie de manière égale entre l'électron et le trou ;
- la paire électron-trou est générée à partir d'un électron situé au sommet de la bande de valence qui est promu à la bande de conduction.

Cette modélisation de l'énergie initiale entraîne une dépendance énergétique linéaire de la fréquence des ondes lumineuses, ou une dépendance inverse de la longueur d'onde des ondes lumineuses, comme le montre l'effet photoélectrique reproduit dans Eq. (1.6), où h est la constante de Planck non réduite, c la vitesse de la lumière et E_g le bandgap du semi-conducteur [KS01].

$$E_{ini} = \frac{1}{2}\left(\frac{h\,c}{\lambda} - E_g\right) \tag{1.6}$$

Enfin, les conditions limites doivent être prises en compte pour le bon fonctionnement de

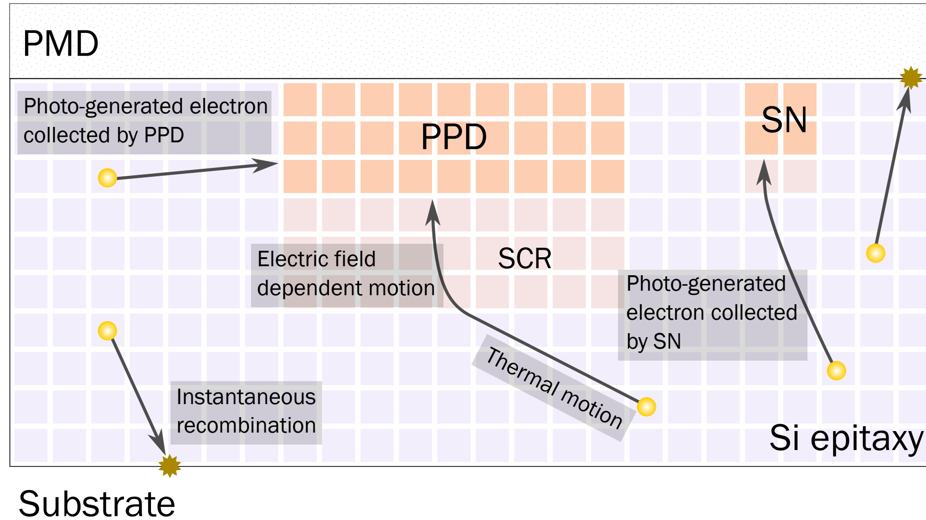

FIGURE 1.3 – Explication de l'équation du transport de Boltzmann modélisée à l'intérieur de la couche épitaxiale de silicium pour un seul pixel.

la simulation. Dans notre cas simplifié, nous supposerons que, lorsqu'elle atteint une surface quelconque, la charge simulée se recombine immédiatement et est donc considérée comme perdue.

La Fig. 1.3 résume la méthode développée pour modéliser la fonction de pondération de la probabilité de collection sur la couche épitaxiale de silicium. Le volume de la couche épitaxiale a été divisé en sous-voxels, des électrons N_{jet} sont simulés pour chaque voxel avec une énergie initiale dépendant de la longueur d'onde de la lumière incidente E_{ini} et un vecteur d'onde initial k_{ini}, la charge se déplace successivement selon l'équation du transport de Boltzmann simplifiée en fonction de la distribution du champ électrique ; la recombinaison instantanée aux conditions limites est prise en compte ; la fonction de pondération de la probabilité de collection est le résultat des charges collectées par point sur le nombre total de charges générées.

1.2.2 La propagation en ligne droite

Afin d'accélérer le processus de développement de la fonction de pondération (ou probabilité de collection), une approche plus simple et plus rapide a été modélisée. Le modèle suppose que les charges qui ont été photo-générées dans le volume épitaxial se propagent sur une ligne droite, avec une direction initiale aléatoire, sans l'influence d'un autre terme externe comme par exemple la diffusion ou le champ électrique local. Le modèle a l'avantage de n'utiliser que des facteurs géométriques pour comprendre si la charge photo-générée peut ou non atteindre le nœud souhaité, ce qui améliore considérablement le temps de simulation.

Le modèle de propagation en ligne droite (SL) présente certaines similitudes avec le modèle

de l'équation du transport de Boltzmann :
- le système analysé, c'est-à-dire la couche épitaxiale, est subdivisé en voxels pour permettre un calcul spatial de la fonction de pondération de la probabilité de collection ;
- toute charge atteignant les limites du système, le volume de la couche épitaxiale, avant d'être collectée par le nœud requis sera considérée comme perdue ;
- si une charge atteint un autre nœud Y pendant que nous construisons la fonction de pondération pour le nœud X, elle sera considérée comme perdue.

1.2.3 Calcul de la sensibilité à la lumière parasite

Pour calculer la sensibilité à la lumière parasite de l'imageur, nous avons besoin du rapport d'efficacité quantique de la photodiode et du nœud de stockage. Nous utiliserons l'intégration spatiale du produit entre G_{abs} et le W_{node}, ce qui donnera le rendement quantique du nœud sélectionné. Le calcul de la sensibilité à la lumière parasite est le suivant :

$$PLS = \frac{QE_{SN}}{QE_{PD}} = \frac{\iiint G_{abs} \cdot W_{SN} \cdot dV}{\iiint G_{abs} \cdot W_{PD} \cdot dV}. \tag{1.7}$$

1.3 Conclusions

La collection directe de photons consiste en des photons capables d'atteindre la surface du silicium dans la région où se trouve le nœud de stockage. Les méthodes de propagation de la lumière couramment disponibles, comme le ray-tracing, permettent de modéliser avec précision la réflexion, la réfraction et l'interférence de la lumière, bien que si la diffraction doit être prise en compte, les simulations FDTD sont mieux adaptées.

La collection de charges libres de diffuser se produit parce que certains photons, pénétrant profondément dans la région neutre de la couche épitaxiale de silicium, génèrent des paires électron-trou qui ne sont pas directement guidées par un champ électrique. Il est important de modéliser la propagation des charges photo-générées à l'intérieur de la couche épitaxiale de silicium pour comprendre les chemins préférés qui conduisent les charges vers le nœud de stockage.

Étant donné la longueur de diffusion élevée des porteurs dans le silicium, deux méthodes ont été développées pour créer une fonction de cartographie de la probabilité de collection afin de comprendre la probabilité qu'une charge atteigne une certaine région ; la première méthode consiste à appliquer l'équation de transport de Boltzmann à particule unique, étant donné une distribution simplifiée du champ électrique ; la seconde méthode consiste à modéliser la propagation des charges en ligne droite.

Chapitre 2

Optimisation de la conception des imageurs CMOS à obturation globale

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Le modèle développé peut servir de base pour déterminer les choix de conception pour l'optimisation des pixels et l'amélioration de l'efficacité d'obturation globale pour un procédé technologique donné. Le positionnement des couches métalliques d'écrantage, le dimensionnement des photodiodes et des nœuds de stockage ainsi que le positionnement des micro-lentilles peuvent jouer un rôle fondamental dans la réponse du capteur d'image à la lumière parasite. L'objectif de ce chapitre est donc d'exploiter le modèle développé pour analyser l'impact des paramètres de conception sur les performances du capteur d'image en termes d'efficacité d'obturation globale.

2.1 Optimisation des dimensions du nœud de stockage

Concentrons-nous maintenant sur la fonction du transport et analysons l'impact du dimensionnement du nœud de stockage sur les performances de l'efficacité d'obturation des imageurs CMOS à obturation globale. Il faut garder à l'esprit que nous utilisions une technologie 5T dans laquelle le rôle du nœud de stockage est effectué par la Floating Diffusion ; la distance entre la Floating Diffusion et la PhotoDiode est fixe et donnée par le procédé technologique et ne peut être modifiée. Nous ne considérerons donc que l'impact de la longueur et de la largeur du nœud de stockage sur les performances de l'efficacité d'obturation globale.

2.1.1 Le facteur de correction géométrique dans les simulations 2D

Fig. 2.1 donne une définition de la *largeur* et *longueur* des nœuds, où une ligne (notée *Y-cut*) qui passe à la fois par PhotoDiode et le nœud de stockage est tracée. Nous définissons la *largeur* comme la dimension perpendiculaire à la ligne et la *longueur* comme la dimension parallèle à la ligne. Concentrons-nous d'abord sur le facteur de correction de la géométrie.

Les simulations 2D sont prises le long de la ligne *Y-cut* et donc un facteur de correction géométrique est nécessaire afin de prendre en compte la 3ème dimension manquante, qui

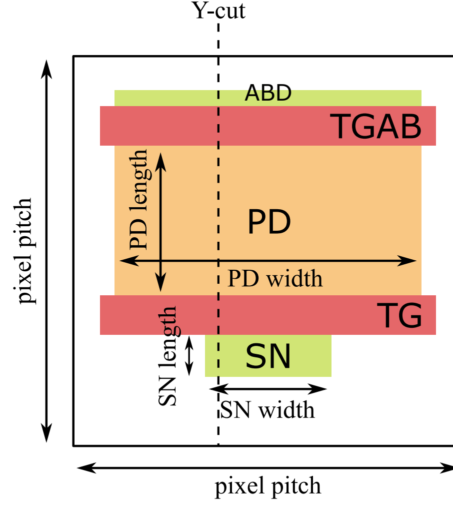

FIGURE 2.1 – Schéma en vue de dessus des pixels avec description des dimensions de la photodiode et du nœud de stockage. Pour une meilleure compréhension, les transistors RST, SF et SELY n'ont pas été montrés, alors que les transistors TG et TGAB ainsi que l'ABD sont présents.

a été déterminée comme la largeur du nœud. La sensibilité à la lumière du nœud dépend linéairement de la largeur du nœud et peut être formulée comme suit :

$$QE_{PD} = \frac{y_{PD}}{p} \cdot QE_{PD,2D} \tag{2.1}$$

$$QE_{SN} = \frac{y_{SN}}{p} \cdot QE_{SN,2D} \tag{2.2}$$

où y_{PD} et y_{SN} sont respectivement la largeur de la photo diode et du nœud de stockage, p est le pas des pixels et $QE_{PD,2D}$ et $QE_{SN,2D}$ sont les rendements quantiques de la photodiode et du nœud de stockage calculés à partir de simulations 2D. L'augmentation de la largeur de la photodiode (ou du nœud de stockage) augmenterait donc linéairement la sensibilité à la lumière de la photo diode (ou du nœud de stockage).

2.1.2 Impact de la longueur et de la largeur sur la sensibilité à la lumière parasite

Nous aimerions maintenant analyser l'impact de la longueur d'un nœud sur ses performances en matière de sensibilité à la lumière. Contrairement à ce qui a été présenté précédemment dans le cas de la largeur d'un nœud, cela ne peut pas être fait par un facteur multiplicatif, puisque la longueur du nœud est un paramètre important lors du calcul de la fonction du transport.

Une étude a été menée pour analyser l'impact de la longueur du nœud de stockage sur la sensibilité à la lumière du nœud de stockage ainsi que sur l'insensibilité à la lumière parasite

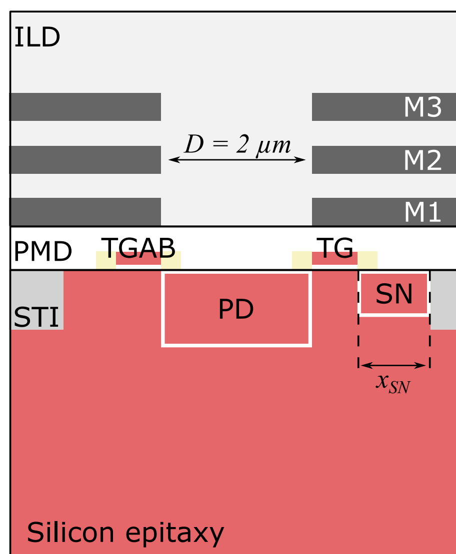

FIGURE 2.2 – Schéma du pixel simulé en FDTD pour étudier l'impact de la longueur du nœud de stockage sur la sensibilité à la lumière parasite. La dimension de l'ouverture D est constante, ainsi que d'autres dimensions dans la structure. La longueur du nœud de stockage est désignée par x_{SN}. Les dimensions du STI de droite varient en fonction de la longueur du nœud de stockage.

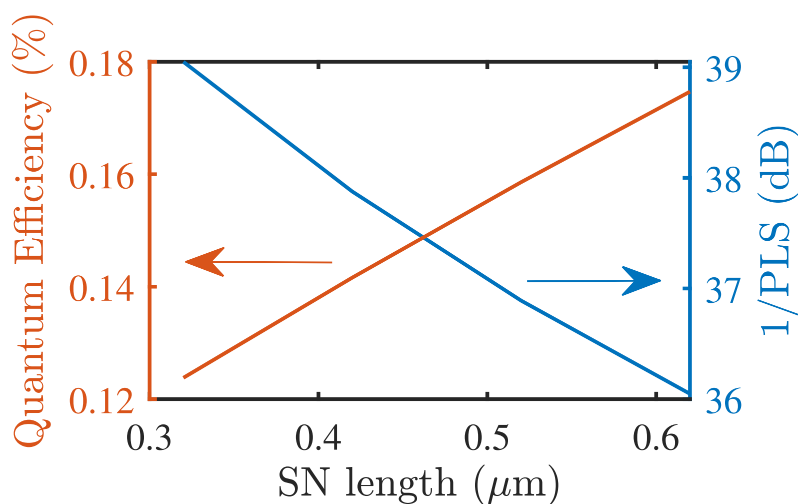

FIGURE 2.3 – Résultats de la simulation de l'efficacité quantique (courbe rouge) et de l'insensibilité à la lumière parasite (1/PLS) (courbe bleue) en fonction des dimensions du nœud de stockage pour $\lambda = 650\,\text{nm}$.

(1/PLS) du pixel simulé. Des simulations, exploitant le modèle en ligne droite, ont été réalisées

sur une simple structure de pixels 5T, comme le montre la Fig. 2.2 représentant la structure de pixels modélisée dans les simulations FDTD. La couche épitaxiale de silicium se trouve sur le fond de la structure ; des isolations par tranchées peu profondes (STI) sont creusées dans la couche épitaxiale de silicium, qui est exploitée pour séparer les couches actives des pixels. Tous les principaux éléments des pixels se trouvent à l'intérieur de la région active, c'est-à-dire la région où il n'y a pas de STI ; la photodiode se trouve au centre de la couche épitaxiale, le nœud de stockage se trouve à droite de la photodiode. Entre la photodiode et le nœud de stockage et juste au-dessus, la structure TG est représentée, consistant en un oxyde de grille SiO_2, une grille de transfert (TG) en poly-silicium et des espaceurs en nitrure. Le ABD se trouve à gauche de la photodiode et, juste au-dessus et entre les deux, le TGAB est représenté, également constitué d'un oxyde de grille SiO_2, d'une TG en polysilicium et d'espaceurs en nitrure. Les deux grilles sont immergées dans le diélectrique pré-métallique. Juste au-dessus de la couche diélectrique pré-métallique (PMD) se trouve la couche diélectrique inter-couches (ILD), dans laquelle les différentes couches métalliques sont immergées. Comme indiqué précédemment, M1 est le niveau le plus proche de l'interface Silicium/SiO_2, M3 est le niveau le plus éloigné de l'interface Silicium/SiO_2 et M2 se trouve entre les deux. La longueur du nœud de stockage est notée x_{SN}. Le STI du côté droit est en contact avec la région du nœud de stockage et donc ses dimensions sont réduites avec l'augmentation de la longueur du nœud de stockage.

La Fig. 2.3 montre l'évolution de la sensibilité à la lumière du nœud de stockage en fonction de la longueur du nœud. De la même manière, il est possible de calculer l'insensibilité à la lumière parasite (1/PLS) de la structure des pixels en fonction de la longueur du nœud de stockage, lorsque les dimensions de la diode photo sont maintenues constantes. Les résultats montrent clairement une détérioration de l'insensibilité à la lumière parasite (1/PLS), car la sensibilité à la lumière du nœud de stockage augmente avec l'augmentation de sa longueur.

2.2 Utilisation des couches métalliques BEOL pour l'écrantage à la lumière

Le modèle proposé permet d'analyser l'impact de la conception des éléments Back-End-Of-Line sur les performances des pixels. Comme décrit précédemment, les éléments Back-End-Of-Line n'interviennent que dans la modélisation de la réponse optique en régime permanent de la structure des pixels. Cela signifie que, lorsqu'une analyse paramétrique sur les éléments Back-End-Of-Line doit être effectuée sans modification de la conception du Front-End-Of-Line, il ne sera pas nécessaire de recalculer la fonction de transport en régime permanent, puisqu'elle sera valable pour l'ensemble de l'analyse paramétrique. En d'autres termes, les critères présentés dans le chapitre 1 permettent d'exploiter une fonction de transport en régime permanent en combinaison avec différentes réponses optiques en régime permanent puisque les deux phénomènes sont considérés comme indépendants.

L'objectif de l'utilisation du Back-End-Of-Line pour améliorer les performances de l'efficacité d'obturation globale repose principalement sur la compréhension de la protection contre la lumière avec l'utilisation de couches d'interconnexion métalliques, grâce à la mo-

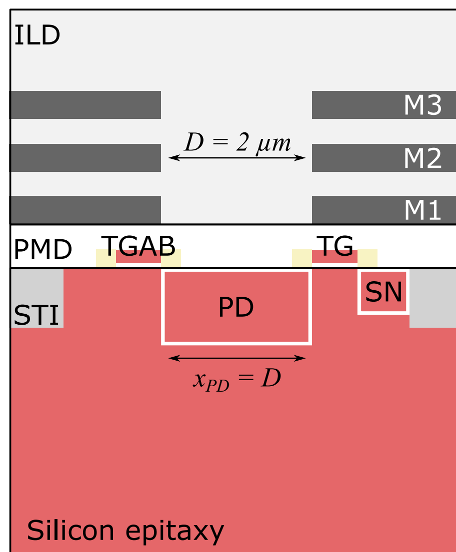

FIGURE 2.4 – Schéma du pixel FDTD simulé. La dimension de l'ouverture D est constante et correspond à x_{PD}, soit la longueur de la PhotoDiode. Les "M1", "M2" et "M3" sont représentés dans le schéma, bien qu'ils puissent ne pas être présents pour chaque simulation. Si elles ne sont pas présentes, la couche métallique est remplacée par le diélectrique inter-couches (ILD).

délisation complète de la propagation de la lumière à l'intérieur de la structure du pixel en exploitant la simulation FDTD. Un procédé technologique commercial d'imageurs CMOS a été sélectionné, comportant quatre niveaux d'interconnexion métallique. Seuls trois niveaux métalliques seront exploités, désignés par *M1, M2, M3.* Chaque niveau de métal a une distance définie de l'interface Silicium/SiO_2 ainsi qu'une épaisseur définie. Le niveau de métal inférieur, M1, représente le niveau le plus proche de l'interface Silicium/SiO_2 ; plus le niveau de métal augmente, plus la distance par rapport à l'interface Silicium/SiO_2 augmente.

2.2.1 Choix des couches métalliques à des fins d'écrantage

Avant d'entrer dans une analyse détaillée de l'impact des différentes couches métalliques d'écrantage sur la sensibilité à la lumière du nœud de stockage ainsi que sur les performances de l'efficacité d'obturation globale, examinons de plus près la structure qui a été exploitée pour nos simulations, comme le montre la Fig. 2.4. Les couches métalliques recouvrent entièrement le pixel, tout en laissant une seule fente en correspondance avec la PhotoDiode ; la dimension de l'ouverture est égale à la longueur de la PhotoDiode. Contrairement à ce qui est indiqué sur la figure, les trois couches métalliques ne sont pas toujours présentes dans nos simulations, le but étant d'étudier l'impact des différentes couches métalliques de protection sur les performances de l'efficacité d'obturation globale du capteur d'image. À titre d'exemple, si une simulation contient la combinaison de couches métalliques "M1+M3", cela signifie que la couche M1 ainsi que la couche M3 seront présentes dans la simulation, tandis que M2 disparaîtra et sa place sera occupée par le diélectrique inter-couches (ILD).

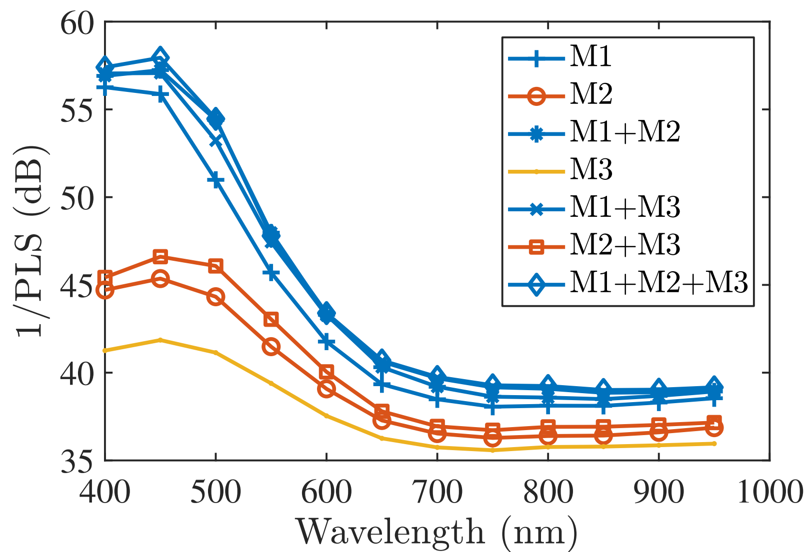

FIGURE 2.5 – Simulation de l'évolution de l'insensibilité à la lumière parasite (1/PLS) en fonction de la longueur d'onde et des couches métalliques d'écrantage. Le groupe bleu a "M1" comme couche métallique d'écrantage la plus basse, le groupe rouge a "M2" comme couche métallique d'écrantage la plus basse et le groupe jaune a "M3" comme couche métallique d'écrantage la plus basse.

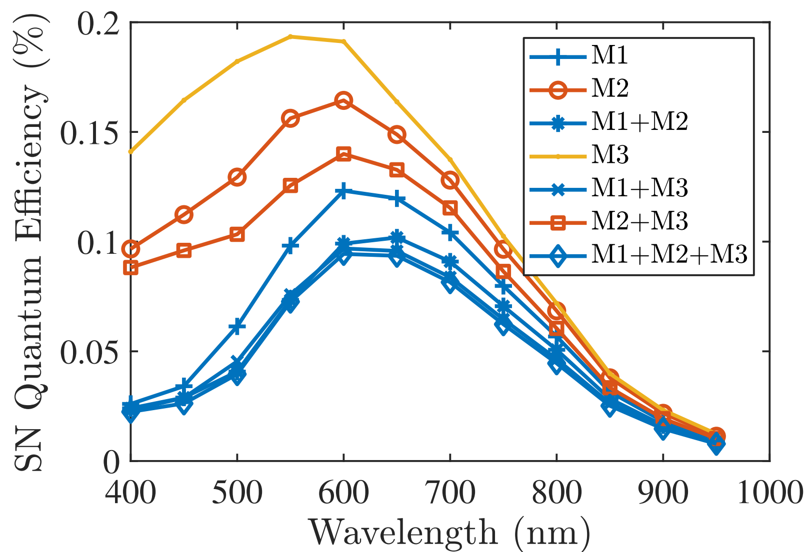

FIGURE 2.6 – Simulation de l'évolution de l'efficacité quantique du nœud de stockage en fonction de la longueur d'onde et des couches métalliques d'écrantage. Le groupe bleu a "M1" comme couche métallique d'écrantage la plus basse, le groupe rouge a "M2" comme couche métallique d'écrantage la plus basse et le groupe jaune a "M3" comme couche métallique d'écrantage la plus basse.

Fig. 2.5 décrit la réponse du pixel à l'insensibilité à la lumière parasite (1/PLS) en fonction de la couche métallique d'écrantage et de la longueur d'onde. Dans une première analyse, on peut apprécier comment l'insensibilité à la lumière parasite (1/PLS) diminue en fonction de la longueur d'onde, pour $\lambda \leq 700\,\text{nm}$ pour chaque combinaison d'écrantage choisie ; en exploitant l'analyse du nombre de Fresnel (N_F), lorsqu'on se déplace vers des longueurs d'onde plus grandes N_F augmente, ce qui conduit à des distributions de champ électrique qui s'étendent de plus en plus vers la région occultée, la région du nœud de stockage étant atteinte par un nombre croissant de photons. Pour $\lambda > 700\,\text{nm}$ l'insensibilité à la lumière parasite (1/PLS) augmente légèrement ; le nombre de Fresnel continue d'augmenter, bien que la photo-génération de charges se produise principalement plus profondément dans le substrat de silicium que près de la surface. Le nombre de charges photo-générées dans la région du nœud de stockage commence à diminuer, les charges générées en profondeur sont de plus en plus protégées par la barrière de potentiel PWELL, limitant ainsi la sensibilité à la lumière du nœud de stockage, comme indiqué précédemment, et étant la principale raison de la légère augmentation de l'insensibilité à la lumière parasite (1/PLS). Trois couleurs ont été choisies pour représenter certaines catégories d'écrantage et peuvent être décrites comme suit :

- **Blue :** La couleur bleue représente la famille de courbes résultant de simulations de la structure des pixels où la couche métallique d'écrantage la plus basse est "M1". Par exemple, la combinaison "M1+M3" exploite deux couches métalliques à des fins d'écrantage et la couche métallique la plus basse exploitée est "M1".
- **Rouge :** La couleur rouge représente la famille de courbes résultant de la simulation de la structure des pixels où la couche d'écrantage métallique la plus basse est "M2".
- **Jaune :** La couleur jaune représente la famille de courbes résultant de la simulation de la structure des pixels où la couche métallique d'écrantage la plus basse est "M3".

Cette catégorisation permet de distinguer un résultat important de nos simulations : la réponse de l'insensibilité à la lumière parasite (1/PLS) des pixels exploitant la même couche inférieure d'écrantage est similaire et des groupes peuvent être formés. En particulier, les structures de pixels comprenant la couche métallique d'écrantage la plus basse, c'est-à-dire "M1", ont de meilleures performances en matière d'insensibilité à la lumière parasite (1/PLS) par rapport aux autres structures de pixels. De la même manière, les structures de pixels incluant "M2" comme couche métallique d'écrantage inférieure obtiennent de meilleures performances par rapport à la structure simple "M3".

2.2.2 Optimisation du positionnement des couches métalliques

Il a été démontré l'importance de la diffraction de la lumière pour la comptabilisation des performances de l'efficacité d'obturation globale dans les imageurs CMOS à obturation globale et comment l'utilisation du niveau correct de blindage métallique peut aider à réduire la lumière diffractée à se propager vers la région occultée. Cependant, jusqu'à présent, toutes les interprétations ont été tirées en considérant la même ouverture de protection contre la lumière juste au-dessus de la photodiode, ce qui signifie que la distance entre le début de la région du nœud de stockage et la fin de l'ouverture dans l'écran métallique a été maintenue constante. Nous avons vu que la tendance de la lumière à se propager par diffraction dépend

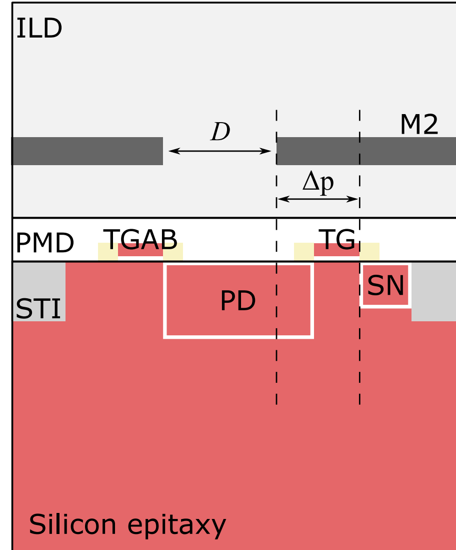

FIGURE 2.7 – Schéma du pixel simulé en FDTD. La dimension de l'ouverture D change en fonction du *recouvrement*, qui est définie comme la distance entre la fin de la couche d'écrantage métallique et le début de la région du nœud de stockage. La dimension de la photodiode est fixe et égale à 2 µm.

de la longueur d'onde et de la distance de l'interface Silicium/SiO_2 et ces paramètres ne sont pas toujours maîtrisables.

La Fig. 2.7 décrit la structure simulée. Elle est similaire à celle exploitée pour étudier l'impact de différentes couches métallique d'écrantage, la différence se situant dans la distance entre le début de la région du nœud de stockage et la fin de la couche métallique d'écrantage, désignée par le paramètre Δp. Lorsque $\Delta p = 0.7\,\mu\text{m}$, la distance entre la gauche et la droite de l'ouverture, donc la dimension de l'ouverture, est égale à la longueur de la photodiode ($D = x_{PD}$), ce qui correspond à la structure présentée pour l'étude sur la combinaison des couches métalliques d'écrantage. Il apparaît clairement que si Δp augmente, la dimension de l'ouverture D diminue en conséquence.

Fig. 2.8 montre les résultats de simulation de l'insensibilité à la lumière parasite (1/PLS) de l'étude présentée pour trois couches métalliques d'écrantage différentes à une longueur d'onde d'impact déterminée $\lambda = 650\,\text{nm}$. On peut noter une réduction de l'insensibilité à la lumière parasite (1/PLS) par rapport au niveau de métal d'écrantage exploité, à partir de $\Delta p \geq 0.5\,\mu\text{m}$. À une longueur d'ouverture donnée, le nombre de Fresnel est plus faible à grande distance [Hec15] ; un nombre de Fresnel plus faible entraîne une diffraction Fraunhofer, donc un effet de diffraction plus prononcé. L'efficacité quantique de la photodiode est plus faible pour un niveau métallique d'écrantage plus élevé en raison de la propagation du champ électrique au-delà de la région de la photodiode, comme le montre Fig. 2.9. Néanmoins, l'efficacité quantique du nœud de stockage diminue également en raison de la plus faible puissance lumineuse atteignant la région du nœud de stockage. Ensuite, une diminution de l'insensibilité à la lumière parasite (1/PLS) pour M2 et M3 pour $\Delta p \geq 1.4\,\mu\text{m}$ est indiquée

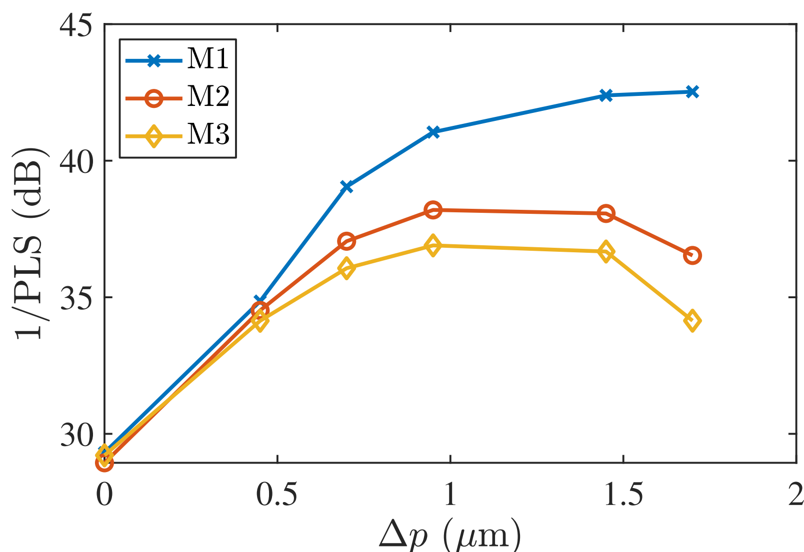

FIGURE 2.8 – Résultats de la simulation de l'insensibilité à la lumière parasite (1/PLS) à $\lambda = 650\,\text{nm}$ en fonction des couches métalliques d'écrantage et Δp, étant la distance entre une extrémité de la couche métallique d'écrantage et le début de la région du nœud de stockage.

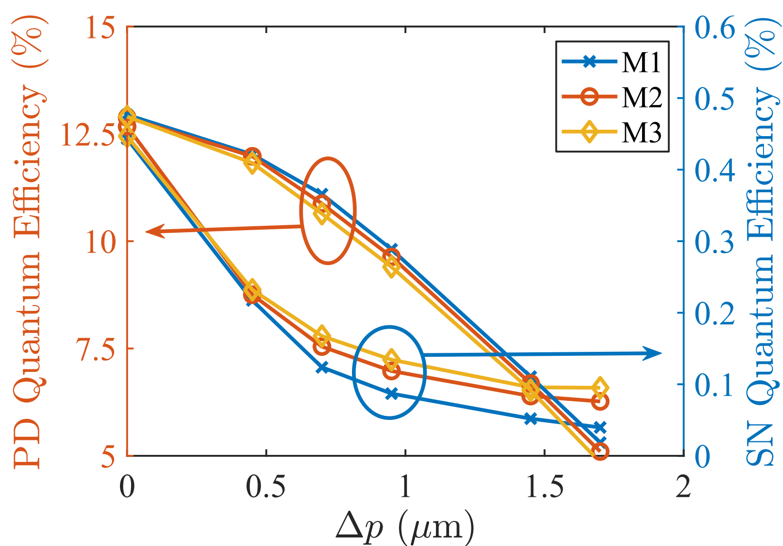

FIGURE 2.9 – Résultats de la simulation de l'efficacité quantique pour la photodiode (à gauche) et le nœud de stockage (à droite) à $\lambda = 650\,\text{nm}$ en fonction des couches métalliques d'écrantage et Δp, étant la distance entre une extrémité de la couche métallique d'écrantage et le début de la région du nœud de stockage.

dans la Fig. 2.8. Cela est dû à une réduction de l'efficacité quantique des photodiodes, alors que l'efficacité quantique des nœuds de stockage reste relativement constante et semble avoir atteint un minimum.

2.3 Conclusions

Il a été démontré que les dimensions du nœud de stockage peuvent avoir une forte incidence sur les performances des imageurs à obturation globale. Néanmoins, certaines contraintes peuvent être imposées au gain ou à la capacité de conversion ; d'autres outils doivent être exploités pour améliorer encore les performances des imageurs à obturation globale.

Le rôle de l'écrantage de la lumière par l'utilisation de couches d'interconnexion métalliques a été étudié. Les avantages de l'utilisation de la couche métallique la plus basse disponible ont été démontrés, en accord avec la théorie de la diffraction et sa modélisation utilisant le nombre de Fresnel [Hec15].

En outre, l'amélioration de l'écrantage de la lumière du nœud de stockage a été étudiée au moyen de la distance entre l'extrémité du niveau métallique d'écrantage et le début de la région du nœud de stockage. Les résultats ont montré que la sensibilité à la lumière du nœud de stockage est effectivement réduite lorsque la distance donnée est augmentée ; il est néanmoins important de prendre en compte le changement de sensibilité à la lumière de la photodiode, qui pourrait être considérablement réduite lors de l'utilisation d'une telle solution.

Chapitre 3

Caractérisation et modélisation des imageurs CMOS à obturation globale

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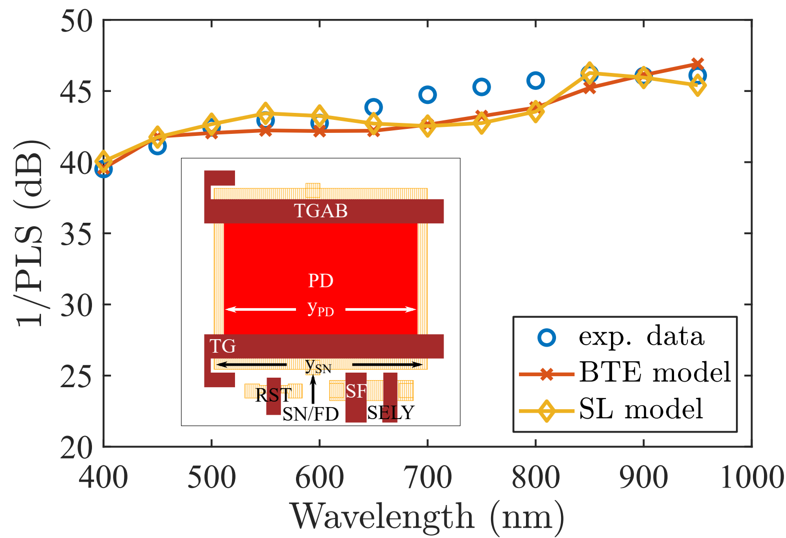
Ce chapitre vise à fournir une référence expérimentale pour prouver les constatations données dans les chapitres précédents, fournissant ainsi la validité du modèle développé. Tout d'abord, une métrique permettant de caractériser la sensibilité à la lumière parasite des capteurs d'images CMOS à obturateur global est développée ; successivement, différents pixels CMOS à obturation globale sont mesurés et comparés afin de valider les hypothèses formulées dans les chapitres précédents. Enfin, le modèle développé est comparé aux données expérimentales.

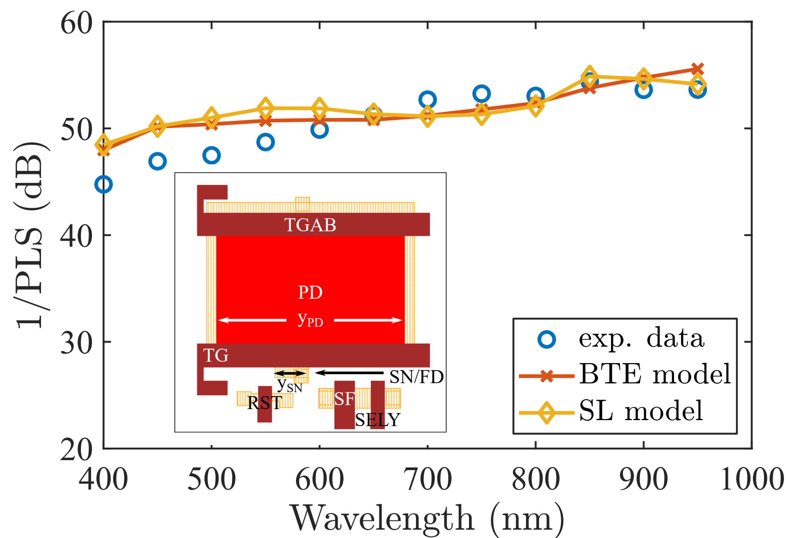
3.0.1 Modélisation de la sensibilité à la lumière parasite d'un imageur CMOS réel

Le facteur de correction géométrique présenté dans l'expression de l'efficacité quantique simulée a été légèrement modifié pour approcher le résultat expérimental, car il a été constaté que l'efficacité quantique n'augmente pas au même rythme que la largeur du nœud de stockage, ce qui serait normal si la largeur du nœud de stockage était une constante multiplicative, comme l'indique Eq. (2.2). Le coefficient y_{SN} a donc été remplacé par une valeur mesurée par la régression linéaire d'une mesure de l'efficacité quantique du nœud de stockage en fonction de la largeur du nœud de stockage. Une hypothèse similaire a été faite avec la PhotoDiode, bien qu'aucune structure avec une largeur de PhotoDiode différente ne soit disponible, de sorte qu'aucune mesure n'a pu être effectuée. y_{PD} a donc été ajusté afin de correspondre aux données expérimentales et il n'est pas ajusté par des mesures sur différentes largeurs de PhotoDiode.

Fig. 3.1 présentent la modélisation de l'insensibilité à la lumière parasite (1/PLS) en fonction de la longueur d'onde des deux pixels REF et VAR. Étant donné que les deux structures ont une PhotoDiode identique, le même coefficient a été utilisé pour calculer l'efficacité quantique de la PhotoDiode. Les simulations reproduisent un comportement similaire à celui de la structure expérimentale dans les deux cas, bien que sous-estimant autour de 700 nm pour la structure REF et surestimant à des longueurs d'onde plus courtes pour la structure VAR. Les fluctuations et les erreurs dans la modélisation de l'insensibilité à de la lumière



(a) REF



(b) VAR

FIGURE 3.1 – Modélisation de l'insensibilité à la lumière parasite (1/PLS) d'un imageur CMOS à obturation globale réel avec l'utilisation des deux modèles développés en fonction de la longueur d'onde. Les cercles bleus représentent les données expérimentales ; les courbes en croix rouge représentent le modèle de l'équation du transport de Boltzmann ; les courbes en losange jaune représentent le modèle de la ligne droite. (a) montre la modélisation de l'insensibilité à la lumière parasite (1/PLS) pour la structure REF, dont la conception est indiquée dans le coin inférieur gauche ; (b) montre la modélisation de l'insensibilité à la lumière parasite (1/PLS) pour la structure VAR, dont la conception est indiquée dans le coin inférieur gauche.

parasite (1/PLS) peuvent avoir pour origine l'efficacité quantique des nœuds de stockage, qui est le dénominateur de la fraction ; une petite variation de cette dernière peut provoquer une variation importante de l'insensibilité à la lumière parasite modélisée (1/PLS). En outre, l'approche simpliste exploitée soit pour construire la carte du champ électrique, pour le modèle de l'équation de transport de Boltzmann, soit pour le modèle de la ligne droite (voir sec. 1.2) peut entraîner des imperfections sur l'estimation de la fonction de pondération de la probabilité de collection et se traduire par des erreurs d'estimation de l'insensibilité à la lumière parasite (1/PLS). Néanmoins, le comportement de l'insensibilité à la lumière parasite (1/PLS) en fonction de la longueur d'onde semble être reproduit dans les deux cas.

3.1 Développement de méthodes pour atténuer la sensibilité à la lumière parasite en post-traitement

Cette section vise à développer un modèle de la sortie du capteur d'image lorsqu'il fonctionne en mode d'obturation globale, permettant ainsi l'analyse et le développement de diverses méthodes de post-traitement pour atténuer la sensibilité à la lumière parasite.

Une méthode de correction post-traitement vise à traiter une image acquise par l'utilisation d'un algorithme, souvent pour améliorer la qualité de l'image acquise, mais pas seulement. Dans notre cas, nous visons à développer et à analyser des méthodes de correction post-traitement pour atténuer l'apparition d'un signal supplémentaire causé par la sensibilité non négligeable à la lumière parasite qui caractérise les imageurs CMOS à obturation globale.

3.1.1 Développement d'une méthode de modélisation de la tension de sortie des imageurs CMOS à obturation globale

Une définition de la sortie du capteur d'image est tout d'abord nécessaire ; la Fig. 3.2 montre un exemple de pixel à obturation globale générique et la lecture de sa colonne. En première approximation, il est possible de modéliser $\mathrm{V_{out}}$ pour le pixel (i, j), avec i et j étant respectivement le numéro de ligne et de colonne, en fonction du nombre d'électrons collectés par la PhotoDiode, $N_{el_{PD}}$, et transféré au nœud de stockage et le nombre d'électrons collectés par le nœud de stockage, $N_{el_{SN}}$, tel que donné par

$$V_{out}(i,j) = A(i,j) \cdot [N_{el_{PD}}(i,j) + N_{el_{SN}}(i,j)] = V_{PD}(i,j) + V_{PLS}(i,j), \tag{3.1}$$

où $A(i, j)$ est un paramètre contenant le gain du buffer (généralement le gain du Source Follower) et le gain de conversion. Nous supposons que les charges collectées par la PhotoDiode seule produisent une tension donnée par V_{PD} et que les électrons collectés par le nœud de stockage seul produisent une tension donnée par V_{PLS}.

Supposons tout d'abord qu'une trame doit être acquise, avec un temps d'intégration de t_{int} ; l'opération de lecture séquentielle nécessite la lecture séparée d'une ligne dans un temps

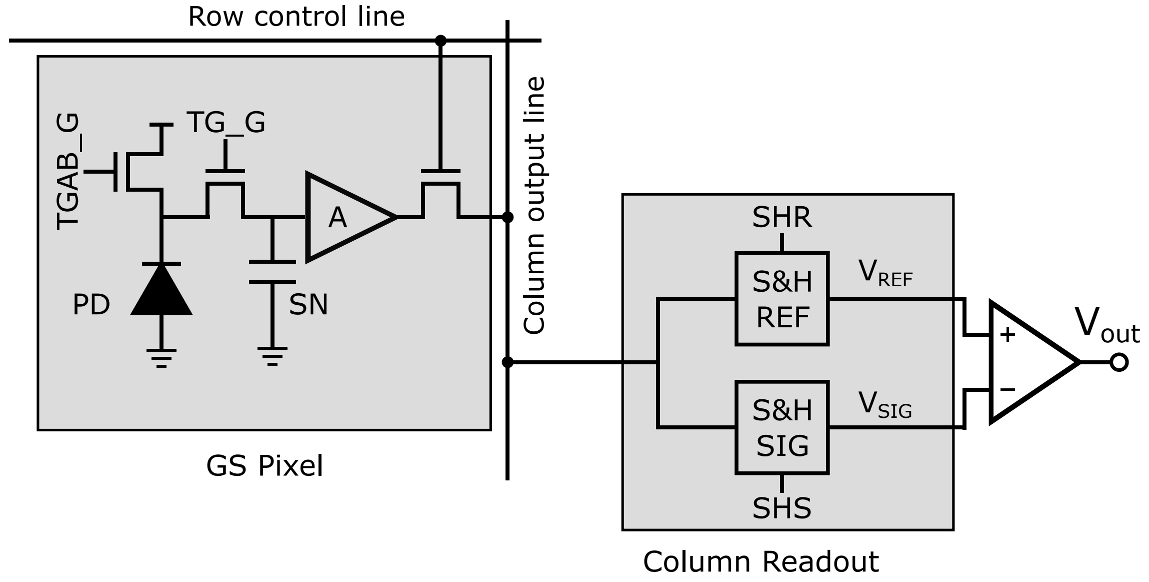


FIGURE 3.2 – Schéma d'un imageur CMOS à obturation globale générique. Le pixel est constitué d'une PhotoDiode, représentée par une diode à polarisation inverse, d'un amplificateur de gain A dans le pixel, d'un transistor de sélection de ligne, d'un nœud de stockage et de deux transistors déterminant le début (TGAB_G) et l'arrêt (TG_G) de l'intégration. La sortie du pixel passe par la ligne de sortie de la colonne pour atteindre la lecture de la colonne, où les tensions de référence (V_{REF}) et de signal (V_{SIG}) sont échantillonnées et stockées temporairement dans leurs Sample&Hold (S&H) respectifs en exploitant les lignes de commande SHR et SHS. Le signal de sortie V_{out} est le résultat de la différence entre V_{REF} et V_{SIG}.

donné t_{rro}. En considérant un éclairage du capteur d'image non variable dans le temps, il est possible de définir V_{PD} et V_{PLS} comme donné par Eqs. (3.2) et (3.3), où $\Gamma(i,j)$ représente le taux de photons incident pour chaque pixel.

$$V_{PD}(i,j) = A(i,j) \cdot QE_{PD}(i,j) \cdot \Gamma(i,j) \cdot t_{int} \tag{3.2}$$

$$\begin{aligned} V_{PLS}(i,j) = A(i,j) \cdot QE_{SN}(i,j) \cdot \Gamma(i,j) \cdot (i-1) \cdot t_{rro} + \\ + A(i,j) \cdot DC_{SN} \cdot (i-1) \cdot t_{rro} \end{aligned} \tag{3.3}$$

Le courant d'obscurité a été pris en compte uniquement pour le nœud de stockage (DC_{SN}), étant donné que les temps d'intégration des imageurs à obturation globale sont souvent très courts et que la contribution du courant d'obscurité d'une PhotoDiode pincée est négligeable. Il faut noter que $V_{PLS}(1,j) = 0$; une opération de réinitialisation est effectuée juste avant la fin de la phase d'intégration, supprimant ainsi tous les électrons acquis par le nœud de stockage pendant la période d'intégration ; les électrons contribuant à V_{PLS} ne sont donc collectés que pendant la phase de lecture. La lecture de la deuxième ligne est effectuée après la lecture de la première ligne ; le temps de stockage est donc équivalent au temps de lecture de la ligne précédente. Ce schéma se poursuit pour l'ensemble de la matrice, expliquant ainsi le facteur $(i-1)$ devant t_{rro}.

La définition de V_{PLS} en fonction de V_{PD} est possible grâce à ce qui suit

$$V_{PLS}(i,j) = V_{PD}(i,j) \cdot PLS(i,j) \cdot \frac{(i-1) \cdot t_{rro}}{t_{int}} + \\ + A(i,j) \cdot DC_{SN}(i,j) \cdot (i-1) \cdot t_{rro}. \tag{3.4}$$

Le signal de sortie peut être décrit comme suit :

$$V_{out}(i,j) = V_{PD}(i,j) \cdot \left[1 + PLS(i,j) \cdot \frac{(i-1) \cdot t_{rro}}{t_{int}}\right] + \\ + A(i,j) \cdot DC_{SN}(i,j) \cdot (i-1) \cdot t_{rro}, \tag{3.5}$$

où $(i-1) \cdot t_{rro}$ représente le temps de stockage de la ligne *i-ème*.

Afin d'assurer la validité de (3.5), des mesures ont été effectuées sur un imageur CMOS à obturation globale avec des pixels 5T à une longueur d'onde fixe de $\lambda = 650\,\text{nm}$. Notamment, pour apprécier les variations de la sortie ligne par ligne, un capteur d'image à faible sensibilité à la lumière parasite ainsi qu'un long temps de stockage par ligne sont nécessaires. Le temps de stockage de la ligne a été choisi pour être de 50 ms, en raison de contraintes d'équipement. Il est possible d'exploiter TGAB pour augmenter le temps pendant lequel toute la matrice est sous la lumière (c'est-à-dire le temps pendant lequel le nœud de stockage se trouve en mode de stockage) tout en bloquant la collection de photodiodes en évitant les phénomènes d'éblouissement conduisant à des débordements.

Le capteur d'images a été exposé à un éclairage en champ plat invariant dans le temps, $\Gamma(i,j) = \Gamma$, on suppose donc que V_{PD} est invariant dans le temps et l'espace. De plus, la sensibilité à la lumière parasite a été considérée comme uniforme dans tout la matrice.

Il est possible de dériver Eq. 3.5 par rapport au numéro de ligne et on obtient l'Eq. 3.6, ce qui montre une augmentation linéaire du signal de sortie en fonction du numéro de ligne à un taux de photons incidents constant.

$$\frac{\partial V_{out}(i,j)}{\partial i} = V_{PD} \cdot PLS \cdot \frac{t_{rro}}{t_{int}} + A \cdot DC_{SN}(i,j) \cdot t_{rro} \tag{3.6}$$

Par conséquent, sachant que la mesure peut être effectuée à différentes intensités lumineuses, c'est-à-dire en fonction du taux de photons incidents, il est possible de dériver Eq. (3.6) par rapport au taux de photons Γ, comme le montre Eq. (3.7), ce qui montre là encore un comportement linéaire.

$$\frac{\partial}{\partial \Gamma}\left(\frac{\partial V_{out}(i,j)}{\partial i}\right) = A \cdot QE_{PD} \cdot PLS \cdot t_{rro} \tag{3.7}$$

Il a été prouvé expérimentalement le comportement linéaire de ces deux équations, ce qui prouve la validité de la méthode développée.

En première approximation, on suppose que l'intensité lumineuse est invariante dans le temps. La sortie du pixel $(i - \grave{e}me, j - \grave{e}me)$ sera donnée, en exploitant l'Eq. (3.5), par ce qui

suit :

$$\mathrm{V_{out}}(i,j) = V_{PD}(i,j) \cdot \left[1 + PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}}\right] \tag{3.8}$$

où

$$t_{strg}(i) = (i-1) \cdot t_{rro} \tag{3.9}$$

définit la durée de stockage de ligne. On note que la contribution en courant d'obscurité a été volontairement oubliée car elle peut être considérée comme une compensation dépendant du temps de stockage ; cette hypothèse permet de simplifier les équations à traiter. À partir de l'Eq. (3.8), il est possible de calculer V_{PD} (étant la tension n'incluant pas le signal induit par la sensibilité à la lumière parasite) par la simple connaissance de PLS(i, j) mesuré par pixel, du temps d'intégration t_{int} et du temps de lecture de ligne t_{rro} comme donné par ce qui suit :

$$V_{PD}(i,j) = \mathrm{V_{out}}(i,j) \cdot \left[1 + PLS(i,j) \cdot \frac{t_{strg}(i)}{t_{int}}\right]^{-1} \tag{3.10}$$

Une fois que la modélisation de l'équation $\mathrm{V_{out}}$ dans les imageurs CMOS à obturation globale aura été entièrement développée, son exploitation pourrait permettre de mettre au point des méthodes de correction en post-traitement dans le domaine temporel pour atténuer la sensibilité à la lumière parasite.

3.1.1.1 Tester la correction avec une approche invariante dans le temps

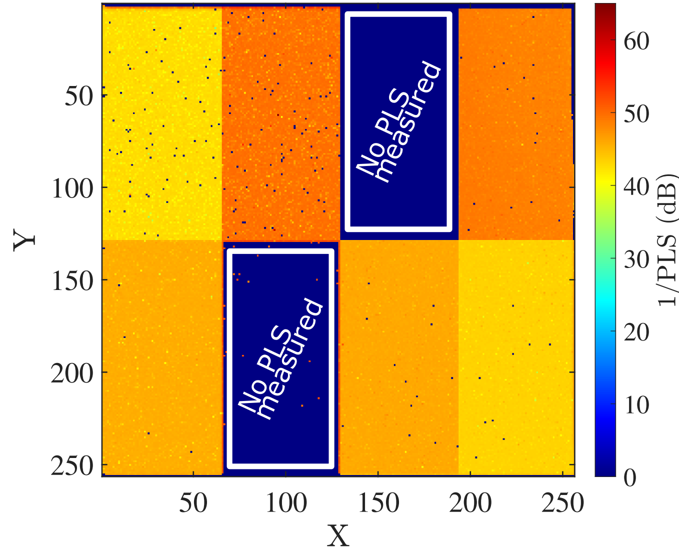


FIGURE 3.3 – Cartographie 2D de l'insensibilité à la lumière parasite (1/PLS) du capteur testé avec 8 zones différentes. Sur les deux zones mises en évidence, la mesure de la sensibilité à la lumière parasite n'a pas été possible.

Afin de prouver l'efficacité de la correction pour atténuer la sensibilité à la lumière parasite,

nous avons décidé de tester notre méthode pour corriger une trame souffrant de sensibilité à la lumière parasite dans des conditions invariantes dans le temps, ce qui signifie que l'intensité de la lumière incidente est constante pendant l'intégration de la trame et la lecture. À cette fin, nous allons donc exploiter l'Eq. (3.8).

Afin d'augmenter la visibilité des phénomènes de sensibilité à la lumière parasite, la lecture des rangées a été augmentée à 50 ms. Le temps d'intégration des images est fixé à 50 ms, tandis que le temps total de lecture est de 12.8 s en considérant un capteur d'images de 256 lignes. L'image a été prise à partir d'un imageur CMOS à obturation globale présentant 8 zones avec des caractéristiques différentes, montrant ainsi une sensibilité différente à la lumière parasite. Cette dernière a été mesurée pixel par pixel sur l'ensemble de la matrice (à l'exception de deux zones sur lesquelles la mesure n'a pas été possible) et le résultat est présenté sur la Fig. 3.3. Les pixels bleu foncé (PLS = 0 dB) représentent les pixels sur lesquels la mesure de la sensibilité à la lumière parasite n'a pas pu être effectuée (souvent des pixels "chauds" en raison d'un courant d'obscurité élevé au niveau du nœud de stockage). La mesure de la sensibilité à la lumière parasite et la capture d'images sont toutes deux effectuées à $\lambda = 650$ nm.

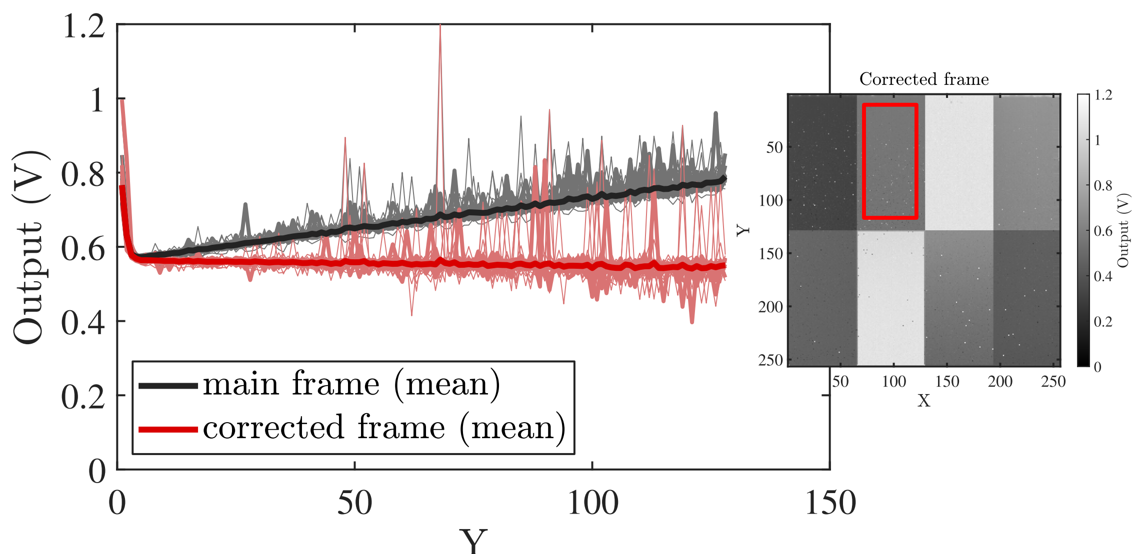


FIGURE 3.4 – Sortie de chaque pixel en fonction du numéro de ligne pour la trame principale (en noir) et la trame corrigée (en rouge). Les lignes pleines représentent la moyenne par ligne de sortie. L'encadré montre la zone à partir de laquelle les pixels sont pris en compte. Le courant d'obscurité du nœud de stockage n'a pas été supprimé.

Pour mieux apprécier l'efficacité de la correction, la Fig. 3.4 montre la sortie des pixels en fonction du numéro de ligne pour la trame principale (en noir) et la trame corrigée (en rouge) pour la zone marquée. Les lignes en gras représentent la moyenne de sortie des pixels sur la même ligne. En dehors des effets de bord (sur les premières lignes), l'efficacité de la correction peut être appréciée au moyen de l'aplatissement de la réponse du capteur par rapport à l'image non corrigée ayant un gradient important en fonction du numéro de ligne en raison de la sensibilité à la lumière parasite. Une légère sur-correction est néanmoins appréciable,

car la courbe rouge semble diminuer en fonction du numéro de ligne. La raison de cette "sur-correction" est encore à l'étude.

Ces derniers résultats montrent l'importance des méthodes de correction en post-traitement dans le domaine temporel et la faisabilité de l'exploitation de la méthode indiquée pour leur traitement.

3.2 Conclusions

Les résultats expérimentaux de deux structures de pixels ont été comparés aux résultats de simulation. Certains paramètres de corrections ont été appliquées au modèle afin d'ajuster correctement les résultats expérimentaux. La tendance de l'insensibilité à la lumière parasite (1/PLS) en fonction de la longueur d'onde est assez bien reproduite pour les deux structures de pixels, bien que certaines inexactitudes soient présentes.

La deuxième partie de ce chapitre traite des mesures exploitées pour développer un modèle analytique de la sortie du capteur d'images CMOS lorsqu'il fonctionne en mode d'obturation globale, prenant ainsi en compte le signal ajouté induit par la sensibilité non négligeable à la lumière parasite. Une fois développé et validé par des mesures expérimentales ad hoc, le modèle analytique a été exploité pour analyser et développer certaines méthodes de post-traitement afin d'atténuer l'effet de la sensibilité à la lumière parasite des capteurs d'images CMOS en mode Global Shutter.

Conclusions et perspectives

Cette thèse présente une étude sur la sensibilité à la lumière parasite des imageurs CMOS à obturation globale. Le travail s'est notamment concentré sur la compréhension des phénomènes conduisant à une sensibilité non négligeable à la lumière parasite, grâce à l'utilisation de simulations et de mesures.

La sensibilité non négligeable à la lumière parasite reste un problème important qui limite l'exploitation des imageurs CMOS à obturation globale, en particulier dans les applications sous forte illumination. La sensibilité à la lumière parasite est causée par la collection de charges parasites par le nœud de stockage dans le pixel, pendant la phase de stockage et de lecture de la trame. Dans ce cadre, les travaux de recherche ont été axés sur le développement d'une méthode de modélisation de la sensibilité à la lumière parasite dans les imageurs CMOS à obturation globale, visant à comprendre les principaux phénomènes liés à la sensibilité à la lumière non négligeable des nœuds de stockage en charge et à perfectionner la conception des pixels grâce à des améliorations de l'écrantage des nœuds de stockage dans le spectre visible et dans le proche infrarouge.

Une méthode de modélisation de la sensibilité à la lumière parasite a été présentée dans le deuxième chapitre de cet ouvrage. La méthode est basée sur la résolution de la propagation optique de la lumière dans la structure du pixel et la propagation des charges photo-générées vers la PhotoDiode et le nœud de stockage grâce à l'utilisation de simulations. Les problèmes d'optique et de transport de charge sont résolus en régime permanent, ce qui permet un déroulement parallèle des simulations et donc une génération indépendante de leurs solutions. Le choix de la simulation optique a été motivé par la nécessité de prendre en compte le phénomène de diffraction de la lumière ; les simulations FDTD avec le logiciel Lumerical ont donc été choisies, permettant une résolution précise et efficace des équations de Maxwell. Le résultat de la simulation est représenté par le taux de génération de charge en régime permanent dans la couche épitaxiale de silicium à une longueur d'onde et à une structure de pixel données.

La résolution du problème du transport de charges a été développée dans le but de construire une fonction de pondération, aussi appelée probabilité de collection, déterminant la probabilité que la photodiode ou le nœud de stockage collectent les charges générées en un point donné de l'espace. Deux descriptions du mouvement des charges dans le silicium ont été exploitées à cette fin : une équation de transport de Boltzmann à une seule particule et un mouvement en ligne droite simplifié tenant compte de la probabilité de franchir une barrière de champ électrique. Afin de reproduire le comportement d'une structure 3D avec des simulations 2D, il a été démontré qu'un facteur de correction de la géométrie est nécessaire. Les sensibilités des nœuds sont donc corrigées avec les informations manquantes de la troisième dimension. On a constaté grâce à des données expérimentales que, bien qu'elles augmentaient linéairement avec la largeur des nœuds, le facteur de correction doit être réduit pour obtenir une bonne correspondance. Les sensibilités de la PhotoDiode et du nœud de

stockage sont donc exploitées pour calculer la sensibilité à la lumière parasite de la structure de pixel donnée.

Grâce à l'utilisation du modèle développé, il a été montré comment la lumière frappant la région du nœud de stockage conduit à la photo-génération de charges qui contribuent directement à la sensibilité à la lumière parasite du capteur. Dans les imageurs CMOS à éclairage frontal (FSI), la collection directe de la lumière a un impact important aux longueurs d'onde plus courtes, où une plus grande densité de charges est générée dans une région peu profonde proche de l'interface Silicium/SiO_2 et donc à l'intérieur du volume du nœud de stockage. Le simple blindage de la zone du nœud de stockage en exploitant les couches métalliques d'interconnexion n'est peut-être pas aussi trivial qu'il n'y paraît. Compte tenu de la réduction continue des dimensions des éléments des imageurs CMOS, la diffraction de la lumière joue un rôle crucial ; les couches de protection contre la lumière n'écrantent pas parfaitement la zone à protéger, ce qui fait qu'une quantité non négligeable de lumière peut pénétrer dans la région du nœud de stockage.

D'autre part, il a été démontré que des charges libres peuvent aussi bien affecter la sensibilité à la lumière du nœud de stockage, entraînant ainsi une dégradation des performances d'un imageur CMOS à obturation globale. Les charges peuvent être photo-générées dans des régions neutres, c'est-à-dire des régions sans présence de champ électrique, comme par exemple plus profondément dans la couche épitaxiale. Étant donné une longueur de diffusion qui est généralement supérieure aux dimensions des pixels à une concentration donnée de dopage de la couche épitaxiale de $10^{15}\,\mathrm{cm}^{-3}$ (ou même moins) à température standard, ces charges peuvent diffuser de manière aléatoire et être collectées par le nœud de stockage. Ce phénomène est particulièrement important pour les grandes longueurs d'onde, car les charges se photo-génèrent plus profondément dans la couche épitaxiale. Les barrières de diffusion comme le PWELL sont généralement exploitées pour empêcher les charges de diffuser vers certaines zones, mais leur efficacité peut être réduite en raison de l'énergie de la charge diffusante et de l'intensité du champ électrique de la barrière. Ces résultats visent à amener la communauté scientifique de l'imagerie à promouvoir la caractérisation de la sensibilité à la lumière parasite à plusieurs longueurs d'onde, car il a été démontré que la sensibilité à la lumière parasite des pixels est fortement dépendante de la longueur d'onde de la lumière incidente, compte tenu également de sa double nature dominée par la génération optique dans le domaine visible et par la diffusion des charges dans le domaine du proche infrarouge.

Le modèle développé a en outre été comparé aux résultats expérimentaux, montrant une bonne reproduction du comportement de l'insensibilité à la lumière parasite (1/PLS) en fonction de la longueur d'onde incidente. D'autre part, les rendements quantiques modélisés des photodiodes et des nœuds de stockage présentent des différences substantielles avec le résultat expérimental dans le domaine des courtes longueurs d'onde.

L'objectif du modèle développé est de servir d'outil rapide à exploiter par les designers de pixels pour améliorer les performances de sensibilité à la lumière parasite des imageurs CMOS à obturation globale d'une manière plus efficace par rapport à l'utilisation des simulations TCAD. Néanmoins, le modèle développé a ses limites, comme par exemple l'exigence d'une construction précise de la carte du champ électrique (pour le modèle de l'équation de

transport de Boltzmann) ou la modélisation de la probabilité de franchissement de la barrière de champ électrique (pour le modèle en ligne droite) qui peut nécessiter un travail supplémentaire pour la mise en place du modèle pour une nouvelle technologie. En outre, l'étalonnage du modèle avec des résultats expérimentaux peut également être nécessaire, étant donné sa nature 2D. Ensuite, la méthode a été développée dans le but de modéliser la sensibilité à la lumière parasite lorsque la photodiode n'est pas saturée ; dans ce dernier cas, les charges peuvent déborder vers le nœud de stockage, entraînant ainsi une augmentation apparente de sa sensibilité à la lumière. Le modèle développé n'est pas en mesure de décrire cette situation et les simulations TCAD doivent être exploitées pour une analyse plus complète.

Dans le troisième chapitre de ce travail, le modèle en ligne droite a été utilisé pour quantifier l'impact des éléments de conception sur la sensibilité à la lumière parasite des imageurs CMOS. Le rôle d'écrantage à la lumière par l'utilisation de couches d'interconnexion métalliques a été étudié. Conformément à la théorie de la diffraction de Fresnel, il a été démontré que les performances de la sensibilité à la lumière parasite sont dominées, en particulier aux longueurs d'onde les plus courtes ($\lambda < 650\,\text{nm}$), par le niveau d'écrantage métallique le plus faible ; l'ajout de niveaux d'écrantage métallique supplémentaires est souvent négligeable. Aux plus grandes longueurs d'onde, l'impact de la collection directe de la lumière par diffraction est atténué par la génération de charges plus profondes ; le choix de la couche métallique de protection présente donc un impact plus faible. L'impact de la diffraction sur la sensibilité à la lumière du nœud de stockage a été atténué par le positionnement de la couche métallique de protection au-dessus du nœud de stockage. Il a été démontré qu'une large couverture du nœud de stockage, c'est-à-dire la conception d'une couche d'écrantage de dimensions plus importantes par rapport à celles du nœud de stockage, contribue à réduire la sensibilité à la lumière de ce dernier. Il est néanmoins important de prêter attention à la couverture des couches métalliques d'écrantage, car la couverture d'une partie de la photodiode entraînera une réduction de la sensibilité à la lumière de cette dernière, limitant l'intérêt de l'amélioration de la sensibilité à la lumière parasite par l'exploitation des couches métalliques. L'application de ces règles empiriques pour l'amélioration des performances de l'efficacité d'obturation globale est néanmoins limitée par la technologie exploitée. Il a été largement démontré dans la littérature que l'Écran de Lumière à Tungstène Enterré (WBLS) est le choix privilégié pour un écrantage amélioré du nœud de stockage, limitant l'application des couches d'interconnexion métalliques comme écrantage aux technologies qui ne permettent pas l'intégration d'un WBLS.

Dans le quatrième chapitre de ce travail, une métrique standard pour mesurer la sensibilité à la lumière parasite des capteurs d'images CMOS à obturateur global a été développée, étant donné qu'aucune directive n'existe dans la norme EMVA 1288 pour ce champ d'application. La méthode est basée sur une mesure classique de l'efficacité quantique de la photodiode et sur le développement d'une mesure de l'efficacité quantique du nœud de stockage. Les résultats sont facilement applicables à tous les types imageurs CMOS à obturation globale à stockage en charge ainsi qu'à ceux à stockage en tension. La métrique développée a été testée sur une matrice de pixels 5T à obturation globale ; les résultats expérimentaux montrent la possibilité de mesurer avec précision la sensibilité à la lumière parasite en fonction de la longueur d'onde.

La deuxième partie de ce chapitre vise à développer un modèle de la sortie du capteur imageurs CMOS à obturation globale, prenant ainsi en compte le signal induit par la sensibilité non négligeable à la lumière parasite. La validité du modèle a été prouvée par des mesures expérimentales, montrant ainsi un comportement linéaire par rapport au nombre de lignes et aux conditions d'éclairage.

Étant donné le comportement linéaire du modèle, différentes méthodes de correction post-traitement des images ont été développées afin d'atténuer l'effet de la sensibilité à la lumière parasite des imageurs CMOS à obturation globale. Les méthodes de correction en post-traitement sont exploitées comme un moyen peu coûteux d'atténuer le problème de la sensibilité à la lumière parasite des imageurs CMOS à obturation globale, sans qu'il soit nécessaire d'explorer la voie coûteuse de l'amélioration du procédé technologique. Des méthodes de correction ont été développées pour un imageurs CMOS à obturation globale à stockage en charge exploitant des pixels 6T, étant donné l'impossibilité d'exploiter des pixels 5T à la fois pour l'opération d'intégration en lecture et pour la correction de la lumière parasite. Néanmoins, étant donné l'utilisation d'une trame de correction supplémentaire, la fréquence d'images minimale du capteur est réduite de moitié par rapport au fonctionnement normal. L'avantage des méthodes de correction développées, par rapport aux méthodes existantes dans la littérature, réside dans le fait qu'elles sont spécialement développées pour échantillonner l'intensité lumineuse pendant la phase de stockage & lecture, permettant ainsi de récupérer la quantité de charges parasites qui ont atteint le nœud de stockage. L'inconvénient de ces méthodes est qu'elles nécessitent une caractérisation précise de la sensibilité à la lumière parasite par pixel sur l'ensemble du capteur ; l'utilisation de la sensibilité à la lumière parasite par pixel peut entraîner des inexactitudes de correction lorsqu'il s'agit de pixels monochromatiques, car la sensibilité à la lumière parasite varie en fonction de la longueur d'onde. Néanmoins, les méthodes développées montrent des résultats prometteurs, ce qui en fait une alternative intéressante et rentable à l'amélioration de l'efficacité d'obturation globale des imageurs par procédé technologique, bien qu'il reste crucial de valider ces méthodes théoriques par des résultats expérimentaux.

Perspectives

Ce travail a permis de présenter une compréhension complète des phénomènes liés à la sensibilité à la lumière parasite des imageurs CMOS à obturation globale. Néanmoins, certains paramètres restent encore à caractériser. Les travaux futurs pourraient viser à mieux comprendre le comportement de la sensibilité à la lumière parasite en fonction de la température de fonctionnement ; cela nécessiterait une légère modification du modèle pour inclure le phénomène du scattering dans la résolution de l'équation du transport de Boltzmann, étant dépendant de la température. Une simulation et une caractérisation complètes de la réponse des pixels à l'angle d'incidence de la lumière dans les directions verticale et horizontale peuvent être recherchées ; les simulations permettraient de tester les différentes structures de pixels à différents angles d'incidence afin de choisir la conception la plus adaptée à l'application requise. Enfin, les travaux futurs pourraient porter sur le comportement de la sensibilité à

la lumière parasite à différentes concentrations de dopage, comme par exemple l'exploitation d'une couche épitaxiale à faible dopage pour augmenter la zone de déplétion de la photodiode et améliorer ainsi la sensibilité à la lumière de la photodiode, ou l'exploration des différentes concentrations de dopage de PWELL pour mieux comprendre l'efficacité de la barrière de potentiel à différentes longueurs d'onde.

Les simulations optiques et de transport présentées dans ce travail ont été réalisées en 2D. La modélisation de la structure en deux dimensions peut être satisfaisante lorsque la troisième dimension est homogène. Néanmoins, lorsque des structures plus complexes doivent être prises en compte et modélisées, comme par exemple la modélisation précise des micro-lentilles, les formes non rectangulaires de la photodiode ou du nœud de stockage, les simulations 3D deviennent obligatoires. Le développement d'un modèle 3D de transport de charge est donc nécessaire. Les simulations 3D peuvent également être exploitées pour valider les simulations 2D et le facteur de correction géométrique présenté précédemment. Les simulations 3D sont extrêmement longues et nécessitent donc une puissance de calcul élevée. Néanmoins, elles deviennent une option viable étant donné le rétrécissement continu du pas des pixels.

Enfin, des méthodes de correction en post-traitement ont été présentées pour les deux modes de fonctionnement des imageurs CMOS à obturation globale, bien que l'efficacité de la méthode n'ait pas encore été prouvée en faisant varier l'intensité lumineuse en fonction du temps. Les travaux futurs pourraient se concentrer sur l'application et le test expérimental des différentes méthodes de correction post-processus présentées, ce qui permettrait de caractériser leur efficacité et le bruit associé. La littérature a montré que les méthodes de correction post-processus constituent une option viable pour atténuer le problème de la sensibilité à la lumière parasite [SJI19] ; [Ge+19] ; la validation des méthodes de correction en post-traitement présentées pourrait constituer un moyen supplémentaire et rentable d'améliorer les performances des imageurs CMOS à obturation globale.

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Abstract — Distortion-free imaging of fast-moving objects has become crucial for a wide spectrum of applications, such as industrial machine vision, motion recognition and Earth imaging from space. CMOS Imaging technology has therefore evolved towards the "snapshot" capture operation, with the development of Global Shutter CMOS Image Sensors. Nevertheless, this type of sensors is affected by a non-negligible sensitivity of the Storage Node to parasitic light, limiting their use especially in strong-light environments. Despite the large efforts to reduce the Parasitic Light Sensitivity issue, there exist a general incoherence in modeling and characterizing this figure of merit. This thesis focuses on developing a framework for modeling, characterizing and mitigating Parasitic Light Sensitivity in Global Shutter CMOS Image Sensors. This is done through the development of a standard characterization method, a simulation method and different post-process correction methods that are successively exploited to give guidelines for improving sensor design and performances in a cost-effective way.

Keywords: CMOS Image Sensor, Global Shutter, Parasitic Light Sensitivity, Global Shutter Efficiency, Modeling, FDTD, Boltzmann Transport Equation, Image Post-Processing

Résumé — L'imagerie à haute-vitesse sans distorsions spatiales est devenue cruciale pour une large gamme d'applications comme la vision industrielle, la reconnaissance du mouvement et l'imagerie de la Terre depuis l'espace. La technologie d'imagerie CMOS a donc évolué vers une modalité de prise de vue appelée « snapshot », grâce au développement des Capteurs d'Image à Obturation Globale. Néanmoins, ce type d'imageurs présente une dégradation des performances due à une sensibilité à la lumière parasite non-négligeable du Nœud de Stockage, qui en limite l'exploitation. Bien que beaucoup de travaux aient été consacrés à la réduction de la Sensibilité à la Lumière Parasite, il existe des interrogations et des manquements relatifs à la caractérisation et la modélisation de cette figure de mérite. Ces travaux s'intéressent au développement d'un cadre pour la modélisation, la caractérisation et l'atténuation de la Sensibilité à la Lumière Parasite dans les imageurs CMOS à Obturation Globale. Le cadre se base sur le développement d'une métrique pour la caractérisation, d'une méthode de simulation et de différentes méthodes de correction en post-traitement dans le but de faire émerger des recommandations pour la conception et d'augmenter les performances des imageurs de manière efficace et peu couteuse.

Mots clés : Imageurs CMOS, Obturation Globale, Sensibilité à la Lumière Parasite, Efficacité d'Obturation Globale, Modélisation, FDTD, Équation du Transport de Boltzmann, Post-Traitement d'Images

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