THÈSE

En vue de l’obtention du

DOCTORAT DE L’UNIVERSITÉ DE TOULOUSE

Délivré par :

Institut Supérieur de l’Aéronautique et de l’Espace

Présentée et soutenue par :
Alice PELAMATTI
le mardi 17 novembre 2015

Titre :
Estimation et modélisation de paramètres clés des capteurs d’image CMOS à photodiode pincée pour applications à haute résolution temporelle

Estimation and modeling of key design parameters of pinned photodiode CMOS image sensors for high temporal resolution applications

École doctorale et discipline ou spécialité :
ED GEET : Micro et Nanosystèmes

Unité de recherche :
Équipe d’accueil ISAE-ONERA OILMPES

Directeur/trice(s) de Thèse :
M. Pierre MAGNAN (Directeur de thèse)
M. Vincent GOIFFON (Co-directeur de thèse)

Jury :
M. Thierry CAMPS - Président du jury
M. Pierre MAGNAN - Directeur de thèse
M. Vincent GOIFFON - Co-Directeur de thèse
M. Albert THEUWISSEN - Rapporteur
M. Tobi DELBRUCK - Rapporteur
Mme Xuezhou CAO
# Contents

List of Acronyms .......................................................... iii

Introduction ................................................................. 1

1 Pinned Photodiode CMOS Image Sensors ........................... 5
   1.1 Let’s start with some history ..................................... 5
   1.2 Figures of merit and non-idealities of digital image sensors . 7
   1.3 Active Pixel Sensors .................................................. 11
   1.4 Pinned photodiode CMOS Image Sensors ............. 15
   1.5 Conclusion .............................................................. 19

2 Modeling, estimation and measurement of charge transfer .......... 21
   2.1 Definitions ............................................................. 21
   2.2 Charge transfer mechanisms in Pinned Photodiodes .......... 22
   2.3 Experimental Measurements ....................................... 46
   2.4 Conclusion .............................................................. 53

3 Definition, estimation and modulation of the pinning voltage ....... 57
   3.1 Definition of the pinning voltage ................................ 57
   3.2 Modeling of the pinning voltage .................................... 59
   3.3 Overview on pinning voltage estimation methods ............... 61
   3.4 Temperature behavior of the pinning voltage ................. 72
   3.5 Static and dynamic pinning voltage modulation methods ..... 74
   3.6 Conclusions ............................................................. 89
   3.7 Summary of pro and cons of pinning voltage estimation methods . 91
4 Static and Dynamic behavior of the Full Well Capacity

4.1 Equilibrium Full Well Capacity ........................................ 94
4.2 Effect of the photon flux on the Full Well Capacity ............... 96
4.3 Temperature behavior of the FWC under stationary illumination 99
4.4 FWC variations as a function of temperature for different TG biasing conditions 99
4.5 Dynamic behavior of the Full Well Capacity ...................... 103
4.6 Conclusion ............................................................... 107

Conclusion and Outlook ..................................................... 111

Bibliography ....................................................................... 124

A Study on the effect of Gate Induced Leakage Current in charge domain global shutter detectors 125

B Estimation of the Charge to Voltage conversion Factor in PPD CIS 129

B.1 The mean variance method ............................................. 130
B.2 Non Linear Estimation method ........................................ 133
B.3 X-ray method with Fe$^{55}$ .............................................. 134

C Charge transfer modeling and simulation: theoretical derivations and codes 137

C.1 Flick’s law derivation from probability calculations ................ 137
C.2 Calibration of the simulation of charge diffusion in the PPD ........ 138
C.3 Simulation of the Random walk of charges in a PPD .............. 142

D Details on the readout electronics of the device under test ......... 147

D.1 Readout Circuit for the 1D pixel arrays ............................ 147
D.2 Simulations ............................................................... 147
D.3 Decoder ................................................................. 150
## List of acronyms

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Full Form</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>Analog-to-digital converter</td>
</tr>
<tr>
<td>APS</td>
<td>Active pixel sensor</td>
</tr>
<tr>
<td>BSI</td>
<td>back side illuminated</td>
</tr>
<tr>
<td>BW</td>
<td>Bandwidth</td>
</tr>
<tr>
<td>CCD</td>
<td>Charge coupled devices</td>
</tr>
<tr>
<td>CIS</td>
<td>CMOS image sensor</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary metal-oxide-semiconductor</td>
</tr>
<tr>
<td>CTI</td>
<td>Charge transfer inefficiency</td>
</tr>
<tr>
<td>CTE</td>
<td>Charge transfer efficiency</td>
</tr>
<tr>
<td>CVF</td>
<td>Charge to voltage conversion factor</td>
</tr>
<tr>
<td>DIBL</td>
<td>Drain induced barrier lowering</td>
</tr>
<tr>
<td>DR</td>
<td>Dynamic range</td>
</tr>
<tr>
<td>EFWC</td>
<td>Equilibrium full well capacity</td>
</tr>
<tr>
<td>EOTF</td>
<td>Electro-optical transfer function</td>
</tr>
<tr>
<td>FD</td>
<td>Floating diffusion</td>
</tr>
<tr>
<td>FF</td>
<td>Fill factor</td>
</tr>
<tr>
<td>FSI</td>
<td>front side illuminated</td>
</tr>
<tr>
<td>FWC</td>
<td>Full well capacity</td>
</tr>
<tr>
<td>GIDL</td>
<td>Gate induced drain leakage</td>
</tr>
<tr>
<td>GIL</td>
<td>Gate induced leakage</td>
</tr>
<tr>
<td>LADAR</td>
<td>Laser detection and ranging</td>
</tr>
<tr>
<td>LEFM</td>
<td>Lateral electric field modulation</td>
</tr>
</tbody>
</table>
**LIDAR**  Light detection and ranging
**PD**  Photodiode
**PPD**  Pinned photodiode
**PTC**  Photon Transfer Curve
**RS**  Reset transistor
**SF**  Source follower transistor
**SCR**  Space charge region
**SELX**  Column selection transistor
**SELY**  Line selection transistor
**SG**  Storage gate
**TAT**  Trap assisted tunneling
**TG**  Transfer gate
**TOF**  Time of flight
**QE**  Quantum efficiency

**List of symbols**

*CFD*   Floating diffusion capacitance capacitance
*C_{PPD}*   PPD capacitance
*D_{n}*   Electron diffusion constant
*E_{c}*   Conduction band
*E_{F}*   Fermi level
*E_{Fn}*   Electron quasi Fermi level
*E_{i}*   Intrinsic Fermi level
*E_{T}*   Trap energy level
*E_v*   Valance band
*N_C*   Effective density of states
*n_i*   Intrinsic doping concentration
$N_T$  Trap density
$V_{bi}$  Built-in voltage
$V_{DD}$  Power supply
$V_{DDST}$  Reset voltage
$V_{HITG}$  TG biasing voltage during the charge transfer phase
$V_{LOTG}$  TG biasing voltage during the light integration phase
$v_{th}$  Thermal velocity
$u_{th}$  Thermal voltage
$V_{pin}$  Pinning voltage
$\Phi_{ph}$  Photon flux
$\sigma_n$  Electron capture cross-section of interface states
$\mu_n$  Electron mobility
$T$  Temperature

List of constants

$k$  Boltzmann constant ($1.3806488 \times 10^{-23} \text{m}^2 \cdot \text{kg} \cdot \text{s}^{-2} \cdot \text{K}^{-1}$)
$q$  Elementary charge ($1.60217657 \times 10^{-19} \text{C}$)
$c$  Speed of light ($299'792'458 \text{ m} \cdot \text{s}^{-1}$)
$h$  Planck’s constant ($6.626 \times 10^{-34} \text{ m}^2 \cdot \text{kg} \cdot \text{s}^{-1}$)
$N_C$  Effective density of states for Si at 300K ($2.8 \times 10^{19} \text{ cm}^{-3}$)
$\rho_{Si}$  Silicon density ($2.33 \text{ g} \cdot \text{cm}^{-3}$)
Introduction

Digital images are part of the 21st century daily life. Thanks to the extremely fast improvement of CMOS Image Sensors (CIS) technology, high-performance commercial image sensors, which used to be confined to high-end or professional cameras during the “Charge Coupled Devices (CCD) era”, can nowadays be found on smart-phones and on tablets. More and more functions can be integrated in smart pixels and every year manufacturers push performances’ limits a little farther. Each technological jump opens the door to new commercial and scientific applications.

Space imaging is a particularly demanding field, as detectors need to meet the mission requirements while guaranteeing a low power budget, radiation hardness, a long term reliability and, most of all, unlike “earthborne” cameras, where the optics can be adapted to meet the detector requirements, “spaceborne” imagers must often comply with the optical constraints of the payload. In the last decade there has been a particular focus on space missions based on high temporal resolution detectors, (such as LIDAR detectors) for meteorology [MFT08], altimetry applications or more generally 3D imaging applications, for the guidance, navigation and control of planetary landers [CC08] (for example to select a safe landing site), for docking in planetary orbit [Kol+15], or for the estimation of the attitude and geometry of space debris. The detectors characteristics are very specific to each mission, however, in general, the main challenge is to sample an incoming waveform as fast as possible within a finite time window.

In standard image sensors, the frame rate is often limited by the maximum output rate, i.e. by the time required to access the pixel array, to perform the analog to digital conversion and to send data off the chip [ED+09]. To enhance the sampling rate, a first solution consists in parallelizing the readout by means of multiple outputs, however the maximum number of outputs is strongly limited by the increasing complexity of the acquisition set-up and the power budget. An alternative approach to continuous frame acquisition consists in separating the acquisition phase from the readout and analog-to-digital conversion phases. This can be achieved by storing temporal samples on analog memories “in-situ” (on chip or in-pixel) during the acquisition time window, and reading the data in a second time. This acquisition mode is often referred to as “burst mode” in opposition to the “continuous mode”. The first published successful achievements of image sensors with in-situ storage are based on CCD sensors [Kos+96]; [EMT99]. A synthetic review of the progress in such direction is given by Etoh et al. in [Eto+11]. Outstanding performances can be achieved with CCD burst sensor, however this incredibly high sampling rate often comes at the expense of a very high power consumption (and self-heating). For most scientific and consumers applications, the main trend is to reproduce CCDs functionalities using CIS technology, which usually comes at a lower cost, offers better power budget performances [Fos93], and unlike CCD technology, is in continuous evolution and should still be available for the next few years 1.

---

1The security of long term supply is a particularly critical topic for space applications, as more than 10 years can pass between the preliminary design of the instrument and the launch.
Introduction

For this reason, a few years after the development of the first CCD burst sensors, we find the first implementations of CMOS detectors with in-situ frame storage [Kle+04]; [ED+11]. The sampling performances of these detectors are not yet comparable to the latest CCD burst sensors (which target 1 Gfps [Eto+13]), nevertheless the recent advent of 3D stacking [Son] can give a great boost to CMOS burst sensors in terms of storage capabilities [Bon+13b].

The maximum sampling rate that can be reached with an image sensor strongly depends on the gain and noise performances of the detector. In fact, a very short sampling time implies a very low signal, and therefore a very low noise floor (or a very high input signal) is necessary to guarantee a good signal-to-noise ratio. Pinned Photodiode (PPD) CMOS Image Sensors offer intrinsically better noise performances than standard CIS (the so called 3T Active Pixel Sensors) and are thus good candidates for high-temporal resolution detectors. An example of a PPD-based burst image sensor, which demonstrated speed capabilities up to 10 Mfps can be found in [Toc+12]. The device has 6 parallel output circuits and output amplifiers and is divided into two zones, one containing the 2D pixel array, and the other the arrays of 104 analog memories per pixel. An alternative (or complementary) approach to multiple storage sites associated to single PPD outputs consists in releasing the speed constraints on the in-pixel electronics by increasing the number of outputs per pixel (multi-tap detector). As PPD pixels are based on charge transfer (and not on charge partition), multi-tap pixels can be easily implemented in PPD CIS and is a currently adopted solution for demodulator pixels (lock-in pixels) for Time-of-Flight applications [Lan+00]; [BLS06]; [Sto+11]; [Kim12]; [Sto+11]; [Bon+13a]; [Han+14].

Once all these speed-up solutions have been implemented, the ultimate sampling speed limit in PPD CIS is due to the time required to transfer electrons from the collection site (the PPD) to the readout node. This transfer time depends on the carrier transport mechanisms that are involved during charge transfer and on the fine tuning of both the pixel design and the technological process to optimize the potential profile along the charge transfer path. Minimizing the transfer time often involves a trade-off between different design parameters, while taking into account the mission/application constraints; therefore during the development of a high temporal resolution PPD CIS detector, it is of primary importance to fully understand the physical meaning of each of the design parameters and how they affect one-another.

This thesis focuses on the definition, analytical modeling, simulation and measurement of PPD CIS key parameters for the design of high temporal resolution detectors. The transfer time, which in PPD CIS, represents the bottle neck in terms of temporal resolution, is addressed in chapter 2. In particular, charge transfer is simulated by means of a Montecarlo model implemented in Matlab® which takes into account thermal diffusion, charge drift and thermionic emission across the potential barrier located at the interface between the PPD and the transfer gate (TG). The effect of the TG fringing field, of self-induced drift and charge trapping under the TG is also discussed. The results of numerical simulations are then compared to TCAD simulations and to experimental measurements performed on dedicated pulsed storage gate pixels which allow reproduction of a worst case scenario, when the packet of photo-charges is generated at the far end of the PPD.

A second important figure of merit used by designer to maximize the charge transfer
efficiency is the pinning voltage (which represents the maximum PPD potential) which is often used as a reference to optimize the TG doping implants and biasing voltages, and sets a limit to the minimum power supply. In the CIS community the pinning voltage is estimated with different methods, which are based on very different physical principles and which do not always provide the same physical parameter and/or are not based on solid semiconductor devices equations. The first part of the third chapter of this work is dedicated to the definition and physical meaning of the pinning voltage and to a comparison of pinning voltage estimation methods. In particular, it is shown that the commonly accepted theoretical definition of this parameter does not correspond to the physical parameter which is measured with the existing methods. The chapter also presents a temperature analytical model of the pinning voltage which is supported by experimental measurements.

To enhance charge transfer speed with respect to simple thermal diffusion, the most intuitive solution is to induce an electron drift field in the PPD [Tub+09]; [Tak+10]; [Sto+11]; [Han+14]. The maximum electric field (and thus the maximum charge transfer speed that can be reached with a particular detector) depends on the PPD length and on the maximum potential drop that can be generated within the PPD, i.e. the pinning voltage. Two potential modulation methods which have been proposed in the literature to generate static [Tak+10] and dynamic [Han+14] electric fields, respectively, are addressed in the second part of chapter 3. In particular, the working principle and limitations of these methods are discussed based on TCAD simulations and on experimental measurements performed on isolated structures and on small pixel arrays.

In low light conditions, the output signal is mainly affected by the device signal-to-noise ratio and by charge transfer performances. On the other hand, when large signals are involved, the amount of collected photocharges is limited by the PPD Full Well Capacity (FWC). Chapter four is dedicated to the modeling of the FWC. In particular it is shown that the PPD FWC is a strong function of the working temperature, of the biasing conditions and of the signal level. This work introduces for the first time the concept of Equilibrium Full Well Capacity (EFWC) which corresponds to the PPD FWC in the dark with TG in accumulation mode and is the only FWC value which only depends on the PPD properties. As shown in this work, the EFWC is an important value to refer to when choosing the illumination conditions or for example when studying the behavior of the FWC for different experimental conditions or after irradiation. this work also discusses the dynamic behavior of the FWC under non-stationary illumination conditions. It is shown that if the illumination level is suddenly changed (as would be the case in dynamic illumination conditions), we observe a discharge/charge of the PPD toward a new equilibrium condition. The charge transient strongly depends on the initial and final illumination levels, and can take up to several minutes for a light-to-dark illumination step. The dynamic behavior of the FWC can lead to significant errors in high temporal resolution applications, such as ToF applications, which are based on pulsed light measurements or, more generally, aim at imaging rapidly varying scenes. For this reason, in such applications the impinging photon flux should always be chosen low enough to maintain the PPD charge below the EFWC.

The models developed in this work could help manufacturers predicting how the differ-
ent experimental conditions can affect the detector performances for a specific high temporal resolution application, and to take these effects into account during the design process. They can also support characterization steps in terms of choosing the right characterization method (especially for the CVF, the FWC and the pinning voltage). In particular, this work emphasizes the importance to define standards for the estimation of PPD CIS figures of merit, in order to provide users with well defined and comparable parameters.
1.1 Let’s start with some history . . .

Photography is the science and art of creating pictures by recording electromagnetic radiation on a radiation-sensitive medium, such as a photographic film, or a semiconductor device. This practice was born at the beginning of the 19th century, when many scientists and inventors, like Joseph Nicéphore Niépce, Louis Daguerre, John Herschel, Hercules Florence and William Fox Talbot developed the photographic process, some collaborating with each others, some unaware of the work of their colleagues. The photographic science resulted from the combination of many inventions and sciences that had been developed in the previous centuries, such as the pinhole camera, the camera obscura, optics and chemistry. The middle class of the Industrial Revolution was the perfect audience for an art that could enable faster and fancier portraits, therefore the historical context had been fundamental for the development of photography. Only twenty years after the first black & white picture was taken, colored pictures were introduced by using three layers of emulsion to capture full color at every point in the image. Technology kept improving and less than one century after the invention of the daguerreotype, pictures were made on 35mm film [Ede78].

In 1965 G. Weckler introduced at Fairchild the first p-n junction photodetector in integration mode [Wec65]; [Wec67]. This early device was based on the observation that the potential of a reversed biased p-n junction, if left floating (by activating a switch), decreases at a rate which depends linearly on the intensity of the impinging photon flux. In particular, the measured potential variation can be expressed as a function of the p-n junction capacitance $C_d$, of the detector area $A_d$ and of the photocurrent density $J_{ph}$:

$$\frac{dV}{dt} \approx \frac{J_{ph} A_d}{C_d} \quad (1.1)$$

where the photocurrent $I_{ph} = J_p A_d$ is due to the generation of electron-hole pairs resulting from the absorption of photons with energy $E_{ph}$ greater than the semiconductor band-gap $E_g$ [Sze85]. In reverse biased conditions, electrons which are photogenerated within the p-n junction space charge region (SCR) (or simply reach the SCR by thermal diffusion) are swept by the electric field within the SCR, resulting in a reduction of the junction reverse bias.
Chapter 1. Pinned Photodiode CMOS Image Sensors

Figure 1.1: (a) Ilse Bing, Self-Portrait in Mirrors, 1931. (b) Slow motion image acquired with the latest sony RX100 IV camera (from www.sony.net).

The energy of a photon can be expressed as a function of the photon wavelength $\lambda$ as [Sze85]:

$$E_{\text{ph}} = \frac{hc}{\lambda}$$  \hspace{1cm} (1.2)

where $h$ is the Planck’s constant and $c$ the speed of light. The amount of collected photo-electrons per photons impinging on the photodetector surface is referred to as Quantum Efficiency:

$$\text{QE}(\lambda) = \frac{J_{\text{ph}}}{q\Phi_{\text{ph}}(\lambda)}$$  \hspace{1cm} (1.3)

with $\Phi_{\text{ph}}(\lambda)$ the impinging photon flux per unit area and $q$ the elementary charge. The QE depends on optical reflections, on optical absorption and on the photodetector capability to collect the generated carriers, it is thus a strong function of $\lambda$ [Sze85]. As a general rule, $I_{\text{ph}}$ can be expressed as:

$$I_{\text{ph}} = A_d \int_{\lambda} \Phi(\lambda)\text{QE}(\lambda)d\lambda$$  \hspace{1cm} (1.4)

The origin of digital imaging is usually associated to the invention of Charge Coupled Device (CCD) by Willard Boyle and George E. Smith at the AT&T Bell Labs in 1969 [BS70], for which they were awarded a Nobel Prize for Physics in 2009. In 1968, P. Noble worked on the first self-scanned MOS pixel array [Nob68], laying the foundations for the later CMOS Active Pixel Sensors (APS) [Fos93], often refereed to as three-transistors (3T) APS. Given the outstanding performances of CCDs [The95]; [Jan01] with respect to MOS sensors, both scientific and commercial image sensors have been mainly based on the CCD technology until the 90s, when CMOS Image Sensors (CIS) slowly took over CCDs under an increasing market pressure for low cost electronics and (more recently) low cost image sensors for con-
1.2. Figures of merit and non-idealities of digital image sensors

Design, technology and size all play fundamental roles in the final performances of an image
detector. Hereafter, a brief general description, supported by some visual examples, of the
main figures of merit and non-idealities of digital image sensors. The list of parameters is
far from being exhaustive, and does not include parameters which are specific to particular
detector technologies. More details on CCD figures of merit can be found in [Jan01]; [The95].
A detailed analysis on PPD CIS key design parameters which are particularly relevant for high
temporal resolution applications, such as the transfer time, the pinning voltage (\(V_{\text{pin}}\)) and
the dynamic behavior of the Full Well Capacity (FWC) are discussed in dedicated chapters
of this work (chapters 2, 3 and 4, respectively). For more details on other figures of merit in
CIS, such as noise, fixed-pattern noise and optical performances, the reader should refer to
[FH14] and the references therein.

1.2.1 Light Sensitivity

The light sensitivity of a detector corresponds to the gain between the input signal (the photon
flux here), and the output signal. Photo-detection, can be divided in three main phases:

- Photon-to-charge conversion (which determines how many photo-electrons are generated
  in the detector per number of impinging photons).

\(^1\)In 2015, a market of about 98 billion USD for CIS has been reported by Chipworks [Fon15]. Chipworks
also reported more than 2500 patents in 2014.
\(^2\)For more details on the evolution of CIS, the reader can refer to the reference provided in this chapter or
to the recent review on PPD CIS by E. Fossum [FH14].
Chapter 1. Pinned Photodiode CMOS Image Sensors

- Charge collection (which determines how many generated photo-electrons are actually collected by the photodiode).
- Charge-to-voltage conversion (which determines the variation of the output voltage per collected photo-electron).

The amount of collected photo-charges per number of impinging photons (which takes into account the first two steps of light detection) is usually expressed by means of the quantum efficiency (QE). The QE of a detector depends on many different parameters, among which optical reflection phenomena, the fill factor (i.e. the ratio between the “useful detection area” of a pixel and its total surface) and the depth of absorption of the impinging photons with respect to the extension of the collection volume of the photodiode. Almost 100% QE can be reached nowadays with back-side illuminated detectors associated to micro-lenses. Charge-to-voltage conversion capabilities are expressed by means of the charge-to-voltage conversion factor (CVF). The CVF depends on the value of the capacitance on which the conversion is performed. In particular, the smaller the capacitance the larger the CVF. The product of the QE and the CVF determine the overall detector light sensitivity.

1.2.2 Dark current

If a detector is left in the dark, we always measure a small output signal due to the collection of thermally generated carriers. This “background” signal is often referred to as dark current, or dark signal. The dark current is a strong function of temperature, and strongly depends on the type of detector and on the quality of the technology. As discussed in the next section, the dark current not only adds an offset to the signal, but its fluctuations also contribute to the total readout noise, therefore it should be made as small as possible to obtain good quality images.

1.2.3 Signal-to-noise ratio

One of the first criteria which makes us qualify an image as a “good” image, is the signal-to-noise ratio (SNR). The SNR is usually expressed in dB as:

\[
SNR = 20 \log \left( \frac{S_{in}}{\sigma S_{in}} \right)
\]  

(1.5)

where \(S_{in}\) is the input signal (for example the number of collected photo-electrons) and

\[
\sigma S_{in} = \sqrt{\sum_i \sigma_i^2 / G_i^2}
\]  

(1.6)

is the root mean square (r.m.s) noise referred to input \(^3\).

\(^3\)With \(G_i > 1\) a gain factor used to refer each noise contribution to the input.
1.2. Figures of merit and non-idealities of digital image sensors

Figure 1.2: Comparison between images with good (left) and poor (right) SNR.

Noise in image sensors can have very different natures [Jan01]:

- The unavoidable photon shot noise is due to the statistical fluctuations of the number of photons impinging on the detector. Its r.m.s value is equal to the square root of the mean signal value.

- The dark current shot noise is due to the statistical fluctuations of the number of carriers participating to the dark current. The higher the dark current, the higher this noise contribution.

- The reset KTC noise, originates from the statistical fluctuation of the potential across a capacitance after reset. Its contribution depends on the mode of operation of the device.

- The transistors of the readout chain also participate to the fluctuation of the output signal, both with a low frequency noise contribution (1/f flicker noise) and white thermal noise (Johnson noise or thermal noise).

As a general rule, to maximize the SNR, signal must be amplified as soon as possible, so that all noise contributions which come after the amplification in the readout chain are negligible.

1.2.4 Dynamic Range

The Dynamic Range (DR) of a detector is the ratio between the maximum and minimum detectable signals ($S_{\text{max}}$ and $S_{\text{min}}$), respectively. It is often expressed in dB as:

$$DR = 20 \log \left( \frac{S_{\text{max}}}{S_{\text{min}}} \right)$$  \hspace{1cm} (1.7)
Chapter 1. Pinned Photodiode CMOS Image Sensors

Figure 1.3: Comparison between images with good (left) and poor (right) DR.

Figure 1.4: Comparison between images with (left) and without (right) FPN correction.

$S_{\min}$ is often limited by the noise floor, whereas $S_{\min}$ can be limited by the saturation of the readout electronics, or by the Full Well Capacity (FWC) of the detector, which represents the maximum amount of charge that can be collected by pixels. In order to maximize the DR, logarithmic detector solutions have been proposed in the literature [PKW05]; [NZA11].

1.2.5 Fixed Pattern noise

Fixed pattern noise (FPN) indicates a fixed non-uniformity of the detector. It is mainly associated to process non uniformity across the pixel array, which result in variations of the dark current signal, and of the gain of both in-pixel amplifiers (if present) and column amplifiers. FPN can often be suppressed by flat field correction methods.
1.3. Active Pixel Sensors

1.2.6 Contrast

The contrast of an image reflects the ability of a detector to image sharp black-white edges. One of the optical key parameters of detectors associated to image contrast is the Modulation Transfer Function (MTF) [EM05], which roughly gives the amplitude of the output signal as a function of the spatial frequency.\(^4\)

![Figure 1.5: Comparison between images acquired with a detector presenting good (left) and poor (right) MTF.](image)

1.2.7 Image lag

If we acquire a frame and then suddenly close the shutter of the camera, the following frames should ideally be completely dark. However, for some detectors, after closing the shutter, we observe a sort of “ghost” image, which slowly fades away as the successive frames are acquired. This phenomenon is referred to as image lag, and can originate from very different mechanisms depending on the type of detector.

1.3 Active Pixel Sensors

When we talk about Active Pixel Sensors (APS), we refer to a pixel-array where one or more transistors are integrated in the pixels to amplify and buffer the acquired photo-charge signal. The schematic circuit of a 3-transistors (3T) APS and the schematic diagram of a 3T APS pixel are shown in Fig. 1.7 and 1.8, respectively.

Pixels are composed of a photosensitive element (the photodiode PD) which is responsible for the collection of photogenerated carriers and for the charge-to-voltage conversion. The three transistors are the reset transistor (RS), the source follower transistor (SF) and the line

\(^4\)Where by spatial frequency we refer to the inverse of the size if the smallest details in the image.
Chapter 1. Pinned Photodiode CMOS Image Sensors

Figure 1.6: Comparison between images acquired with a detector presenting no image lag (left) and with image lag (right).

(a) Before closing the shutter
(b) 1st image after closing the shutter
(c) 2nd image after closing the shutter
1.3. Active Pixel Sensors

Figure 1.7: Schematic diagram of a 3-transistors APS. A more detailed schematic of the pixel is shown in Fig. 1.8.

Figure 1.8: Schematic diagram of a 3T APS pixel. STI stands for Shallow Trench Isolation, PMD stands for Pre-Metal Dielectric.
selection transistor (SELY). The RS transistor is used as a switch to reset the PD potential to \(V_{\text{DDRST}}\) before starting light integration. As discussed later, different readout modes can be enabled by changing \(V_{\text{DDRST}}\), thus the latter is often separated from the analog power supply \(V_{\text{DD}}\). The SF transistor acts as a buffer and allows a low impedance readout of the pixel output voltage. The SELY transistor is used as a switch to connect the output of the pixel to the column bus.

For each column there are a n-MOS current sink and two output circuits, one for the sampling and readout of the reference (\(V_{\text{ref}}\)) and one for the sampling and readout of the signal (\(V_{\text{sig}}\)). Signal and reference are sampled on the storage capacitance \(C_{\text{ref}}\) and \(C_{\text{sig}}\), respectively, by activating the switches SHS and SHR. The output stages consist of a p-MOS in source follower, associated to a column selection transistor (SELX) and to a p-MOS current source (which has usually a very large W/L ratio as it must drive an output capacitance which can be of the order of ten or several tens of pF). Pixels are organized in a 2D-array, and can be accessed independently by activating simultaneously the corresponding line (SELY on) and the corresponding column (SELX on).

A typical readout timing diagram is shown in Fig. 1.9. After the reset, the photodiode potential is left floating and its potential starts to decrease as photocharges are integrated on the PD capacitance. At the end of the integration time, \(V_{\text{sig}}\) is sampled by activating SHS, then the PD is reset by activating RS and \(V_{\text{ref}}\) is sampled by activating SHR. The output signal is then calculated as \(V_{\text{ref}} - V_{\text{sig}}\). As the sampled reference value corresponds to the reset potential of the following integration phase, this readout mode is based on a “Non-Correlated Double sampling” (NCDS). Because of NCDS, in standard 3T APS the signal to noise ratio is significantly worsened by the contribution of reset noise (KTC noise) [Pai+00].

The RST signal is associated to internal logic, so that only one line is reset at the time. This means that the light integration windows of two successive lines are always shifted of the time \(t_{\text{line}}\) required to read one line. This readout mode, called “rolling shutter mode”, is not suitable when it comes to high speed image sensors as it can result in significant image distortion for rapidly changing imaged scenes.

![Figure 1.9: Typical timing diagram for the readout of a 3T APS.](image)
1.4. Pinned photodiode CMOS Image Sensors

1.3.1 Soft reset and hard reset

Depending on the requirements of the target application, two different reset operation modes can be implemented: hard reset and soft reset [Pai+00]. “Soft reset” consists in biasing the RS transistor during the reset phase at the same potential as the power supply ($V_{DDRST}$), so that, as the FD potential approaches $V_{DDRST} - V_t$ (with $V_t$ the RS transistor threshold voltage), the RS transistor enters in sub-threshold conduction. This operation mode has a triple advantage: it significantly reduces KTC noise, screens the FD potential from the fluctuations of the power supply. However, since during the last phase of the FD reset, the RST transistor is in sub-threshold conduction (exponential I-V behaviour), therefore the charge of the PPD capacitance is very slow (logarithmic approach to final reset level). As a result, for a given RST pulse lengths, different reset levels can be reached depending on the initial FD potential, i.e. depending on the signal level during the previous light integration phase. As 3T APS operation is based on a NCDS read-out, this can lead image lag. To minimize these phenomena the APS can be operated in “hard reset” mode, where the RS transistor gate potential is kept at least one $V_t$ above $V_{DDRST}$ during reset. This operation mode guarantees that the FD is never reset in sub-threshold conduction (without, or very low, image lag). However all the advantages of “soft reset” are lost, thus noise performances are poorer and the dynamic range in smaller.

1.4 Pinned photodiode CMOS Image Sensors

The first pinned photodiode (PPD) based image sensor was invented by Teranishi et al. in 1982 to reduce image lag in CCD detectors [Ter+82]. In 1995, Lee at al. introduced PPDs in CMOS sensors, inventing the so called 4T PPD CIS. Despite the additional costs and masks of the PPD CIS technology, PPD-based CIS are currently the main detectors for commercial cameras thanks to the multiple advantages brought by this novel structure in terms of noise and sensitivity. They also find numerous applications in high-end applications, in particular for Time-of-Flight (ToF) applications such as fluorescence life-time imaging [YK06]; [YIK09]; [MC11]; [Li+12] or ranging [Tub+09]; [Tak+10]; [Han+14].

1.4.1 Structure

A schematic drawing of a PPD pixel is shown in Fig. 1.10: the photosensitive element (the PPD) is associated to a Transfer Gate (TG), which isolates the PPD from the FD during light integration (TG off) and enables electron transfer from the PPD to the FD for the readout of the output charge (TG on).

The PPD is a buried junction photodiode formed by a double p+np junction. The p+ surface implant (pinning implant) significantly reduces the dark current with respect to standard 3T APS, as it isolates the PPD depletion region from the generation-recombination centers located at the Si – SiO$_2$ interface (because thermally generated carriers recombine in
Chapter 1. Pinned Photodiode CMOS Image Sensors

the p+ layer before reaching the PPD SCR). For the same purpose, the PPD is also usually surrounded by a p-well that isolate the SCR from the Shallow Trench Isolations (STI). The doping concentrations of the PPD layers (\(N_{\text{a\_pin}}\) and \(N_{\text{d\_PPD}}\) for the pinning implant and the n implant, respectively) are often tuned so that the upper junction can be approximated to a one-sided junction (i.e. the depletion region does not touch the surface and is mainly confined to the n-region). Usually \(N_{\text{d\_PPD}} \gg N_{\text{a\_epi}}\) (with \(N_{\text{a\_epi}}\) the doping of the p-type epitaxy), so that the extension of the SCR of the lower junction in the n-region is negligible with respect to the one of the upper junction. As discussed in chapters 3 and 4, this results in a larger pinning voltage and therefore in a larger equilibrium full well capacity.

As detailed in chapter 3, because of this peculiar buried structure, the PPD potential \(V_{\text{PPD}}\) is “confined” between the surface potential and the PPD maximum potential (referred to as pinning voltage \(V_{\text{pin}}\)). This means that if the PPD is suddenly connected to a deeper potential well (with \(V_{\text{well}} > V_{\text{pin}}\)), \(V_{\text{PPD}}\) starts increasing as charges are being transferred to the neighboring potential well, until reaching \(V_{\text{PPD}} = V_{\text{pin}}\). Thanks to this potential floor, true charge transfer can be achieved in PPDs, whereas with standard photodiodes, only charge sharing is possible (Fig. 1.11).

The TG is a transistor where the source and the drain correspond to the PPD and the FD, respectively. Depending on the technology, specific implants can be included under the TG, for example to isolate the PPD from the FD (these implants are often referred to as Anti Punch-Through implants, APT) or to modulate the TG threshold voltage along the TG channel in order to minimize charge spill back from the FD to the PPD [BBK12] and/or to avoid creating potential pockets or potential barriers along the charge transfer path [Jan01].

The FD and the RS, SF and SEL transistors are strongly reminiscent of the structure of a 3T APS pixel, except that the FD is not used here to collect photo-electrons, but to perform the charge to voltage conversion. As the most simple structure of a PPD pixel is made of 4 transistors (TG, RS, SF, SELY), PPD CIS are sometimes referred to as 4T APS. Note that in practice, PPD pixels are rarely limited to 4 transistors, as additional transistors can be included to implement specific features (such as anti-blooming or global shutter functions).

1.4.2 Principle of operation

A typical timing diagram for a 4T pixel is shown in Fig. 1.12. At the end of the integration time, the FD is reset by activating the RS transistor and \(V_{\text{ref}}\) is sampled. The TG is pulsed on to transfer the PPD charge \(Q_{\text{PPD}}\) to the FD. \(V_{\text{sig}}\) is sampled a new integration phase can start. Like in 3T APS, the output charge \(Q_{\text{PPD}}\) is estimated as

\[
Q_{\text{PPD}} = \frac{V_{\text{ref}} - V_{\text{sig}}}{\text{CVF}}
\]

(1.8)

Two main differences can be identified with respect to the operation of a 3T pixel:

- The charge to voltage conversion is performed on the FD (and not on the photodiode,
1.4. Pinned photodiode CMOS Image Sensors

Figure 1.10: Schematic drawing of a PPD pixel. APT stands for Anti Punch-Through implant.

Figure 1.11: Whereas true charge transfer can be implemented by associating a PPD to a TG and a FD (a) only charge sharing can be implemented with a standard PD (b).
as in 3T APS), thus the CVF does not depend on the PPD capacitance (i.e. the pixel gain can be adjusted independently from the PPD area). A study on CVF estimation methods for PPD CIS can be found in appendix B.

- No additional reset phase is necessary between the sampling of $V_{\text{ref}}$ and the sampling of $V_{\text{sig}}$. Thanks to this Correlated Double Sampling (CDS) operation, the output signal is not affected by reset noise.

### 1.4.3 Rolling Shutter vs. Global shutter operation

As introduced in the previous section, in PPD CIS, charge collection and charge readout are performed on two different capacitance (the PPD capacitance and FD capacitance, respectively) and are two independent operations. In fact, if we neglect eventual leakage currents affecting the FD, once the TG has been turned off (after charge transfer), all the additional photo-charges collected by the PPD do not contribute to the output signal, which is memorized on the FD capacitance. This means that whereas in 3T APS only rolling shutter readout mode is possible, in PPD CIS the timing diagram can be adjusted so that all the lines of the array perform light-integration simultaneously. As this operation mode allows equivalent function of a shutter, it is referred to as “global shutter” (GS) operation. With respect to rolling shutter operation, this read-out mode is much more suitable for high speed imaging applications as it strongly reduces image blurring and motion artifacts.

Different GS PPD CIS detectors which enable CDS have been reported in the literature, where $V_{\text{ref}}$ and $V_{\text{sig}}$ are stored either in the voltage domain (by sampling the reference and signal potentials on additional storage capacitors [Mey13]; [WM15]; [Lin+15]) either in the charge domain (by implementing multiple transfers [Lau+07]; [YIK10]; [Sak+12]). As discussed in [Mey13], the charge storage domain approach offers the lowest readout noise, however the sampled charge can be affected by the parasitic light sensitivity of the storage.
node. As addressed in appendix A, another phenomenon which can compromise the output signal in charge domain GS is the Gate Induced Drain Leakage (GIDL) current of the TG.

1.5 Conclusion

Due to their very good noise SNR capabilities and to the possibility to implement true charge transfer, PPD CIS technology is an interesting candidate for high temporal resolution detectors. The latter require fast sampling of an incoming input signal, and often involve the readout of extremely low signal levels (due to the short integration time per sample). To conceive a high performance high temporal resolution PPD CIS detector, designers often have to make trade-offs between optical constraints, speed performance, noise performance, while taking into account typical signal levels and experimental conditions. For instance, to maximize the SNR, the PPD should be designed as large as possible, however, this would lead to a worsening of the detector temporal resolution, therefore, as discussed in chapter 2, an optimum trade-off must be found between speed and PPD size. Another PPD CIS key design parameter is the pinning voltage, discussed in chapter 3, which must be engineered, depending on the available power supply and on the design of the TG, to guarantee a good transfer efficiency (in particular it must be adjusted to be smaller than the TG channel potential and FD potentials to enable charge transfer and to avoid spill back of charges from the FD to the PPD). By modulating the pinning voltage (with geometrical and/or doping solutions, or more exotic approaches), a drift field can be generated within the PPD to enhance the charge transfer speed. As discussed in chapter 3, each modulation method has its advantages and limitations, and introduces different trade-offs in terms of PPD geometry. Finally, during the design process, one also needs to size the PPD depending on the final target application. In particular, in small PPDs, the signal can be larger than the PPD Equilibrium Full Well Capacity (EFWC). In stationary illumination conditions, this results in charge blooming. A smart sizing of the full well of the device becomes even more critical in non-stationary illumination conditions, where significant measurement errors can result from the dynamic behavior of the FWC following a sudden change in the illumination level.
Chapter 2

Modeling, estimation and measurement of charge transfer

As discussed in the introduction of this work, to design a detector for high temporal resolution applications, a widely used approach consists in implementing a “burst readout mode”, which is based on the in-pixel storage of temporal samples. In PPD CIS, the sampling-rate bottleneck corresponds to the maximum speed at which charge can be collected and transferred to a storage capacitance (the FD in 4T APS). If we make the assumption that charge collection is almost instantaneous\(^1\), and we neglect the limited bandwidth of the electronics, the device final temporal resolution depends on the time required to transfer all the collected charge to the storage node/s.

In some scientific applications, such as space applications (often tied to CCD-solutions heritage), large pixel areas can be required to match the constraints dictated by the optics [Kra+13]). During the design of such large pixel PPD-based detectors, it is important to understand the effect of the length of the charge transfer path (thus of the PPD length) on charge transfer efficiency, in order to reach an optimum trade-off between the geometrical requirements of the instruments and the final performances of the detector.

This chapter discusses the different charge transport mechanisms that are responsible for charge transfer in PPD CIS and how they are affected by the design of the PPD pixel. In particular, charge transfer is simulated based on a Montecarlo simulation of the random walk of single carriers. These results are compared to TCAD simulations and to experimental measurements obtained on a novel dedicated pulsed gate pixel structure.

2.1 Definitions

Charge transfer can be characterized in terms of transfer time or Charge Transfer Efficiency (CTE). The most intuitive definition of “transfer time” would be the time required to transfer all the photo-electrons collected during charge integration from the PPD to the FD. As discussed in the following sections, charge transfer is a highly random process, therefore the term “transfer time” makes sense only if we refer to an average transfer time. For this reason,\(^1\)

\(^1\)For example if the wavelength of the input signal is chosen so that most of the photocharges are generated within the PPD or if a vertical drift field is generated within the epitaxy [Tub+09] to ensure an “instantaneous-like” electron collection.
Chapter 2. Modeling, estimation and measurement of charge transfer

it is more common to characterize detectors in terms of CTE:

\[
CTE = \frac{Q_{\text{out}}}{Q_{\text{PPD}}}
\]  

(2.1)

or Charge Transfer Inefficiency (CTI) (where CTI = 1 − CTE), which gives the average output charge (or residual charge for the CTI) normalized with respect to the total charge stored in the PPD before transfer. As discussed in chapter 1, when 3T APS are readout in soft reset mode, a ghost image can appear for non-stationary illumination conditions because of an incomplete reset of the photodiode potential. This phenomenon is often referred to as “image lag”. As incomplete charge transfer produces similar effects, the term “image lag” is also used in PPD CIS when referring to the different physical mechanisms that cause poor CTI performances. In this chapter we will indicate as transfer time, the minimum TG pulse-width which allows to reach a given CTI level.

2.2 Charge transfer mechanisms in Pinned Photodiodes

Charge transfer mechanisms in CCDs have been broadly studied in the past decades [CKR72]; [Bar75]; [MMM73]; [Ban+91]; [Jan01]. Three main transfer mechanisms are accounted for the charge transfer behavior: thermal diffusion, fringing field and self-induced drift [CKR72]. If carriers encounter potential “pockets” or a potential “bumps” (referred to as “design traps” in [Jan01]) on the transfer path, thermionic emission of electrons [SN85] across this potential barrier should also be taken into account for the estimation of the CTI. Charge transport in PPDs has many similarities with CCDs, as it also involves the transfer of one carrier type (electrons and more recently holes [Ste+08]) from one potential well (the PPD buried well) to a second potential well (the FD), and eventually to a third [Yas+11]. In addition, like in CCDs, depending on the design and on process fine tuning, very different CTI performances can be obtained.

An additional mechanism that can affect charge transfer is charge loss under the TG due to the recombination of electrons with trapped holes which start to be emitted as soon as the TG is turned on. This phenomenon is discussed in section 2.2.8, where it is also shown, by
2.2. Charge transfer mechanisms in Pinned Photodiodes

means of a mathematical derivation, that the probability of electron trapping during charge transfer is extremely low and should not affect the CTI.

In this section, the different transfer mechanisms are studied and modeled for PPDs. In particular, a Matlab® function, detailed in appendix C.3 has been developed to simulate charge transfer, based on a random walk of charges. This model allows estimation of the effect of the PPD size and of other charge transport mechanisms such as charge drift, self-induced drift and thermionic emission (detailed in sections 2.2.3, 2.2.4 and 2.2.7, respectively). As discussed in section 2.2.5 the effect of the fringing is not simulated, as its contribution can be approximated to a reduction of the effective PPD length. As hole trapping and emission phenomena under the TG have not yet been adequately modeled, measured and understood, trapping mechanisms have also not been taken into account in the model. Numerical simulations are finally compared to TCAD simulations (Synopsys).

2.2.1 Charge diffusion

When considered singularly, electrons behave as random walkers, i.e. their movement consist in a series of random spatial steps that consists of a free flight interrupted by collisions. Their Brownian motion can be regarded as a strong Markov process, as it respects the Markov Property: For the prediction of the future $X(t) : t > \bar{t}$, knowing the process $X(t) : t > 0$ on the interval $[0, \bar{t}]$, is as useful as just knowing the endpoint $X(s)$. In other words at each time $\bar{t}$ the process starts afresh [MP10]. In [Rat+12] the 3D brownian motion of minority carriers is modeled as follows: after each time interval $\Delta t$, a carrier moves of a generic random step $\vec{r}_n$, uniformly distributed over a sphere of radius:

$$\Delta l = \sqrt{x^2 + y^2 + z^2} \quad (2.2)$$

If $\vec{i}, \vec{j}$ and $\vec{k}$ are the unit vectors of a Cartesian coordinate system, the random step can be expressed as:

$$\vec{r}_n = \vec{i}x_n + \vec{j}y_n + \vec{k}z_n \quad (2.3)$$

After $N$ steps (with $N = t/\Delta t$) the distance $d_{Nrw}$ from the starting point will be:

$$d_{Nrw} = \left| \sum_{n=1}^{N} \vec{r}_n \right| \quad (2.4)$$

with mean square value:

$$\langle d_{Nrw}^2 \rangle = N \times \Delta l^2 \quad (2.5)$$

If a host of electrons is considered instead, the microscopic random effects result in a macroscopic picture corresponding to a diffusion process, governed by the diffusion equation (Flick’s Law) [TN09]:

$$\frac{\partial n(x,y,z,t)}{\partial t} = D_n \nabla n^2(x,y,z,t) \quad (2.6)$$
with \( D_n \) the diffusion coefficient, usually expressed in \((\text{cm}^2/\text{s})\). In order to simulate the random walk of carriers, the relationship between the spatial and temporal steps can be calculated as follows: If we indicate as \( N_{\text{tot}} \) the total number of electrons involved in the diffusion process:

\[
N_{\text{tot}} = \int_{\mathbb{R}^3} n(x, y, z, t) \, dx \, dy \, dz \quad (2.7)
\]

and with \( d_{\text{diff}} = \sqrt{x^2 + y^2 + z^2} \) the displacement from the initial position, we can express its mean and mean square values as:

\[
\langle d_{\text{diff}} \rangle = \frac{1}{N_{\text{tot}}} \int_{\mathbb{R}^3} d_{\text{diff}} \cdot n(x, y, z, t) \, dx \, dy \, dz = 0 \quad (2.8)
\]

\[
\langle d_{\text{diff}}^2 \rangle = \frac{1}{N_{\text{tot}}} \int_{\mathbb{R}^3} d_{\text{diff}}^2 \cdot n(x, y, z, t) \, dx \, dy \, dz = 6D_n \cdot t \quad (2.9)
\]

Equating 2.5 and 2.9 \((d_{\text{W}} = d_{\text{diff}})\) yields:

\[
\frac{\Delta t}{\Delta l^2} = \frac{1}{6D_n} \quad (2.10)
\]

which gives the relationship between the spatial step and the time steps that can be used to simulate the random walk of carriers in 3D. All the expressions above can be applied also to the 1D and 2D cases. In particular 2.10 will become:

\[
\frac{\Delta t_{2D}}{\Delta l_{2D}^2} = \frac{1}{4D_n} \quad (2.11)
\]

\[
\frac{\Delta t_{1D}}{\Delta l_{1D}^2} = \frac{1}{2D_n} \quad (2.12)
\]

for the 2D and 1D cases, respectively. The same results can be obtained by means of probability calculations. The derivation in 1D can be found in Appendix C.1. An example of a 2D random walk generated in Matlab\textsuperscript{®} is shown in figure 2.2.

### 2.2.1.1 Charge diffusion in a Pinned Photodiodes

Figure 2.3a shows the simulated electrostatic potential (TCAD simulation) in a 2D PPD pixel with TG ON \((V_{\text{TG}} = 3.3 \text{ V})\) and \(V_{\text{FD}} = 3.3 \text{ V}\). Figure 2.3b and 2.3c show the electrostatic potential profile along the cuts A-A\(^\prime\) and B-B\(^\prime\), corresponding to a vertical cut at the center of the PPD and to a cut along the charge transfer path\(^2\), respectively. As can be observed, the potential along A-A\(^\prime\) is such that carriers will tend to be confined within the narrow potential well of the PPD. Along B-B\(^\prime\), the potential is almost flat, except for the region close to the TG, where the PPD potential is bent by the fringing field. As the extension of the fringing field is of the order of a 100 nm – 200 nm, its contribution to the CTI can be neglected as long as the PPD length is of the order of a few \(\mu\text{m}\). Under these assumptions, a 1D “confined”

\(^2\)Where the charge transfer path is identified as the maximum potential followed by electrons during charge transfer.
2.2. Charge transfer mechanisms in Pinned Photodiodes

2D RANDOM WALK

Figure 2.2: Example of a 2D random walk generated in matlab

diffusion process (in the x-direction) can be a good approximation for a first estimation of the transfer time.

The diffusion process has been simulated both resolving numerically the diffusion equation and implementing a Monte Carlo simulation of the random walk of a set of carriers. The diffusion coefficient for electrons has been calculated with the Einstein relation [TN09]:

$$D_n = \mu_n \frac{k_B T}{q}$$

with $\mu_n$ the electron mobility and $k_B$ the Boltzman constant. A mobility of 500 cm$^2$/(V·s) has been estimated from the TCAD simulation of a PPD implemented with typical doping implants. The corresponding diffusion coefficient is $D_n \approx 13$ cm$^2$/s. To simplify the diffusion model as much as possible, the following boundary conditions have been used for the numerical solution of the diffusion equation:

1. All carriers that reach the TG-PPD interface ($x = L_{PPD}$) are considered to be “transferred”. Thus the interface behaves as a perfect “absorbing well”:

$$u(L_2, t) = 0 \quad \forall t > 0.$$  \hspace{1cm} (2.14)

2. The potential barrier that defines the end of the PPD is considered as a perfect reflecting
Figure 2.3: (a) Electrostatic potential distribution in the PPD for $V_{\text{TG}} = +3.3$ V. The white line corresponds to the limit of the SCR. The inset shows a zoom on the PPD-TG interface region where the ON biasing of the TG induces a fringing field in the first hundreds of nm of the PPD. (b) Electrostatic potential along the y axis (cut A-A’). (c) Electrostatic potential along the charge transfer path (cut B-B’).
2.2. Charge transfer mechanisms in Pinned Photodiodes

Figure 2.4: (a) Simulated charge distribution in a 2 µm long PPD after 50 ps from the opening of the TG (\(V_{TG}\) pulsed from \(V_{LOTG}\) to \(V_{HITG}\)) considering the random walk of single electrons and the numerical solution of the diffusion equation. (b) Simulated CTI as a function of the transfer time for the same conditions as in (a).

The same boundary condition has been applied to the Monte Carlo simulation of the random walk of single electrons. In particular:

1. The transfer time corresponds to the time required for a single carrier to reach the TG-PPD interface (\(x = L_{PPD}\)).
2. A carrier that reaches the potential barrier located at \(x = 0\) "bounces" on the wall (and therefore can only move in the +\(x\) direction).

Figure 2.4 shows the charge distribution in a 2 µm PPD 50 ps after the beginning of charge transfer (opening of the TG) considering a pure diffusion regime. In the simulation it is assumed that electrons are uniformly distributed in the PPD at \(t_0\), that the \(V_{TG}\) signal rise-time is infinitely small and that self induced drift is negligible. The two simulations are in good agreement, thus each of the two approaches can be used depending on the phenomenon of interest. In particular, whereas the solution of the diffusion equation is suitable to simulate simple diffusion processes (associated with simple drift problems), the Monte Carlo approach allows easy introduction of more complex phenomena such as the effect of non constant electric fields or statistical processes such as thermionic emission. The Matlab\(^\text{®}\) code used for the calibration of the two simulations is detailed in appendix C.2.

Note that in a pure diffusion regime, the CTI only depends on the initial charge distribution in the PPD and is not affected by the absolute number of carriers. However in practice,
as discussed in the following sections, CTI performances can differ significantly depending on the initial number of electrons in the PPD. In particular:

1. At high charge density levels, the electrostatic repulsion between charges (self-induced drift) can enhance charge speed in the first instants of charge transfer [CKR72]. This mechanism is detailed in section 2.2.4.

2. There can be a potential barrier at the PPD-TG interface, due to a potential bump or a potential pocket. The PPD potential increases as charge is being transferred toward the FD. As a result, the height of the barrier, and thus the probability of carriers crossing the potential barrier (and the associated time constant) depends on the PPD charge level. This mechanism is further discussed in section 2.2.7.

### 2.2.2 Transfer time mapping

Ideally one would like to estimate the time required to transfer an electron to the FD as a function of its initial position, obtaining a mapping of the transfer time. Let us first look at the worst-case scenario: the random walk of a single electron located at the far end of the PPD with respect to the transfer gate. A Monte Carlo simulation of such a scenario has been implemented in Matlab®. The simulation consisted of 1000 repetitions of the experiment for four different PPD lengths: 1\(\mu\)m, 2\(\mu\)m, 8\(\mu\)m and 16\(\mu\)m. The histograms of the corresponding transfer times are shown in figure 2.5a. The highest probability of complete transfer corresponds to about 200 ps for a 2\(\mu\)m long photodiode, and to about 10 ns for a 16\(\mu\)m. But whereas for the shortest diode length even the slowest walkers reach the TG in less then 10 ns, for the 16\(\mu\)m diode the transfer time can be up to 600 ns. It is important to keep in mind this statistical behavior, especially when single photon resolution is targeted. In particular, one should be aware that, even if the device enables a sensitivity of a few electrons (and all photo-electrons have been successfully collected by the PPD), single electrons might reach the FD in one frame, and not in the following frame. This charge transfer uncertainty (noise) is an additional contribution with respect to the noise sources studied in [Fos03].

The CTI curves corresponding to the histograms in Fig. 2.5a are presented in Fig. 2.5b. As can be observed, increasing the PPD length results in a simple shift of the CTI curve. As shown in Fig. 2.6, the transfer time \(t_{\text{transf}}\) estimated with this simplified pure diffusion charge transfer model increases as the square of the PPD length. Note that the fact that the square fit does not pass by the origin is due to the uncertainty in the hand estimation of the transfer time. For less noisy curves, the Montecarlo simulation should be repeated considered a higher number of random walkers.

Figure 2.7 shows the CTI curves and corresponding transfer times simulated for different electron initial positions \(x_0\) in a 2\(\mu\)m PPD. As would be expected, the first electrons are transferred more rapidly as charges are released closer to the TG, whereas the transfer time improvement is more and more negligible as we approach the transfer of the last electrons. This means that statistically, if single electron resolution is targeted, the fact that a charge is
2.2. Charge transfer mechanisms in Pinned Photodiodes

Figure 2.5: (a) Histogram of the transfer time of 1000 single $e^-$ located at $x = 0$ at $t = 0$ for different PPD length and (b) corresponding CTI curves.
generated close to the TG, does not always imply a significant improvement in transfer speed. The main parameter that affects CTI performances is therefore the PPD length, and not the initial charge location.

2.2.3 Charge drift

If a small electric field $E_{\text{field}}$ is induced in the semiconductor, each electron experiences a force $-qE_{\text{field}}$ and is accelerated in the opposite direction of the electric field during the time between two collisions [Sze85]. The total motion of the carriers is then due to the combination of their thermal (random) motion and their drift velocity (before velocity saturation):

$$v_{\text{drift}} = -\mu_n E_{\text{field}}$$  \hspace{1cm} (2.16)

As charge drift is by definition “directional”, introducing an electric field to drive the charge packet toward the TG is the most intuitive solution to speed up the transfer process. The main design and process solutions that have been proposed in literature to generate such an electric field are discussed in chapter 3. This section discusses how charge drift can be accounted for in the model.

For the Montecarlo simulation of the random walk of charges, the effect of the drift field can be taken into account by simply introducing an additional positive spatial step $dx_{\text{drift}} = \mu_n E_{\text{drift}} \times dt$ for all electrons after each time step $dt$. Note that a numerical solution is of interest only if the time required to transfer charges by drift only is comparable to diffusion time constants. Otherwise, the time required for an electron to travel from a

---

3Note that in these simulations it is assumed that the PPD width does not affect charge transfer
2.2. Charge transfer mechanisms in Pinned Photodiodes

Figure 2.7: Simulated CTI for a pure diffusion regime considering an initial delta-like charge distribution located at different $x_0$ (blue curves). The PPD length is $L_{PPD} = 2\mu m$ and $x_0$ varies from $0.1L_{PPD}$ to $0.9L_{PPD}$ (where $x_0 = L_{PPD}$ corresponds to the PPD-TG interface). The red dashed curve corresponds to the CTI curve simulated considering a uniform charge distribution. As expected, the closer $x_0$ is to the end of the PPD (PPD-TG interface), the faster the first electrons arrive. However, due to the non-directionality of the diffusion process, even for $x_0 = 0.9L_{PPD}$, the last electrons reach the TG shortly before the ones that started from $x_0 = 0.1L_{PPD}$. 
point $x_0$ to a point $x_1$ can simply be calculated analytically as:

$$t_{\text{drift}} = \int_{x_0}^{x_1} \frac{dx}{\mu_n(x)E_{\text{field}}(x)}$$  \hfill (2.17)

The analytical solution of Eq. 2.17 allows easy accountability of local mobility and electric field variations. If both are constants along the PPD length, Eq. 2.17 becomes:

$$t_{\text{drift}} = \frac{x_1 - x_0}{\mu_n E_{\text{field}}(x)}$$  \hfill (2.18)

The maximum drift field that can be induced in a PPD is limited by the maximum PPD potential (i.e the pinning voltage $V_{\text{pin}}$ addressed in chapter 3), which in today’s technological processes is often of the order of 1 V or lower and is destined to reduce with further technology scaling. Figure 2.8a shows the electric field that can be induced in the PPD, as a function of the PPD length ($L_{\text{PPD}}$) assuming $\Delta V = 1V$. The figure also shows the corresponding transfer time assuming a pure drift motion. As can be observed, due to the limitations in terms of voltage drop, the transfer time increases with the square of the PPD length (like diffusion!). Therefore improving CTE performances by introducing a drift field is not a trivial solution. Note that to further increase the drift field, one can either increase $V_{\text{pin}}$ or $\mu_n$, however, there is often a trade-off between these two approaches, as $\mu_n$ is a strong function of the doping level[MSS83]. In addition, increasing $V_{\text{pin}}$ might not always be possible as its value is often finely adjusted to ensure good transfer efficiency (for a given FD reset voltage $V_{\text{DDRST}}$).

But how large should the drift field be to observe a significant enhancement of the transfer time with respect to simple diffusion? A possible approach to answer this question is to estimate the minimum “useful” electric field $E_{\text{min}}$ for which the transfer time ($t_{\text{drift}}$) that is calculated assuming a pure drift motion, is shorter than the one estimated for a pure diffusion
2.2. Charge transfer mechanisms in Pinned Photodiodes

regime. This condition can be expressed as:

\[ t_{\text{drift}} = \frac{L_{\text{PPD}}}{v_{\text{drift}}} = \frac{L_{\text{PPD}}}{\mu_n E_{\text{min}}} \leq t_{\text{diff}} \quad (2.19) \]

To simplify the expression as much as possible, we can express the diffusion time as a function of the PPD length and of a fitting parameter \( k_{\text{diff}} \) as:

\[ t_{\text{diff}} = k_{\text{diff}} L_{\text{PPD}}^2 \quad (2.20) \]

If we assume that the induced electric field is constant in the whole PPD, we can express \( E_{\text{min}} \) as a function of the corresponding potential drop across the PPD \( \Delta V_{\text{min}} \) and of the PPD length as:

\[ E_{\text{min}} = \Delta V_{\text{min}} L_{\text{PPD}} \quad (2.21) \]

Combining the previous equations finally yields:

\[ V_{\text{min}} \geq \frac{1}{\mu_n k_{\text{diff}}} \quad (2.22) \]

As it can be observed, \( V_{\text{min}} \) does not depend on the PPD length and is about 8 mV for \( \mu_n = 500 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1} \) and \( k_{\text{diff}} = 0.26 \text{s} \cdot \text{cm}^{-2} \) (where \( k_{\text{diff}} \) has been extrapolated from figure 2.6). Note that this result is obtained by considering an ideal PPD. As discussed in the following, measured transfer times can be much longer than the ones estimated by simply considering charge diffusion due to the presence of design traps.

2.2.4 Self induced drift

Charge diffusion does not take into account the fact that electrons are charged particles, that can interact with each other. In practice, electrons stored in the PPD locally modify the PPD potential, generating a self-induced drift field. Whereas this self-repulsion is usually negligible when few electrons are left in the PPD, it can accelerate transfer speed in the early phase of charge transfer. In the following, the self-induced electric field is derived based on the considerations in [KL71]; [CKR72].

The PPD local potential at given position \( x \) and at a given instant \( t \) can be estimated from the charge stored in the PPD as:

\[ \Phi(x, t) = \Phi_0 - \frac{q}{C'_{\text{PPD}}} n(x, t) \quad (2.23) \]

with \( \Phi_0 \) the local potential corresponding to a fully depleted PPD, \( n(x, t) \) the local electron density per unit area at an instant \( t \) and \( C'_{\text{PPD}} \) the PPD capacitance per unit area. For simplicity \( C'_{\text{PPD}} \) is considered constant and only charge motion along the x-axis is taken into account. The self-induced electric field, and the resulting electron flux can then be expressed as:

\[ E_{ai} = -\frac{\partial \Phi}{\partial x} = \frac{q}{C'_{\text{PPD}}} \frac{\partial n(x, t)}{\partial x} \quad (2.24) \]
As can be observed, Eq. 2.25 is strongly reminescent of the diffusion equations. In particular, we can define an equivalent diffusion coefficient $D_{\text{eff}}$ such that:

$$j_n(x, t) = D_{\text{eff}} \frac{\partial n(x, t)}{\partial x}$$

(2.26)

with:

$$D_{\text{eff}} = \frac{\mu n q}{C'_{\text{PPD}}} n(x, t)$$

(2.27)

Based on these considerations, the self-induced field enhances charge transfer speed as long as:

$$D_{\text{eff}}(t) = \frac{\mu n q}{C'_{\text{PPD}}} n_{\text{av}}(t) \geq D_{\text{diff}}$$

(2.28)

where $n_{\text{av}}$ is the average charge density in the PPD and $D_{\text{diff}} = \mu_n u_{\text{th}}$ is the diffusion coefficient (with $u_{\text{th}}$ the thermal voltage). The minimum $n_{\text{av}}$ for which charge transfer enhancement is observed is thus:

$$n_{\text{avmin}}(t) = \frac{C'_{\text{PPD}}}{\mu_n q} D_{\text{diff}} = \frac{u_{\text{th}}}{q} \cdot C'_{\text{PPD}}$$

(2.29)

For example, if we consider an area capacitance of 1.2 fF/µm² [Goi+13], self induced drift will play an important role until $n_{\text{avmin}} \approx 190e^- \mu m^{-2}$, which corresponds to about 750e⁻ in a 2 µm × 2 µm PPD.

### 2.2.5 Fringing field

Another mechanism which can enhance charge transfer speed with respect to simple diffusion is the electric field induced by the TG “on-potential” in the PPD neighboring regions. Such aiding fields are often referred to as fringing fields [CKR71]. If we assume a potential difference between the PPD and the TG channel of about 1.5 V and that the fringing field extension in the PPD is about 300 nm to 500 nm, then we can assume an average field of about $E_{\text{fr}} = 30$ kV/cm. Note that this is a rough simplification, as the fringing field changes both spatially (the closer to the TG channel, the higher $E_{\text{fr}}$) and temporally (as the PPD is being emptied, its potential increases, and $E_{\text{fr}}$ decreases). As the contribution of this additional field is better modeled by means of a TCAD simulation, in the numerical model its effect can simply be considered as a shortening of the PPD effective length of about 300 nm.

### 2.2.6 Comparison between numerical simulations and TCAD simulations

The transfer time estimated with the Montecarlo model has been compared to TCAD simulations. Figure 2.9 shows the CTI curves simulated for three different PPD lengths (2 µm, 4 µm and 8 µm). In the simulation the PPD is at equilibrium (in the dark with the TG in
2.2. Charge transfer mechanisms in Pinned Photodiodes

Figure 2.9: CTI simulated in TCAD considering a PPD length of 2 µm, 4 µm and 8 µm, respectively.

accumulation mode before charge transfer\(^4\). As can be observed, the transfer time to reach 0.001 CTI is comparable to the one estimated with the Montecarlo simulation in Fig. 2.6 for \(L_{PPD} = 8\mu m\), whereas for shorter PPD lengths, the transfer time obtained with the TCAD simulation is much smaller than estimated with the Montecarlo model. This main difference could be due to the contribution of the TG fringing field, which results, in small PPDs, in a relatively significant PPD length shortening.

2.2.7 Effect of the TG-PPD interface potential barrier on CTI

The transfer time in a 2D 4 µm long PPD has been simulated in TCAD for different \(V_{HTG}\) values (TG biasing potential during transfer) in two PPD structures (structure A and structure B shown in Fig. 2.10). Structure B corresponds to the structure simulated in section 2.2.6, whereas structure A differs from B in the overlap between the TG and the \(N_{ppd}\) implant (in particular, in B the overlap is larger, resulting in a PPD implant which comes closer to the TG surface).

The CTI curves simulated for structure A and B are shown in Fig. 2.11. The TG off-to-on transition is 100ps wide, which explains the different CTI slope observed in the first tens of ps. As can be observed, the \(V_{HTG}\) biasing voltage during charge transfer plays an important role in the CTI performances for structure A, and almost none for structure B. This behavior can be explained by the presence of a potential barrier \(\Phi_b\) at the TG-PPD interface of structure A [Fos03]; [FL07]; [Zho+11]; [Jan+14]. Because of this barrier, electrons which reach the TG-PPD interface are not instantaneously transferred to the FD, but have a given probability

\(^{4}\)This condition corresponds to a uniform initial distribution
Figure 2.10: Doping profile of the two simulated 2D PPD pixel structures (structure A on the top and structure B on the bottom).

Figure 2.11: Simulated CTI (TCAD simulation) for a 4 μm long PPD structure with and without a potential barrier (structure A and structure B, respectively) at the PPD-TG interface, considering different $V_{HTG}$ biasing voltages (2.7 V, 3.0 V; 3.3 V and 4.0 V.)
2.2. Charge transfer mechanisms in Pinned Photodiodes

$p_{\text{jump}}$ to have sufficient energy to cross the barrier by thermionic emission [Fos03]:

$$p_{\text{jump}} = \exp\left(-\Phi_b/u_{th}\right) \quad (2.30)$$

or otherwise “bounce back” and continue their random walk in the PPD. The height of $\Phi_b$ can depend on different parameters:

- It is affected by the fine tuning of doping implants under the TG. In particular if the doping profile under the TG is not accurately “laddered”, potential barrier/s or potential pockets can appear along the charge transfer path (for example, the barrier height is larger in structure A than in structure B).

- The higher $V_{HTG}$, the lower the potential barrier [Jan+14] (this is shown in Fig. 2.11 and more graphically in Fig. 2.12).

- As shown in Fig. 2.13, as charges are being transferred toward the FD, the PPD potential increases, also resulting in an increase of the potential barrier seen by the electrons (under the assumption that the high potential of the barrier is unaffected by the PPD potential). Therefore the barrier height is time dependent.

On the basis of these considerations, for a given pixel design, users can only operate on $V_{HTG}$ to reduce the barrier height. Note however, that a trade-off must be found when choosing the TG biasing potential, since as discussed in [Goi+14b], the higher $V_{HTG}$, the higher the charge spill back in the PPD due to charge partition at the end of the transfer phase (during the TG on-to-off front).

The effect of the potential barrier on charge transfer has been previously modeled in [Fos03], [FL07] and more recently in [HYT15] where a Montecarlo simulation approach, a mathematical probabilistic approach and an iterative method approach have been proposed, respectively. In [Zho+11] a TCAD approach is chosen instead. The effect of design traps on the CTE has also been discussed and simulated in [Jan+14], however no details are given on the model. Here a Montecarlo simulation approach is chosen. In particular, with respect to the simple diffusion model presented at the beginning of this section, we introduce a certain probability $p_{\text{jump}}$ for electrons to cross the potential barrier once they reach the TG-PPD interface ($x = L_{PPD}$). With respect to [Fos03] and [FL07], where it is assumed that carriers are always “ready to jump” over the barrier, in this model no electric field maintains the electron cloud close to the TG, and bounced electrons can continue their random walk in the PPD well. In addition, whereas in [Fos03] and [HYT15], the temporal dependence of the potential barrier is modeled by taking into account the increase of $\Phi_b$ as a function of the PPD charge level, a constant potential barrier is assumed here. This simplification leads to an overestimation of charge transfer inefficiency for high charge levels (for example at the beginning of charge transfer): however as the last electrons are removed from the PPD, if we assume a constant PPD capacitance $^5$, the PPD potential variation is fairly small and thus the error introduced by the constant barrier approximation can be considered negligible.

$^5$Here again, this is a simplification, as the capacitance decreases as the PPD approaches full depletion.
Chapter 2. Modeling, estimation and measurement of charge transfer

Figure 2.12: Simulated (TCAD) electrostatic potential profile at the PPD-TG interface (PPD structure A) after 10ns of the opening of the TG, considering two different $V_{HTG}$ biasing voltages (2.7 V and 4 V, respectively). As can be observed, the potential barrier height depends on $V_{HTG}$ and can be removed by over-driving the TG during charge transfer.

Figure 2.13: Simulated (TCAD simulation) electrostatic potential profile at the PPD-TG interface (PPD structure A) as a function of time. As the PPD is being emptied, we observe an increase in the potential barrier. The electrostatic potential scale is the same as in Fig. 2.12.
2.2. Charge transfer mechanisms in Pinned Photodiodes

Figure 2.14: Simulated CTI curves (Montecarlo simulation) for a 2 µm long PPD considering the effect of the potential barrier ($\Phi_b$) on charge transfer. For simplicity reasons, the barrier height is considered constant during the whole transfer (which leads to an overestimation of the transfer time for the first transferred electrons). As can be observed, as $\Phi_b$ is increased by 300 mV, the transfer time can increase of up to 2 orders of magnitude.

Figure 2.14 shows the result of the Montecarlo simulation of the transfer of 1000 single $e^-$ initially located at $x_0 = 0$ in a 2 µm long PPD, considering decreasing TG biasing potentials (which correspond to increasing potential barrier levels). As can be observed, the transfer time can increase of 2 to 3 orders of magnitude with respect to ideal diffusion when the potential barrier increases of 0.2 V – 0.3 V. As a comparison, Fig. 2.15 shows the simulated transfer time considering charges always confined in a potential pocket at the TG-PPD interface. As can be observed, if charges are maintained close to the TG (by a potential pocket or by the fringing field), the transfer time is much faster than the one estimated for the case where carriers keep diffusing after bouncing off the potential barrier.

As discussed in the introduction of this section, the PPD potential depends on the PPD charge level, and so does the potential barrier seen by electrons. Figure 2.16 shows the CTI simulated in TCAD for two different integration times $t_{int1} > t_{int2}$, corresponding to two different PPD charge levels before transfer. As can be observed, the transfer efficiency is

---

Note that in this potential pocket simulation, the transfer time that can be extrapolated for a 0 V barrier potential is about $10^{-14}$ s, which corresponds to the simulation time resolution.

The light flux and the illumination times are chosen so that for both simulations, the PPD charge is below the EFWC (refer to chapter 4).
poorer for the smaller charge level. Since reducing the PPD charge is roughly equivalent to an increase in the potential barrier (if self-repulsion phenomena are neglected), it results in a shift of the CTI curve.

2.2.8 Charge Trapping

Charge trapping phenomena under the TG are also accounted for poor CTI performances in [Jan+13]; [Bon+13a]; [Jan+15]. In particular in [Jan+13] and [Bon+13a] it is suggested that electrons can be trapped during charge transfer. Part of the trapped charge is released before the end of the TG pulse and part is released after the end of the pulse, resulting in either lag charge (if electrons are re-injected in the PPD) or in charge loss (if they are collected by the FD). These mechanisms are schematized in Fig. 2.17. The main difficulty of the quantitative estimation of charge trapping under the TG resides in the fact that the charge packet is not stored under the TG, but only “passes” under it for a very short amount of time. For this reason, whereas charge trapping has been accurately modeled in CCDs [Tom73], only qualitative analyzes can be found for PPD CIS.

As suggested in [Jan+15], another mechanism which could lead to charge loss during transfer is the recombination of electrons with holes that have been trapped under the TG during the integration phase and which are re-emitted during charge transfer (Fig. 2.18). The following sections discuss the emission and capture of carriers (section 2.2.8.1 and 2.2.8.2, respectively) associated to interface states located under the TG. In particular, it is shown, by means of analytical reasoning derived from [Tom73], that electron charge trapping is negligible in PPD CIS.
2.2. Charge transfer mechanisms in Pinned Photodiodes

Figure 2.16: Simulated (TCAD simulation) CTI for two different illumination times $t_{\text{LED1}} > t_{\text{LED2}}$ in a 4 $\mu$m long 2D PPD structure. The photon flux is the same for the two curves.

Figure 2.17: Schematic representation of electron trapping during charge transfer.

Figure 2.18: Schematic representation of electron trapping during charge transfer.
2.2.8.1 Emission of Carriers from Filled Interface States

Let us first discuss carrier emission phenomena from filled interface states. For simplicity, the derivation will refer to electron emission but the same derivation can be applied to hole emission by considering the hole quasi Fermi-level instead of the electron quasi-Fermi level and by inverting the TG biasing conditions.

Let us assume that the TG has been on for a time long enough to fill all interface states below the electron quasi-Fermi level $E_{F_{\text{on}}}$, The TG is then turned off. The velocity of electron emission to the conduction band from $n_T$ occupied traps with energy $E_T > E_F = E_{F_{\text{off}}}$ is:

$$r_e = -\frac{dn_T(E_T)}{dt} = e_n(E_T)n_T(E_T)$$  \hspace{1cm} (2.31)

where $e_n(E_T) = 1/\tau_e$ is the emission probability (with $\tau_e$ the emission time constant) and $n_T$ follows Fermi statistics:

$$n_T(E_T) = N_T(E_T)f(E_T)$$  \hspace{1cm} (2.32)

with $N_T(E_T)$ the trap density and $f(E_T)$ the probability of occupation of the state by an electron:

$$f(E_T) = \frac{1}{1 + e^{(E_T - E_F)/kT}}$$  \hspace{1cm} (2.33)

The emission probability $e(E_T)$ can be calculated using Shockley-Read-Hall equations as [SR52]; [Tom73]:

$$e_n(E_T) = \sigma_n(E_T)v_{\text{th}}N_C e^{E_T - E_C}/kT$$  \hspace{1cm} (2.34)

where $\sigma_n(E_T)$ is the electron capture cross-section of the interface state, $N_C$ is the effective density of states in the conduction band (or in the valence band if holes are considered) and $v_{\text{th}}$ is the mean thermal velocity of charge carriers:

$$v_{\text{th}} = \sqrt{\frac{3kT}{m}} \approx 1.161 \times 10^5\text{cm/s at room temperature.}$$  \hspace{1cm} (2.35)

Based on the previous expressions, the time dependence of the occupancy of traps within an energy range $dE_T$ around $E_T$ can be calculated as:

$$n_T(E_T,t) = N_T(E_T)f(E_T)e^{-e_n(E_T)t}dE_T$$  \hspace{1cm} (2.36)

Therefore the emission time constant is simply:

$$\tau_e = \frac{1}{e_n} = \frac{1}{\sigma_n(E_T)v_{\text{th}}N_C e^{E_T - E_C}/kT}$$  \hspace{1cm} (2.37)

Figure 2.19 shows the emission time constant $\tau_e = 1/e_n$ calculated with the capture cross-sections in [Tom73] following Eq. 2.34 (room temperature). Note that traps which are closer

---

8The product $N_C e^{E_T - E_C}/kT$ corresponds to the number of electrons in the conduction band for the case when the Fermi level falls at $E_T$. 

42
2.2. Charge transfer mechanisms in Pinned Photodiodes

Figure 2.19: Trap emission time constant $\tau_e = 1/e_n$ as a function of the trap energy level.

to the conduction band will tend to empty first, followed by lower energy traps. Deep trap levels (few KT from the mid-gap energy) tend to be involved in recombination processes rather than re-emitting the electrons to the conduction band.

The total number of emitted carriers after a time $t$ is given by the integration of empty traps over the energy range $E_g/2 - E_C$. For simplicity we will now refer to $\xi = E_C - E_T$ in our calculations.

$$N(t) = \int_0^{E_g/2} N_T(\xi) f(\xi) \left[ 1 - e^{-e_n(\xi)t} \right] d(\xi)$$

which combined with Eq. 2.34 gives:

$$N(t) = \int_0^{E_g/2} N_T(\xi) f(\xi) \left[ 1 - e^{-t\sigma_n(\xi)\bar{v}N_C e^{-\xi/kT}} \right] d(\xi)$$

(2.39)

If both $\sigma_n(\xi)$ and $N_T(\xi)$ are constant across the bandgap, and the Fermi level is close to the conduction band, Eq. 2.39 can be simplified as [Str72] 

$$N(t) = N_T kT \ln(\sigma_n \bar{v} N_C t)$$

(2.40)

In practice as discussed in [Tom73], this approximation may lead to an underestimation of the number of emitted carriers.

---

43
Chapter 2. Modeling, estimation and measurement of charge transfer

2.2.8.2 Capture of carriers during charge transfer

Let us now estimate the probability of electrons being trapped by interface states during charge transfer. The lifetime $\tau_t$ of a trap with capture cross-section $\sigma$ in the presence of a static surface charge density $c_s$ with mean thermal velocity $v_{th}$ is given by:

$$\tau_t = \frac{1}{\sigma v_{th} c_s} \quad (2.41)$$

where $c_s$ can be expressed as a function of the normal electric field $E_s$ at the interface and of the total free carrier density $N_f$ in the inversion layer:

$$c_s = \frac{q}{kT} E_s N_f \quad (2.42)$$

which gives:

$$\tau_t = \frac{kT}{\sigma v_{th} q E_s N_f} \quad (2.43)$$

The probability $p_{trap}$ of a trap capturing a carrier during charge transfer is given by

$$p_{trap} = 1 - e^{-\Delta t / \tau_t} \quad (2.44)$$

where $\Delta t$ is the time required to transfer the charge packet.

The density of charge trapped during charge transfer can finally be estimated as:

$$Q_{trap} = c_s \times p_{trap} \times N_T L_{TG} W_{TG} \quad (2.45)$$

where $L_{TG}$ and $W_{TG}$ are the TG width and TG length respectively.

To evaluate numerically this CTI contribution, one needs first to estimate the charge density $N_f$ during transfer, the time $\Delta t$ required to transfer the charge packet and the density of interface state $N_T$. Let’s say for example that we want to transfer $N_{e^-} = 10ke^-$. We assume a TG size of $5 \mu m \times 1\mu m$, a density of states $N_T = 2 \times 10^{10} \text{ cm}^2/\text{eV}$, an electric field $E_s = 2 \times 10^4 \text{ V/cm}$ normal to the TG interface and a capture cross-section of about $\sigma = 1 \times 10^{-15} \text{ cm}^2$ (which is the default value in Sentaurus). By applying the approximation proposed in [Tom73], the average charge density during transfer can be estimated as:

$$N_f = \frac{N_{e^-}}{W_{TG} v_f \Delta t} \quad (2.46)$$

where $v_f$ is the average charge speed in the TG channel ($v_f = 5 \times 10^6 \text{cm/s}$ here). The resulting charge density is about $N_f = 4 \times 10^7 \text{ e}^-/\text{cm}^2$ (or $N_f = 0.4 \text{ e}^-/\mu \text{m}^2$), which gives a trapping constant of $\tau_t \approx 260 \mu s$ and a trapping probability of almost zero. These results are based on strong simplifying hypotheses (such as a constant capture cross-section or the approximation of an uniform charge transfer), however they are not surprising if we compare

\[\text{[Tom73]}\] Which consists in modeling the transfer process as a uniform transfer of charge across the TG.
2.2. Charge transfer mechanisms in Pinned Photodiodes

the typical full well capacity per unit area of a PPD (about a few ke−/µm²), to the one of a
CCD (where tens of ke−/µm² are usually involved). Furthermore the transfer path in a PPD
is of the order of the µm (compared to several µm in CCDs).

Whereas the probability of observing electron trapping during charge transfer is close to
zero, this is not case for the trapping of holes during the integration time, which is often of
the order of several ms. As the emission rate only depend on the density of full traps and on
the traps capture cross-section, as soon as the TG is turned on, holes start to be released by
the interface states and can recombine with electrons, resulting in charge loss. This charge
loss will mainly depend on the V_{LOTG} biasing voltage, as the more the TG is accumulated,
the higher the number of trap energy levels are involved.

Note that the effect of charge trapping is very difficult to separate from the other physical
mechanisms affecting the CTI which have been discussed in this chapter, as they all more or
less depend on the charge level and on the TG biasing conditions. However a possible way to
verify the presence (or not) of charge trapping under the TG is to perform CTI measurements
varying V_{LOTG} and on PPD pixels with different PPD lengths (as the amount of charge lost
by recombination should be proportional to L_{TG}).

2.2.9 Let’s summarize …

Table 2.1 summarizes the physical mechanisms affecting PPD CIS CTE performances, which
have been addressed in this work. For each mechanism, the table indicates the design and/or
operation parameters which can be adjusted to modify the CTE, what effect we expect to
observe by varying these parameters and, when possible, the measurements that have been
performed in this work (and which are presented in the following sections).

<table>
<thead>
<tr>
<th>Mechanism</th>
<th>Parameter</th>
<th>Expected behavior</th>
<th>In this work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Charge diffusion</td>
<td>L_{PPD}</td>
<td>t_{transf}×L_{PPD}²</td>
<td>Meas. for L_{PPD}=2μm, 4μm, 8μm, 16μm</td>
</tr>
<tr>
<td>Charge Drift</td>
<td>L_{PPD}</td>
<td>t_{transf}×L_{PPD}² for fixed ∆V_{PPD}</td>
<td>Simulation</td>
</tr>
<tr>
<td></td>
<td>∆V_{PPD}</td>
<td>t_{transf}×∆V_{PPD} for fixed L_{PPD}</td>
<td>Simulation</td>
</tr>
<tr>
<td>Thermionic emission</td>
<td>V_{HTG}</td>
<td>t_{transf} &gt;&gt; when V_{HTG} &gt;&gt;</td>
<td>Meas. for V_{HTG}=2.9V to 3.7V</td>
</tr>
<tr>
<td></td>
<td>Q_{PPD}</td>
<td>t_{transf} &lt;&lt;= when Q_{PPD} &gt;&gt;</td>
<td>Meas. for 2 Q_{PPD} levels</td>
</tr>
<tr>
<td>Fringing field</td>
<td>V_{HTG}</td>
<td>t_{transf} &lt;&lt;= when V_{TG} &gt;&gt;</td>
<td>Not measured</td>
</tr>
<tr>
<td>Self Drift</td>
<td>Initial Q_{PPD}</td>
<td>&gt;&gt; of initial transfer speed</td>
<td>Analytical development</td>
</tr>
<tr>
<td>e⁻ recombination with trapped h⁺</td>
<td>L_{TG}</td>
<td>Q_{out} &lt;&lt;= when L_{TG}&gt;&gt;</td>
<td>Analytical development</td>
</tr>
</tbody>
</table>

Table 2.1: Table summarizing the mechanisms affecting charge transfer in PPD CIS and the
parameters that can be varied to improve the transfer time.
Chapter 2. Modeling, estimation and measurement of charge transfer

2.3 Experimental Measurements

This section presents experimental results on the transfer time for PPD lengths up to 32\(\mu m\). Transfer time measurements are based on dedicated PPD pixels which present an additional gate, referred here as Storage Gate (SG), which allow experimental reproduction of a worst-case scenario when charges are generated at the far-end of the PPD with respect to the TG. Whereas simple rectangular PPDs are tested here, these structures are well suited to compare transfer efficiency performances in different PPD geometries.

2.3.1 When do we observe image lag?

To define the experimental set-up, it is important to first identify when it is possible to observe image lag. In fact, depending on the operation conditions, measurements can be unaffected by image lag even for detectors which present very poor CTE, or for very small TG pulse widths. As shown in the following, image lag can be observed only in pulsed-light conditions or by introducing an additional dump phase after charge transfer\(^{11}\).

2.3.1.1 Charging lag and effect of lag in stationary illumination conditions

Figure 2.20 shows a schematic representation of the effect of charging lag phenomena with and without a dump phase during the readout of the detector. Let us assume that the device is in the dark and that light is suddenly turned on at the instant \(t = t_0\) (Fig. 2.20a). A timing diagram with no dump phase is considered at first (Fig. 2.20d). As shown in Fig. 2.20b, a certain amount of residual charge is left in the PPD after the first charge transfer. After the integration time of the second image, the amount of charge stored in the PPD will be equal to the number of collected photo-electrons plus the lag electrons of the previous image. If we assume that the CTI does not depend on the charge level, more carriers will be transferred during the second transfer with respect to the first transfer. The output signal will keep increasing in the successive frames until the number of photo-electrons collected in the PPD is equal to the charge transferred to the FD. This condition corresponds to stationary illumination conditions, where the measured output signal is not affected by the CTE of the detector and for which an average constant residual charge is always left in the PPD after charge transfer (this lag charge depends on the signal level and on the CTI of the detector). The output transient following the light step is referred to as “charging lag” [Jan01]. Let’s now consider the response to the light step when using a timing diagram which includes a dump phase (Fig. 2.20c). As shown in Fig. 2.20c, the condition at which the output charge equals to the input signal is never reached, thus the output signal is always affected by the CTE of the detector, even in stationary illumination conditions. This behavior becomes evident

\(^{11}\)Where the dump phase consists in a second TG pulse following the sampling of the signal, which is often used in commercial detectors to dump the residual PPD charge.
2.3. Experimental Measurements

during the measurement of the Electro-Optical Transfer Function (EOTF)\textsuperscript{12}, which can show a significant non-linearity at small signal levels if the detector presents a poor CTE when operating the detector with a dump phase (Fig. 2.21).

2.3.1.2 Discharging lag

If we now turn off the light at the instant $t = t_1$, the charge stored in the PPD is equal to the thermally generated charge plus the residual charge corresponding to the previous stationary illumination level. As a consequence, the output signal of the first image acquired after the light step is larger than the dark signal. In the following frames the amount of residual charge tends to zero and the output signal tends to the dark signal. In theory, in analogy to the stationary illumination condition, the residual PPD charge in the dark depends on the level of the dark current, however as the latter is usually very small and remains more or less constant from one frame to the other, this residual charge should have no impact on the output signal.

2.3.2 Device under test and experimental set-up

A 1D $1 \times 56$ pixels array has been designed in a commercially available 0.18 $\mu$m PPD-CIS technology. The matrix consists of seven sub-arrays of $1 \times 8$ Storage Gate (SG) PPD. Each sub-array corresponds to a different PPD size. Figure 2.22 shows the cross-section and top view of a SG PPD pixel. With respect to standard 4T PPD pixels, SG pixels present an additional gate (the SG), located at the opposite side of the PPD, which is used to store carriers during charge integration. All PPDs are 5 $\mu$m wide (to minimize geometrical effects on the width direction), whereas the PPD length varies from 2 $\mu$m to 32 $\mu$m. For all pixels, the SG is 5 $\mu$m wide (same width of the PPD) and 0.3 $\mu$m long, whereas the TG is 5 $\mu$m wide and 0.7 $\mu$m long. The CVF is about 10 $\mu$V/e$^-$. The schematic architecture of the experimental set-up is shown in Fig. 2.23. A FPGA (Field Programmable Gate Array) generates the pixel addresses to drive the address decoder (X<0:5>) and two additional signals to trigger the pulse generators which generate the driving signals for the TG, the SG, the RST and the LED (which is pulsed after each image). The output is digitized with a 14bits Analog to Digital Converter (ADC) and then acquired at a rate of 2Msamples/s. The timing diagram and the measurement principle are detailed in the sections below.

Note that none of the array driving signals is decoded so that their pulse amplitude, pulse width and pulse fall and rise times can all be adjusted. The pixel array is mounted in a PGA-84 package. Part of the driving signals are in common with the driving signals of the other pixel arrays tested in this work. Pixel are addressed by means of a dedicated 6 bits 3.3V decoder. For more details on the driving electronics and on the readout electronics refer to appendix D.

\textsuperscript{12}Where the EOTF corresponds to the measured mean output signal as a function of the number of impinging photons.
Figure 2.20: Schematic representation of charging lag phenomena (b) without and (c) with an additional dump phase after charge transfer in response to an illumination step (a). Green electrons correspond to photogenerated electrons, orange electrons to lag electrons and blue electrons to transferred electrons. The timing diagram without and with dump phase are shown in figures (d) and (e), respectively. $V_{\text{ref}}$ and $V_{\text{sig}}$ correspond to the sampling of the reference and the signal, respectively.
2.3. Experimental Measurements

Figure 2.21: Schematic drawing of the Electro-Optical Transfer Function measured with (blue) and without (red) introducing a dump phase after the sampling of the signal.

Figure 2.22: (a) Cross-section view of a storage gate pixel structure. Top view of a storage gate pixel (b).
2.3.3 Timing diagram

The implemented timing diagram (shown in Fig. 2.24) allows experimental reproduction of an initial delta-like charge distribution located at the far end of the PPD. In the charge integration phase (during which electrons are stored under the SG), the SG is on ($V_{SG} = 3.3$ V). Both the RST transistor and the TG are pulsed on for about 100 $\mu$s ($V_{RST} = 3.3$ V and $V_{TG} = V_{HTG}$) to completely empty the PPD and to reset the FD potential. The reference ($V_{ref}$) is sampled, and the TG is turned on again for 90 $\mu$s. The TG and SG are pulsed off ($V_{SG} = -0.4$ V and $V_{TG} = V_{LOTG}$) with a relative time delay $\Delta t$ between the TG and SG falling edges, which corresponds to the interval of time during which charges can be transferred from the far end of the PPD (PPD-SH interface) to the FD. Finally the signal ($V_{sig}$) is sampled and a new integration phase can start. To modulate the charge stored under the SG, the experimental set-up also includes a LED ($\lambda_{LED} = 540$ nm), which is pulsed on ($V_{LED} = 5$ V) during charge integration. The LED pulse width ($t_{hiLED}$) is adjusted depending on the targeted signal level. The difference $V_{out} = V_{ref} - V_{sig}$ is performed directly on the PCB by means of an instrumental amplifier (For the purpose of clarity, this block is not represented on the schematic in Fig. 2.23).

Note that $t_{hitG}$ must be chosen long enough so that the maximum delay $\Delta t_{max}$ (here 90 $\mu$s) between the falling edges of the SG and TG signals is sufficiently long to ensure that

---

13As during charge transfer, the SG is in accumulation mode, the latter acts as a reflection wall on which charge “bounce” as if they had reached the end-wall in a standard PPD-pixel.
2.3. Experimental Measurements

Figure 2.24: Timing diagram for the estimation of transfer time on pulsed storage gate pixels.

all released charges have been transferred. The CTI corresponding to a given delay $\Delta t$ is calculated here as:

$$CTI = 1 - \frac{V_{\text{out}}(\Delta t)}{V_{\text{out,max}}}(2.47)$$

where $V_{\text{out,max}}$ is the output voltage measured for $\Delta t = \Delta t_{\text{max}}$ and $V_{\text{HTG}} = 3.5$ V.

2.3.4 Experimental results

Figures 2.25 and 2.26 show the CTI measured for increasing PPD lengths and increasing $V_{\text{HTG}}$ biasing voltages (where CTI values are presented in linear and logarithmic scales, respectively). Data has been averaged on 8 pixels per PPD length over 400 acquisitions.

As expected from simulations, when $L_{\text{PPD}}$ is reduced, we observe a shift of the curve (in linear scale) toward lower transfer times. The plateau observed by looking at the CTI in logarithmic scale is most probably due to the resolution of the test set-up. We can also observe that the $V_{\text{HTG}}$ potential strongly affects the CTI, therefore, even at typical TG biasing potentials (such as $V_{\text{HTG}} = 3.3$ V), charge transfer is limited by the potential barrier at the PPD-TG interface (at least for the tested technology). The larger CTI shift as a

---

14 Since for $V_{\text{HTG}} = 3.5$ V almost 100% CTE is reached for all tested pixels after 90$\mu$s.
15] The CTI is presented in both scales as together they allow to observe CTI variations at both the beginning and the end of charge transfer.
16 Note that due to process variations and the poor statistics, significant variations in the CVF value and in the SG storage capacity are observed across the array. As a result, the amount of transferred charge is not identical for all the pixels of the array and the minimum measurable CTI can vary for the different curves.
Figure 2.25: CTI measured as a function of the delay between the falling edges of the SG and TG signals with the timing diagram in Fig. 2.24 for different PPD lengths and increasing $V_{HITG}$ biasing voltage (with CTI values presented in linear scale).

Figure 2.26: CTI measured as a function of the delay between the falling edges of the SG and TG signals with the timing diagram in Fig. 2.24 for different PPD lengths and increasing $V_{HITG}$ biasing voltage (with CTI values presented in logarithmic scale).
2.4 Conclusion

Figure 2.27: Charge transfer time corresponding to a 0.01 CTI (red) and 0.1 CTI (blue) measured as a function of the PPD lengths with $V_{HTG} = 3.3$ and $V_{LTG} = 0$.

function of $V_{HTG}$ observed for long PPDs with respect to short PPDs can be attributed to two different phenomena:

- Firstly, PPDs with dimensions of the order of a few $\mu$m or lower have a smaller pinning voltage (refer to chapter 3), which results in a smaller potential barrier.
- Moreover, since for a given amount of injected charge, short PPDs are more full (relatively speaking) than long PPDs, the decrease of the PPD potential due to the presence of carriers in the potential well (which results in a smaller potential barrier) is much larger in small pixels.

Figure 2.27 shows the transfer time corresponding to a 0.01 CTI and 0.1 CTI extrapolated from the CTI curve for $V_{HTG} = 3.3$ V in Fig. 2.26. As predicted by numerical simulations, the transfer time increases as the square root of the PPD length. Figure 2.28 shows the CTI measured for different PPD lengths for two different LED pulse widths. The LED intensity and pulse width are chosen so that the stored charge is well below the PPD EFWC. As expected from TCAD simulations, reducing the initial charge level before transfer results in a shift of the CTI curve, as carriers involved in the first part of the transfer transient experience a smaller potential barrier if the signal level is increased.

2.4 Conclusion

This chapter detailed the different charge transfer mechanisms that should be taken into account during the design of PPD CIS pixels. Understanding these mechanisms is particularly critical in for the design of high temporal resolution PPD CIS detectors, where the maximum sampling frequency is limited by the time required to transfer the charge packet from the
Figure 2.28: Charge transfer inefficiency (plotted in a linear scale) measured as a function of the delay between the falling edges of the SG and TG signals for increasing PPD lengths for two different initial charge levels ($Q_{PPD2} > Q_{PPD1}$).

PPD to the FD. Charge transfer has been studied based on the Montecarlo simulation of the random walk of single carriers. The model developed in this work simulates both the drift and the diffusion of carriers within the PPD. The model takes into account charge confinement within the PPD, but also self-repulsion phenomena and the effect of design traps at the PPD-TG interface. Numerical simulations have been compared to 2D TCAD simulations and to experimental measurements performed on dedicated pulsed Storage Gate (SG) pixels. Assessing CTI performances with SG pixels to test different PPD sizes and geometry has many advantages, in particular:

- The amount of transferred charge only depends on the SG size and not on the PPD size.
- The charge initial distribution is the same, whatever the PPD geometry.
- They allow experimental reproduction of a delta-like initial charge distribution located at the far end of the PPD, which represents a worst case scenario when photoelectrons are generated at the farthest from the TG.

Due to the statistical nature of charge diffusion, “mapping” the transfer time as a function of a carrier initial location is not trivial, as the electron arrival time is not deterministic. For this reason, the transfer time is defined in this work as the time required to reach a given CTI level. Numerical simulations showed that the transfer time increases as the square root of the PPD length. TCAD simulations have confirmed this behavior on PPD lengths of 8 µm. However, if the PPD length is further reduced, the measured transfer time starts to deviate from the theoretical curve (faster transfer of the first electrons observed in Fig. 2.26). This behavior could be explained by the fact that, in short PPDs, the extension of the TG fringing
2.4. Conclusion

field is large enough for not being negligible any more with respect to the PPD length. It has been shown that, for the tested technology, charge transfer is always affected by the potential barrier at the TG-PPD interface, even for long PPD lengths. Increasing the $V_{HTG}$ biasing voltage can be a valid solution to improve CTI performances, however a trade-off must be found between the barrier height and charge partition phenomena. Based on this analysis, introducing even a small electric field to drive the charge packet close to the TG can strongly enhance the transfer speed, as electrons are kept close to the TG and are always “ready to jump” across the barrier. Another approach to the problem, which can be applied when the detector is used in integration mode, consists in creating a potential well close to the TG (for example by using a different pinning implant).

In this work, only rectangular PPDs have been tested, however this method can help comparing CTI performances for more exotic PPD shapes, for different biasing voltages and different charge levels.
Definition, estimation and modulation of the pinning voltage

Temporal resolution performances in PPD CIS are significantly affected by both the technology and design of the pixel design. In particular, as addressed in chapter 2, design traps located at the PPD-TG interface (such as potential barriers or potential pockets), can lead to a significant worsening of the transfer time. To minimize these effects, both the TG threshold voltage and the $V_{DDRST}$ power supply must be carefully adjusted as a function of the PPD maximum potential, often referred to as pinning voltage ($V_{pin}$). The optimum value of $V_{pin}$ strongly depends on the requirements of the target application. For example, designing a PPD with a small $V_{pin}$, often results in better CTE performances. On the other hand, as discussed in chapter 4, a larger $V_{pin}$ results in a higher PPD Equilibrium Full Well Capacity (EFWC). Therefore, during the design of the pixel, a trade-off must be found between dynamic range and speed performances.

Given the importance of the pinning voltage on the final performances of the device, it is of primary important to be able to reliably measure its value to monitor the effect of experimental conditions and design/process variations. The first part of this chapter focuses on the definition and physical modeling of $V_{pin}$ and on the comparison between $V_{pin}$ estimation methods. It is shown that the commonly accepted theoretical definition of this parameter does not correspond to the physical parameter which is measured with the existing methods. The temperature behavior of the pinning voltage is also investigated based on an analytical model and on experimental measurements. To enhance charge transfer speed, the most intuitive solution is to induce a drift field in the PPD by means of a spatial modulation of the PPD potential. Two potential modulation methods, based on the generation of a static and of a dynamic field, respectively, are discussed in the second part of this chapter. The physical principle of each method is introduced, modeled and discussed by means of TCAD simulations and experimental measurements.

### 3.1 Definition of the pinning voltage

The pinning voltage is commonly defined as the maximum deviation of the electron quasi-Fermi potential $\Delta E_{FM_{\text{max}}}$ [Gro67] between equilibrium ($V_{PPD} = 0$ V) and fully empty conditions (the PPD is fully empty of minority carriers)[KF05]. In TCAD simulations however,
Figure 3.1: Schematic representation of a PPD pixel at equilibrium (a) and after charge transfer (b). The dashed lines correspond to the extension of the space charge region. The corresponding schematic potential diagrams along the cut A-A’ are shown in (c) and (d), respectively. The schematic energy band diagrams along the cut B-B’ at equilibrium (e) and at full depletion conditions (f) are shown in (a) and (b), respectively.
3.2. Modeling of the pinning voltage

The pinning voltage is often retrieved as the maximum variation of the electrostatic potential $\Delta \Phi_{\text{max}}$ [FH14]; [Mic+11] (maximum bending of the conduction band). As shown in the band diagrams in Fig. 3.1e and 3.1f, these two parameters ($\Delta E_{\text{fn max}}$ and $\Delta \Phi_{\text{max}}$) represent two very different physical parameters which can differ, as discussed later in this section, of several hundreds of mV.

To gain a better insight on how $V_{\text{PPD}}$ and the PPD charge ($Q_{\text{PPD}}$) change as a function of the biasing potential applied to the PPD, a possible approach is to simulate the structure in Fig. 3.2a, which corresponds to a PPD biased by means of two n+ implants located at both sides of the PPD. With respect to a full PPD pixel (PPD+TG+FD) this structure has the advantage of allowing a symmetrical biasing of the PPD and guarantees that the potential applied to the PPD is not affected by the non-idealities of the TG. Note that the structure in Fig. 3.2a corresponds to a Junction Field Effect Transistor (JFET) implemented with typical PPD implants (as the channel of JFETs is also formed by a double p-n-p junction). As addressed in this work, such JFET test structures represent a useful experimental tool to gain a better insight into the PPD physics and to optimize PPD technological processes. For this reason, $V_{\text{pin}}$ is sometimes referred to as “pinch-off voltage” in analogy to the pinch-off voltage ($V_p$) of JFETs [Nea11].

Figure 3.2b shows the PPD maximum electrostatic potential $\Phi$, maximum electron quasi-Fermi level $E_{\text{fn}}$ and maximum electron density $Q_{\text{PPD}}$ (plotted in linear and logarithmic scales) as a function of the injection potential ($V_{\text{inj}}$) applied to the structure in Fig. 3.2a. At small injection potentials, both $\Phi$ and $E_{\text{fn}}$ increase as $V_{\text{inj}}$ is increased and we observe a linear drop of $Q_{\text{PPD}}$. However, when the PPD reaches its maximum electrostatic potential (i.e. when $V_{\text{inj}} = \Delta \Phi_{\text{max}}$), the channel is not yet empty, as there is a thermionic emission of carriers from the n+ regions toward the PPD channel. The logarithmic drop of $Q_{\text{PPD}}$ in this region ($V_{\text{inj}} > \Delta \Phi_{\text{max}}$) can be explained by the fact that the probability for a charge to cross the barrier is an exponential function of the barrier height [TN09]. Eventually, at $V_{\text{inj}} = \Delta E_{\text{fn max}}$ the PPD is empty of charges ($Q_{\text{PPD}}$ plateau).

The $\Delta E_{\text{fn max}}$ definition is suitable when referring to the condition at which all charges have been removed from the PPD (because the electron density is a function $E_{\text{fn}}$ [Gro67]). However, as discussed in section 3.3.2, $\Delta E_{\text{fn max}}$ does not truly represent a “PPD parameter”, as it corresponds to the minimum TG channel potential that must be applied to completely empty the PPD. On the other hand $\Delta \Phi_{\text{max}}$ mainly depends on the PPD doping profiles $^1$ and corresponds to the PPD potential floor, which is usually the parameter that CIS manufacturers wish to monitor during the design of the detector. For this reason, in the following, when referring to $V_{\text{pin}}$ we will be referring to $\Delta \Phi_{\text{max}}$.

3.2 Modeling of the pinning voltage

A simple 1D approximation of $V_{\text{pin}}$ can be obtained by making the following assumptions:

$^1$As discussed in section 3.4, $\Delta \Phi_{\text{max}}$ is also a strong function of temperature.
Figure 3.2: (a) The simulated structure (TCAD) is a 3D partially pinned PPD biased by means of two n+ implants located at both side of the PPD channel. (b) PPD maximum electrostatic potential $\Phi$, maximum $E_{fn}$ and maximum electron density $Q_{PPD}$ (plotted in linear and logarithmic scales) as a function of the injection potential applied to the PPD by means of two n+ implants. Three main working regions can be identified: a linear region ($V_{inj} < \Delta \Phi_{\text{max}}$), a logarithmic region ($E_{fn\text{max}} > V_{inj} > \Delta \Phi_{\text{max}}$) and a full depletion region ($V_{inj} > E_{fn\text{max}}$). The corresponding potential diagrams are schematized in (c).
3.3 Overview on pinning voltage estimation methods

- The effect of the lateral depletion region (associated to the P\textsubscript{well}-N\textsubscript{PPD} junction) on the extension of the vertical depletion region, is negligible. This hypothesis is usually verified as long as the PPD length and width are larger than a few \( \mu \text{m} \).

- The PPD doping profile is such that the PPD can be approximated to a single abrupt p-n junction [TN09], which corresponds to the upper P\textsubscript{pin}-N\textsubscript{PPD} junction.

Under these hypotheses, \( V_{\text{pin}} \) can simply be expressed as the potential that must be applied to the upper P\textsubscript{pin}-N\textsubscript{PPD} junction to fully deplete the PPD buried channel of depth \( d_{\text{PPD}} \):

\[
V_{\text{pin}} = \frac{qN_{\text{PPD}}d_{\text{PPD}}^2}{2\varepsilon_{\text{Si}}} - V_{\text{bi}} \tag{3.1}
\]

where \( q \) is the elementary charge, \( \varepsilon_{\text{Si}} \) the Si permittivity and \( V_{\text{bi}} \) the upper junction built-in voltage [TN09]. Note that more detailed analytical estimations could be obtained by considering both the upper and lower junctions [Cao+14] and a non uniform doping profile for the buried channel implant. Moreover, as in practice the pinning voltage is strongly affected by the 3D potential distribution, additional geometrical parameters should be introduced in Eq. 3.1 to take into account geometrical effects\(^2\). However, this model has the advantage of being simple, and allows easy prediction of the effect of many design parameters (such as the doping levels) and of experimental conditions (such as the working temperature) on \( V_{\text{pin}} \).

3.3 Overview on pinning voltage estimation methods

Pinning voltage measurements are often used in the industry to monitor production lines and for the optimization and development of technological processes. As none of the existing \( V_{\text{pin}} \) estimation methods has yet been officially identified as a golden standard, each manufacturer measures the pinning voltage with custom developed techniques, which can be based on very different physical principles. In particular, in the CIS community, \( V_{\text{pin}} \) is estimated based on:

1. Measurements performed on isolated test structures or on test structures arrays. These methods can be divided into:
   - JFET-based extraction methods [SD82]; [PU09]; [Cou09]; [Hyn81], where \( V_{\text{pin}} \) is extracted as the pinch-off voltage \( V_p \) [Nea11] of JFET test structures implemented with typical PPD implants (PPD-JFET structure and TG-PPD-JFET structure in Fig.3.3a and Fig.3.3b, respectively).
   - Capacitance measurements [LRF11].

2. In-pixel measurements [TBT12]; [Goi+14b]; [XGT15]; [Cha+14], where \( V_{\text{pin}} \) is measured directly on full PPD pixels arrays.

\(^2\)In [PU09] an analytical expression of the effect of size on \( V_{\text{pin}} \) is proposed, however the expression involves two experimental fitting parameters which are not related to specific physical parameters, and therefore it is not suitable for a quick hand estimation of \( V_{\text{pin}} \).
Figure 3.3: (a) Schematic drawing of a PPD-JFET structure implemented with typical PPD implants. (b) Schematic drawing of a TG-PPD-JFET structure implemented with typical PPD implants.

These techniques are discussed in the following sections.

3.3.1 Test structure methods

This section reviews some of the most commonly used methods to estimate $V_{\text{pin}}$ on isolated test structures (or test structure arrays). In particular, the physical principle of the different methods is discussed based on analytical models and TCAD simulations. It is shown that some methods are more reliable than other methods for the estimation of the absolute value of $V_{\text{pin}}$.

3.3.1.1 The Square root method

The square root (SQRT) method [SD82] (Fig. 3.4) is a well established JFET pinch-off voltage ($V_p$) characterization technique. It is based on the measurement of the JFET drain to source current equation at saturation [Nea11]:

$$I_{\text{DS}} = I_{\text{DSS}} \left(1 - \frac{V_{\text{SG}}}{V_p}\right)^2$$  \hspace{1cm} (3.2)

where $V_{\text{SG}}$ is the JFET source-to-gate biasing voltage (with $V_G$ the substrate biasing voltage and $V_{\text{SG}} > 0$, $I_{\text{DS}}$ is the JFET saturation drain-to-source current, and $I_{\text{DSS}}$ is the $I_{\text{DS}}$ saturation current measured for $V_{\text{SG}} = 0$. Note that for the purpose of clarity, $V_p$ is defined here as a positive quantity (whereas in [Nea11] it is defined as a negative quantity). Figure 3.4 shows the experimental extraction of $V_p$ on a JFET with $W_{\text{JFET}} = 20 \mu$m, $V_p$ is estimated as the intersection of the tangent to the square root characteristic with the x-axis. The linear fitting is performed at small $V_{\text{SG}}$ biasing voltages (corresponding to high current values), thus the measurement is not affected by the resolution of the experimental set-up. Note however, that since a large voltage (2 V) is applied between source and drain, this method
3.3. Overview on pinning voltage estimation methods

Figure 3.4: Square root of the drain to source current ($I_{DS}$) as a function of the gate to source biasing voltage $V_{SG}$ measured on a PPD-JFET structure (with a constant drain to source biasing voltage $V_{DS} = 2\, \text{V}$). In the square root (SQRT) extraction method[SD82] the pinch-off voltage $V_p$ of the JFET can be extracted as the X-intercept of the tangent to $\sqrt{I_{DS}}$ at small $V_{SG}$. The tested device is a PPD-JFET with $W_{JFET}/L_{JFET} = 20\, \mu\text{m}/20\, \mu\text{m}$ (foundry A).

should be used only for long PPD-JFET structures to avoid the drain potential affecting the potential at the source (equivalent of short channel effects in MOS transistor [TN09]). This can be considered as a strong limitation to this method, as designers aim at estimating $V_{pin}$ in structures which are as close as possible to real pixels. However, since standard JFET structures usually have n+ implants at both sides of the PPD, none of the JFET methods discussed in this work truly allows to observe the effect of the PPD length on $V_{pin}$. Therefore only $V_{pin}$ variations with the PPD width [Tak+10] can be monitored with JFET structures.

To respect design rules and to approach as much as possible in-pixel conditions, PPD-JFET isolated structures can be designed with a TG on both source and drain sides. A schematic drawing of such a device, referred to in this work as TG-PPD-JFET, is shown shown in Fig. 3.3b. Figure 3.5 shows the square root characteristic measured on a $W_{JFET}/L_{JFET} = 10\, \mu\text{m}/7\, \mu\text{m}$ TG-PPD-JFET (with $W_{TG}/L_{TG} = 10\, \mu\text{m}/7\, \mu\text{m}$). As can be observed, the measured current varies significantly with the TG biasing voltage. This behavior is due to the fact that the JFET is in series with two TG, which usually have an asymmetrical channel doping (to avoid charge spill back in the PPD [BBK12]) and present a strong channel resistance when the currents flows from the FD toward the PPD. This means that if the gain $W_{JFET}/L_{JFET}$ of the JFET is too high, the measured output current will be limited by the TG transistors and not by the JFET. As a consequence, no meaningful $V_{pin}$ value can be extracted. For this reason these structures are not recommended for the estimation of $V_{pin}$. Figure 3.6 shows the Sqrt.

---

3 Or with only one TG on one side. In this case the PPD is partially pinned.

4 Maximum currents of the order of a few $\mu\text{A}$ have been measured on TG test transistors with $W_{TG}/L_{TG} = 10\, \mu\text{m}/7\, \mu\text{m}$.
Chapter 3. Definition, estimation and modulation of the pinning voltage

Figure 3.5: Experimental square root of the drain to source current \( I_{DS} \) as a function of the gate to source voltage \( (V_{SG}) \) measured on a TG-PPD-JFET structure (Fig. 3.3b). As can be observed, \( I_{DS} \) always depends on the TG biasing voltage \( V_{TG} \). Therefore, no meaningful \( V_{pin} \) can be extracted. The tested device is a TG-PPD-JFET with \( W_{JFET} = 10 \mu m \), \( L_{JFET} = 20 \mu m \) (foundry A). The TG size is \( W_{TG} = 10 \mu m \), \( L_{TG} = 7 \mu m \).

characteristic simulated in TCAD. The simulated JFET structure is identical to the one used for the simulations in Fig. 3.2\(^5\). As it can be observed, the pinning voltage estimated with the Sqrt. method gives a good estimate of the \( \Delta \Phi_{max} \) value of the simulated structure. It can be inferred that this method is a suitable technique for the estimation of the absolute value of \( V_{pin} \).

3.3.1.2 The Floating Source Method

The floating source method proposed in [Cou09] consists in leaving the source of a PPD-JFET structure floating and monitoring its source potential \( V_S \) as a function of the applied drain potential \( V_D \). This method is based on the assumption of a “on-off” behavior of the JFET. In particular it is assumed that, as long as \( V_{SG} < V_p \), the JFET is on and the capacitance of the floating source is charged by a current \( I_{DS} > 0 \) (\( V_S \) follows \( V_D \)). After pinch-off (\( V_{SG} > V_p \)) the JFET is considered to be in off mode (\( I_{DS} = 0 \)) and \( V_S \) does not follow \( V_D \) anymore. \( V_p \) is extracted as the \( V_S \) potential at saturation. In this measurement, a current \( I_{out} \) is forced at the source.

In practice \( I_{DS} \) is never zero, as there is always a subthreshold current flowing in the JFET due to the net thermionic emission of electrons from the source toward the channel [Bre75]. As a result, \( V_S \) will follow the \( V_D \) potential even after pinch-off. In particular:

\(^5\)Note that TCAD simulation have not been calibrated to match experimental data.
3.3. Overview on pinning voltage estimation methods

![Graph showing the relationship between \( V_{\text{SG}} \) and \( \sqrt{I_{\text{DS}}} \)]

Figure 3.6: Square root of the drain to source current \( (I_{\text{DS}}) \) as a function of the gate to source biasing voltage \( V_{\text{SG}} \) simulated for the same JFET structure as in Fig. 3.2. As it can be observed, the \( V_{\text{pin}} \) value estimated with the Sqrt. method corresponds to the \( \Delta \Phi_{\text{max}} \) value in Fig. 3.2b.

- For \( V_D < V_p \) (Fig. 3.7b), the current charging the source capacitance \( (I_C) \) becomes zero when \( I_{\text{JFET}} = I_{\text{out}} \).
- For \( V_D > V_p \) (Fig. 3.7c), the JFET is in subthreshold conduction and the measured \( V_S \) depends on \( I_{\text{out}} \) and on the hold time \( t_H \) between two \( V_D \) steps.

Figure 3.7a shows the \( V_S \) potential as a function of \( V_D \) measured with the test set-up in Fig. 3.7b for different \( I_{\text{out}} \) values.\(^6\) As can be observed, arbitrary \( V_p \) values can be estimated with this method depending on \( I_{\text{out}} \). It should also be noted that since the saturation of the \( V_S \) curve depends on a current balance (and thus on the value of \( I_{\text{DS}} \)), different \( V_p \) values are to be expected for two devices with the same width and different lengths (whereas they should have the same \( V_p \) value if \( L_{\text{JFET}} \) is long enough). A similar test set-up is used in [Hyn81] to measure the potential levels in virtual phase CCDs. With respect to [Cou09], a small \( V_{\text{DS}} \) value is maintained during the whole acquisition. However, the considerations on the validity of the method remain the same, as the saturation point of \( V_S \) will still be a function of \( I_{\text{out}} \) and of the hold time.

### 3.3.1.3 Current Method

In the extraction method discussed in [PU09] by Park et al., a small voltage difference is applied between \( V_D \) and \( V_S \) (10 mV), and \( I_{\text{DS}} \) is monitored as their potential is increased with \(^6\)Note that if \( I_{\text{out}} \) becomes too small, the effective output current will be the leakage current of the experimental set-up.
Figure 3.7: (a) Source potential ($V_S$) as a function of the drain potential ($V_D$) measured on a PPD-JFET structure for different output current values with the floating source extraction method [Cou09]. The pinning voltage is extracted as the $V_S$ potential at which $V_S$ does not follow $V_D$ any more. As can be observed, depending on the accuracy of the experimental set-up ($I_{out}$), an arbitrary $V_p$ can be estimated with this method. The tested device is a PPD-JFET with $W_{JFET} = 10\,\mu\text{m}$ and $L_{JFET} = 20\,\mu\text{m}$ (foundry B). (b) Equivalent circuit of the test set-up for the floating source extraction method discussed in [Cou09]. $I_{out}$ can be due to parasitic leakage currents or can be forced during the measurement. As illustrated in (c) and (d), if $V_D < V_p$ the current charging the source capacitance $I_C = 0$ when $I_{JFET} = I_{out}$, whereas if $V_D > V_p$ the JFET is in sub threshold conduction and the measured $V_S$ depends on $I_{out}$ and on the hold time $t_H$ between two $V_D$ steps.
3.3. Overview on pinning voltage estimation methods

respect to $V_G$. $V_{\text{pin}}$ is estimated as the $V_S$ potential at which $I_{DS} = 0$ (Fig. 3.8). Here this method is referred to as the Current Method (CM). Unlike the SQRT method, the CM is not based on the resolution of JFET equations and like the floating source method, it is based on the assumption of an “on-off” behavior of the JFET. By looking at the current in the logarithmic scale, we can see that the zero current condition cannot be reached (as the minimum measurable current corresponds to the accuracy of the test set-up). By comparing the CM $I_{DS}$ characteristic to the SQRT characteristic, it can be observed that this method provides an overestimation of $V_p$. In addition, it can also be observed that the biasing condition at which $V_{SG} = V_{\text{psqrt}}$ corresponds to the transition of the CM characteristic from the linear region to the logarithmic regime (sub-threshold region). This potential corresponds to the $V_{SG}$ above which the conduction between source and drain is dominated by the thermionic emission of charges from the source toward the JFET channel. Thus the experimental set-up proposed in [PU09] is suitable for the estimation of $V_{\text{pin}}$, as long as the pinch-off voltage is estimated as the potential at which the I-V characteristic enters the logarithmic region and not when the current becomes “zero”. Even if this approach does not provide an accurate and unique $V_{\text{pin}}$ value (as there is no net transition between the two working regions), it has the advantage with respect to the SQRT method of being compatible with shorter JFET lengths (given the small applied $V_{DS}$) and to be based on a “symmetrical biasing” of the JFET.

3.3.1.4 The “Rectangle” method

The “rectangle” method is a pinning voltage estimation technique based on the “rectangle” structure shown in Fig. 3.9 and which is often used by manufacturers [Lah15]; [Kor15] during process development or production line quality assessment. The method working principle is as following: the FD is biased at 3.3 V, whereas the PPD is left floating, and the output potential $V_{\text{out}}$ is monitored as a function of the TG biasing voltage. A constant current $I_{\text{out}}$ (which can be of the order of 1 nA [Lah15]) is injected in the PD. The pinning voltage is extracted as the $V_{\text{out}}$ potential at saturation. Like the floating source method, this method is also based on the assumptions that the potential applied to the biasing electrode is equal to the PPD potential ($V_{\text{PPD}} = V_{\text{out}}$) and that once the PPD potential reaches $V_{\text{pin}}$, no more current can flow in the structure. The same considerations drawn for the floating source method can be extended to the “rectangle” method. In particular, as schematized in Fig. 3.9e, $V_{\text{out}}$ can become higher than the maximum PPD potential ($V_{\text{pin}}$), since saturation is reached only when the sub-threshold current $I_{\text{subth}}$ of the device formed by the series of the TG and of the PPD JFET becomes equal to $I_{\text{out}}$. With respect to the floating diffusion method, results obtained on “rectangle” devices can be even harder to interpret, as measurements can be significantly affected by the design of the TG.

\footnote{Or the $V_S$ potential at which the $I_{DS}$ current reaches a certain percentage (for example 1%) of the initial current value [Lah15].}
Figure 3.8: (a) Drain to source current $I_{DS}$ measured as a function of the source to gate voltage $V_{SG}$ for $V_{DG} = 10$ V. In [PU09] the pinch-off voltage $V_p$ is estimated as the $V_{SG}$ potential at which the $I_{DS}$ current is zero. (b) Equivalent circuit of the test set-up discussed in [PU09]. Schematic potential diagram for (c) $V_D < V_p$ and (d) $V_D > V_p$. 
3.3. Overview on pinning voltage estimation methods

Figure 3.9: (a) “Rectangle” structure used for the estimation of $V_{\text{pin}}$. (b) Working principle: $V_{\text{FD}}$ is biased at 3.3 V and $V_{\text{pin}}$ is retrieved as the $V_{\text{out}}$ at saturation (as it is assumed that no current flows in the structure once $V_{\text{out}} > V_{\text{pin}}$). Schematic circuit of the test set-up of the rectangle method. A current $I_{\text{out}}$ of about 1 nA [Lah15] is forced at the output. In practice, there is always a current flowing in the structure due to the thermionic emission of carriers across the potential barrier at the PPD-TG (d) or the barrier between the n+ output electrode and the PPD (e). The saturation value of $V_{\text{out}}$ depends on a balance of current ($I_{\text{CS}} = 0$ only when $I_{\text{out}} = I_{\text{subth}}$), therefore and $V_{\text{out}}$ can become larger than $V_{\text{pin}}$. As a result, arbitrary pinning voltage values can be obtained with this method depending on the chosen $I_{\text{out}}$. 
3.3.1.5 C-V method

An alternative approach which is used in the industry to measure the pinning voltage is based on C-V (charge-voltage) measurements on large arrays of partially pinned photodiodes [LRF11]; [Lah15]; [Cao15] such as the one shown in Fig. 3.10a. The method consists in measuring the variation of the output capacitance $C_{out}$ of an array of partially pinned photodiodes as a function of the applied biasing voltage $V_{bias}$. The working principle is as follows: while $V_{bias}$ is increased, both the PPD charge and $C_{PPD}$ decrease; eventually the PPD potential reaches its maximum value ($V_{pin}$), $C_{PPD}$ becomes zero and $C_{out}$ reaches its minimum value. $V_{pin}$ is extracted as the biasing voltage at which $C_{out}$ reaches a plateau. An example of experimental measurements obtained on different PPD areas is shown in Fig. 3.10b. These data are a courtesy of Lahav Assaf, from TowerJazz, therefore the size of the contact and the exact geometry of the test structure is not known. However some considerations on this methods can nevertheless be made:

- Even when the PPD is fully depleted, the capacitance of the biasing n+ implant keeps decreasing, thus, there is no obvious reason for which the output capacitance should reach a plateau.

- Therefore the plateau probably corresponds to the point when the output capacitance reaches the minimum measurable capacitance, which can either correspond to the parasitic capacitance. The latter can either be limited by the parasitic capacitance of the contact (and if applicable, of the TG link) or by the resolution of the instrument. As a result, it would seem that arbitrary $V_{pin}$ values can be estimated depending on the "zero" of the test set-up.

These results are based only on physical considerations and should be validated experimentally.

3.3.2 In-pixel methods

The in-pixel $V_{pin}$ extraction method has been proposed by Tan et al. in [TBT12], then further discussed in [Goi+14b]; [XGT15]; [Cha+14]; [Inn15]. The method consists in monitoring the electrical injection of carriers in the PPD as a function of the injection potential $V_{inj}$ applied to the FD (by modulating $V_{DDRST}$ while the TG and RST transistors are on). After the injection phase, the TG is turned off, the FD is reset (to sample the reference) and then the TG is turned on again to transfer the injected charge back to the FD and sample the signal. The corresponding timing diagram is shown in Fig. 3.11.

Figure 3.12 shows the experimental measurement of the output charge $Q_{out}$ as a function of $V_{inj}$ (pinning voltage characteristic). The tested device is PPD CIS array fabricated in a

---

8With respect to JFET methods, this approach has also the disadvantage of requiring large test-structure arrays (in order to reach a high enough output capacitance).
3.3. Overview on pinning voltage estimation methods

Figure 3.10: (a) Cross-section of a partially pinned PD structure used for the estimation of $V_{\text{pin}}$ based C-V measurements. Structure can also include a TG. (b) C-V measurements obtained on arrays of partially pinned photodiodes with increasing PPD areas. $V_{\text{pin}}$ is extracted as the biasing potential at which $C_{\text{out}}$ reaches a plateau [LRF11].

Figure 3.11: Timing diagram for the in-pixel estimation of the pinning voltage (reproduced from [Goi+14b])
commercially available 0.18 µm PPD CIS technology (more details are given in table 3.12c). $V_{\text{pin}}$ is estimated as the $V_{\text{inj}}$ potential above which direct charge injection is nil. Whereas in [TBT12], this potential is retrieved by means of a linear fit of the pinning voltage characteristic at small $V_{\text{inj}}$ (linear method), the integral method proposed in [Goi+14b] takes into account the integration of charges on the PPD capacitance $C_{\text{PPD}}$. Note that in practice (as was expected from the results of the simulation in Fig. 3.2), by looking at the pinning voltage characteristic in logarithmic scale, it can be observed that the PPD is far from being empty when $V_{\text{inj}} = V_{\text{pin}}$ (it still contains a few percent of the initial charge, which can be of the order of several thousands of electrons).

Four main working regions can be identified on the characteristic:

- In region A ($V_{\text{inj}} < V_{\text{pin}}$) charges are directly injected in the PPD and $Q_{\text{out}}$ is a linear function of $V_{\text{inj}}$. As discussed in chapter 4, the PPD charge measured at $V_{\text{inj}} = 0$ corresponds to the Equilibrium Full Well capacity (EFWC).
- In region B ($\Delta E_{\text{fnmax}} > V_{\text{inj}} > V_{\text{pin}}$) charges are injected in the PPD by thermionic emission. Since the thermionic emission is an exponential function of the potential barrier seen by electrons, the pinning voltage characteristic is a logarithmic function of $V_{\text{inj}}$.
- In region C ($V_{\text{inj}} > \Delta E_{\text{fnmax}}$) the thermionic emission is negligible ($Q_{\text{out}} < 1e^-$), thus the PPD can be considered empty. $\Delta E_{\text{fnmax}}$ can be estimated by finding the intercept between the charge plateau (here $\approx 1e^-$) and the fit of the logarithmic region.
- A fourth working region, corresponding to the charge partition regime [Goi+14b] can be identified on the characteristic. Whereas the other 3 regions mainly depend on the injection phase, charge partition is due to the partition of charge (that was located in the TG channel during charge injection) between the FD and the PPD when the TG is turned off to sample the reference.

As indicated in Fig. 3.12a, different parameters can be estimated from the pinning voltage characteristic: $V_{\text{pin}}$ ($\Delta \Phi_{\text{max}}$), the Equilibrium Full Well Capacity (EFWC) (which will be discussed in section 4.1), the TG channel potential $\Phi_{\text{TG}}$ [Goi+14b]) and $\Delta E_{\text{fnmax}}$. The latter corresponds to the minimum potential that must be applied to a well adjacent to the PPD to completely empty the PPD (i.e. the minimum useful TG channel potential). Note however, that $V_{\text{pin}}$ values estimated with this method should be handled with care, since if the pixel presents a low CTE or if the experimental conditions and the timing diagram are not set carefully, $V_{\text{pin}}$ might not be properly estimated [Goi+14b].

### 3.4 Temperature behavior of the pinning voltage

The effect of temperature on the pinning voltage can be modeled by re-writing equation 3.1 and taking into account the temperature dependence of the different parameters. In the
3.4. Temperature behavior of the pinning voltage

Figure 3.12: (a) Pinning voltage characteristic plotted in linear and logarithmic scales: injected charge $Q_{\text{inj}}$ vs. injection potential $V_{\text{inj}}$ measured in the dark at $T = 60^\circ \text{C}$. (b) Schematic potential diagram in regions A, B and C. The curve has been measured on the PPD CIS pixel-array designed at ISAE which is described in table (c).

<table>
<thead>
<tr>
<th>Node</th>
<th>Array size</th>
<th>pixel pitch</th>
<th>pixel geometry</th>
<th>CVF</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.18 $\mu$m</td>
<td>64 $\times$ 128 pixels</td>
<td>4.5 $\mu$m</td>
<td>2.5 $\mu$m $\times$ 2.5 $\mu$m square PPD</td>
<td>20 $\mu$V/e$^-$</td>
</tr>
</tbody>
</table>
Chapter 3. Definition, estimation and modulation of the pinning voltage

first term of the equation \( \frac{qN_{PPD}d_{PPD}}{2\epsilon_{Si}} \) all parameters are design or geometrical constants, therefore the temperature behavior of \( V_{pin} \) can be simply approximated to the temperature behavior of \( V_{bi} \):

\[
V_{bi}(T) = \frac{kT}{q} \ln \left( \frac{N_a N_{PPD} n_i(T)}{n_i^2(T)} \right)
\]

(3.3)

where \( n_i(T) \) can be modeled as in [Mis+93]. Figure 3.13 shows the pinning voltage characteristic measured at different temperatures, where \( V_{pin} \) is estimated with the integral method [Goi+14b]. Note that at \( T = 233 \) °K and \( T = 263 \) °K the behavior of the pinning voltage characteristic at injection voltages close to \( V_{pin} \) differs from the one observed at higher temperatures. This deviation is attributed to a low injection time, which is not sufficiently long for the PPD to reach equilibrium through thermionic injection. As the \( C_{PPD} \) extraction region [Goi+14b] is smaller at these temperatures, a higher error in the extracted pinning voltage is to be expected. As shown in Fig. 3.14, this simple model reproduces well the increase of \( V_{pin} \) with temperature.

3.5 Static and dynamic pinning voltage modulation methods

In large pixels, the PPD potential is flat (except for the fringing field close to the TG and to the PPD borders) and charge transfer mainly depends on charge diffusion. As discussed in chapter 2, by relying on a simple diffusive transport, the transfer time to reach a good CTE for PPD lengths of several \( \mu m \) can be of the order of several tens of \( \mu s \). These long transfer times are mainly due to the non-directionality of the diffusion process and to the presence of design traps. To overcome these limitations, the PPD potential can be spatially modulated.
3.5. Static and dynamic pinning voltage modulation methods

Figure 3.14: Pinning voltage as a function of temperature (integral method).

to induce a drift field in the PPD, resulting in a double advantage in terms of CTE:

- Charge transport is faster and directional.
- The charge density at the PPD-TG interface is higher, resulting in a higher probability for charges to cross the potential barrier.

Different solutions have been proposed in the literature to induce a drift field in PPD pixels [SPS10]; [Li+12]; [Miy+14]; [Tub+09]. These methods can be divided into two main categories: static and dynamic methods, which are based on the generation of a static and a time varying electric fields, respectively. Static methods are suitable for single-tap (single output) PPD pixels, where charges can be always accelerated in the same direction. These methods involve a geometrical modulation or a doping modulation of the PPD potential and can be rather simple to implement. For multi-tap pixels, a static drift field can strongly limit the number of outputs and the pixel geometry. To implement more exotic devices, such as a pixel demodulator (often referred to as lock-in pixels) for high temporal resolution applications [Lan+00]; [BLS06]; [Sto+11]; [Kim12]; [Sto+11]; [Bon+13a]; [Han+14], it can be of great interest to generate an electric field which can be modulated in time.

3.5.1 Geometrical modulation of the pinning voltage

Caranhac et al. [CT00] proposed to accelerate charge transfer in large area CCD by modulating the smallest geometrical dimension of both the photodiode and the draining gates. Figure 3.15 shows a schematic of the patented device. Zone 1 represents the light sensitive region (photodiode), zone 2 the storage gate and zone 3 the draining gates. As can be observed the
width of the draining gates increases toward the storage gate. As discussed in this section, the narrower the gate width, the less deep the potential well beneath (within certain limits). Therefore, the trapezoidal shape of the gates creates a sort of charge slide, so that carriers which are generated far from the storage region are “captured” by the draining gate and drifted toward the storage gate. This due to the fact that, as discussed in this section, within certain limits, the narrower the gate width, the less deep the potential well beneath. To further enhance charge collection speed, the same geometrical potential modulation principle is applied to the photosensitive area. The photodiode consists of a highly p doped thin layer deposited on a n-layer over a p-substrate (in other words a PPD). The introduction of zones devoid of any n-layer (indicated as 10 in the figure) modulates the pinning voltage, creating an electric field within the photodiode fingers that accelerates electrons toward the draining gates.

Figure 3.15: Example for driving-gate CCD. Figure 4 of US patent [CT00].

### 3.5.1.1 Physical Principle

A simple 1D model of $V_{pin}$, which only depends on the PPD vertical doping profile, has been developed at the beginning of this chapter. However, as discussed in [Tak+10], a 1D approximation of the pinning voltage over-estimates the PPD maximum potential for small PPD widths, as both vertical depletion and lateral depletion must be taken into account.
3.5. Static and dynamic pinning voltage modulation methods

In a first time, we will consider the extension of the depletion region in the vertical and horizontal directions (which is associated to the vertical p+-Nppd junction and to lateral Pwell-Nppd junction, respectively) as two independent phenomena. The minimum biasing potentials that must be applied to the Nppd region to fully deplete the PPD in the vertical direction ($V_{\text{pinVert}}$) or in the horizontal direction ($V_{\text{pinLat}}$) can be estimated in 1D, respectively as:

$$V_{\text{pinVert}} = \left( \frac{d_{\text{ppd}}}{2} \right)^2 \frac{q N_{\text{d,ppd}}}{\epsilon_{\text{Si}}}$$

and

$$V_{\text{pinLat}} = \left( \frac{W_{\text{ppd}}}{2} \right)^2 \frac{q N_{\text{d,ppd}}}{\epsilon_{\text{Si}}} \left( 1 + \frac{N_{\text{d,ppd}}}{N_{a_{-w}}} \right) = V_{\text{pin}} \left( \frac{W_{\text{ppd}}}{2d_{\text{ppd}}} \right)^2 \left( 1 + \frac{N_{\text{d,ppd}}}{N_{a_{-w}}} \right)$$

with $W_{\text{ppd}}$ the PPD width, $d_{\text{ppd}}$ the PPD vertical depth and $N_{a_{-w}}$ the doping concentration of the Pwell surrounding the PPD. For both expressions, the extension of the SCR has been approximated to the one of a one-sided abrupt junction.

If we assume $\left( 1 + \frac{N_{\text{d,ppd}}}{N_{a_{-w}}} \right) \approx 2$, then the minimum $W_{\text{ppd}}$ for which $V_{\text{pinLat}} \approx V_{\text{pinVert}}$ is $W_{\text{ppdMIN}} = \sqrt{2} d_{\text{ppd}}$. If we consider a PPD depth of about 300 nm-500 nm, the minimum PPD width $W_{\text{ppdMIN}}$ for which we should observe geometrical modulation is about 400 nm-700 nm.

In practice, as shown later in this section, geometrical modulation is observed up to several $\mu$m widths. This can be explained by a lateral enhancement of the vertical depletion, which is a phenomenon also observed in short-channel MOS transistors, causing Drain induced Barrier Lowering (DIBL) effects [TN09]. This lateral enhancement is even more accentuated when the PPD has both a small length and a small width. To take into account these 3D effects, Poisson’s equation should be solved in 3D. A simpler approach is given by TCAD simulations, which have the advantage, with respect to analytical solutions, to also take into account realistic doping profiles.

### 3.5.1.2 TCAD simulations

Lateral enhancement of the extent of the vertical depletion region has been simulated in TCAD, based on the rectangular partially pinned photodiode structure in Fig. 3.16\(^9\). The pinning voltage has been estimated for $L_{\text{PPD}} = 5 \mu$m and increasing $W_{\text{PPD}}$ dimensions, where $V_{\text{pin}}$ is estimated as the maximum variation of the electrostatic potential as suggested in chapter 3. As can be observed in Fig. 3.17, pinning voltage variations of the order of 100 mV-150 mV (for an intrinsic pinning voltage of about 700 mV) can be obtained by varying the PPD width\(^{10}\). Figure 3.18 shows the spatial distribution of the maximum variation of the PPD potential in two 3D PPD structures with $L_{\text{PPD}} \times W_{\text{PPD}} = 1 \mu$m $\times$ $1\mu$m and $L_{\text{PPD}} \times W_{\text{PPD}} = 10\mu$m $\times$ $1\mu$m, respectively\(^{11}\). As can be observed, combining a small width with a small length results in a further decrease of $V_{\text{pin}}$ (about 50 mV here), since vertical

\(^9\)Note that an alternative approach to study this phenomenon could have been to simulate a trapezoidal PPD and monitor the PPD potential variation as a function of the PPD length.

\(^{10}\)Larger $\Delta V_{\text{pin}}$ could be obtained for larger intrinsic pinning potentials.

\(^{11}\)The 3D geometry of the simulated structure is not shown here and include, with respect to the structure in Fig. 3.16 a TG which covers the whole PPD width.
Chapter 3. Definition, estimation and modulation of the pinning voltage

Figure 3.16: Simulated 3D partially pinned photodiode structure (TCAD) for the study of the geometrical modulation of the PPD potential.

depletion is enhanced the lateral depletion from the three sides of the PPD.

3.5.1.3 Experimental Results

The effect of the PPD size on the pinning voltage has been measured both on PPD-CIS arrays and on isolated PPD-JFET test structures. Experimental results are shown in Fig. 3.19. As expected from simulations, the pinning voltage is a strong function of the PPD width up to a few µm. In particular \( V_{\text{pin}} \) variations of the order of 0.5V-0.6 V are observed for this technology. The smaller \( V_{\text{pin}} \) values measured with the in-pixel method for \( W_{\text{PPD}} = 2.5 \) µm is due to the combination of both a small length and a small width (lateral assisted vertical depletion). Finally, it can also be observed that the floating source method and the current method do not provide the absolute value of \( V_{\text{pin}} \). Nevertheless, these methods still allow monitoring \( V_{\text{pin}} \) relative variations.

3.5.2 Doping modulation

As second approach to modulate the pinning voltage consists in varying the doping profile along the charge transfer path. This can be implemented by means of a linear doping gradient as in [Dur+10] or in two (or more) pipelined doping steps as in [Miy+14]; [Li+12]. The main advantage of doping modulation with respect to geometrical modulation is the increased
3.5. Static and dynamic pinning voltage modulation methods

Figure 3.17: Simulated $V_{pin}$ for the partially pinned photodiode structure in Fig. 3.16 as a function of the PPD length $L_{PPD}$ (for $W_{PPD} = 5 \mu m$).

Figure 3.18: Distribution of the maximum variation of the PPD potential $\Delta V_{PPD}$ in a 3D PPD structure with (a) $L_{PPD} = 10 \mu m$ and (b) $L_{PPD} = 10 \mu m$, respectively. The PPD width is $W_{PPD} = 1 \mu m$ for both structure. The $\Delta V_{PPD}$ along the cuts A-A’ and B-B’ is shown in (c).
design freedom (as it does not requires particular geometrical constraints). However, this solution cannot be implemented in commercially available PPD-CIS technologies, which usually provide only one (or two) constant pinning implants to implement the PPD.

3.5.3 Lateral Electric Field Modulation (LEFM)

A dynamic potential modulation method has been proposed by Kawahito et al. in 2013 [Kaw+13]. This method, referred to as Lateral Electric Field Modulation (LEFM) method is based on the control of the PPD potential by means of pairs of lateral gates. A fully working sensor designed on a dedicated 0.11 µm PPD CIS technology based on the LEFM has recently been presented in [Han+14]. In this section, the working principle of LEFM is first presented then the method is simulated in TCAD and the main design trade-offs are discussed. Finally the last part of this section presents experimental results obtained for a two-tap detector based on LEFM which has been designed in a commercially available 0.18 µm technology.

3.5.3.1 Modulation Principle

The LEFM method consists in modulating the PPD potential $V_{PPD}$ by means of the fringing field induced by pairs of lateral gates (LG). In particular, by introducing multiple pairs of LG, whose potential varies in time, a dynamic modulation of the PPD potential profile can be obtained.
3.5. Static and dynamic pinning voltage modulation methods

Figure 3.20 shows the cross-section of a PPD associated to a set of lateral gates (LG) (located on both sides of the PPD). To visualize the corresponding 3D device, one should imagine that the TG is located perpendicular to the page. In this structure, each LG is associated to a n+ diffusion biased at a potential \( V_D \). As is will be shown later, these diffusions can be used to drain the charge generated by interface states under the LG, but are not essential for the LEFM working principle.

![Cross-sectional view of the 2D LEFM structure simulated in TCAD. Schematic potential diagram for increasing lateral gate biasing potentials \( V_{LG} \).](image)

Since the pinning implant is highly doped, it can be assumed that the surface remains pinned to the substrate potential. Therefore the PPD potential cannot be larger than the intrinsic pinning voltage (\( V_{pinHI} \)) which would be measured without geometrical modulation, whatever the applied \( V_{LG} \) (within typical biasing ranges). This means that to be able to modulate the PPD potential, \( V_{pin} \) must first be reduced by means of geometrical modulation. In other words the LEFM works only on narrow PPDs and the LEFM consists in “compensating the geometrical modulation” by means of a fringing field. If we indicate as \( V_{pinLO} \) the pinning voltage of a narrow PPD before applying LEFM, the maximum potential modulation that can be generated within the PPD is:

\[
\Delta V_{PPD} = V_{pinHI} - V_{pinLO} \quad (3.6)
\]

From this analysis, it can easily be inferred that the narrower the PPD, the larger the \( \Delta V_{PPD} \) (and thus the electric field) that can be generated.
3.5.3.2 TCAD simulations

The 2D structure in Fig. 3.20 was simulated in TCAD. The PPD is first emptied (by activating the LG), then the LG biasing potential $V_{LG}$ is decreased from 3.3 V to $-1$ V. Since in 2D the pinning implant is not connected to the substrate, a small surface electrode biased at 0 V is added on top of the PPD.

Figure 3.21 shows the maximum PPD potential as a function of $V_{LG}$ for different PPD widths. As expected, the effect of the LG potential is much stronger on the narrower pixels (which have a lower pinning voltage due to geometrical modulation effects), whereas almost no modulation is observed for the 4µm pixel.\(^{12}\)

\[\text{Figure 3.21: Simulated maximum PPD potential as a function of } V_{LG} \text{ for different PPD widths. The simulated structure is shown in Fig. 3.20.}\]

3.5.3.3 Device under test

A test chip has been designed with the following goals:

1. Verify the LEFM working principle on a commercially available 0.18 µm PPD CIS technology.

2. Study the effect of the PPD width on the LEFM.

3. Compare different design solutions.

\(^{12}\)Note that the intrinsic pinning voltage is larger than the one estimated in Fig. 3.17. This difference is mainly due to the fact that here the structure is simulated in 2D (an infinite depth is assumed by the simulator), whereas the structure simulated in Fig. 3.17 is a 3D structure.
3.5. Static and dynamic pinning voltage modulation methods

The tested device is a 1D pixel array, divided into 25 sub-arrays of 8 pixels each, with different sizes and different geometries. Each pixel has 2 outputs, associated to 2 transfer gates TG1 and TG2. The in-pixel output electronics consists of two identical 4T-pixels readout chains (Fig. 3.22) such as the one described in appendix D. To increase the number of collected electrons, pixels have been designed as “5-fingered” structures, with communalised outputs. Two pairs of LG are associated with each finger. All the LGs on the same side of the pixel are connected together. The PPD potential is modulated with the two signals LG1 and LG2, which allow orientation of the PPD charge either toward TG1 or toward TG2. In this work only 8 pixel variations are studied\(^{13}\). The tested pixels can be divided into two main categories: pixels with a draining diffusion associated to the LG (“D pixels”) and pixels without the draining diffusion (“ND pixels”). The layout of these two pixel designs is shown in Fig. 3.23. For each pixel-type, 4 different PPD widths (0.5 µm, 1.0 µm, 2.0 µm and 4.0 µm) have been tested. Note that the goal of this test chip is not to implement a “ready-to-use” imager for a particular application but to verify the charge orientation efficiency that can be obtained with LEFM on the tested technology and to get a first “feeling” of the best design solutions. For better statistics and uniformity, it would be interesting to confirm the results presented in the following on a larger matrix.

3.5.3.4 Experimental Results

This section presents the main experimental results obtained on the test-chip. Note that all the tested pixel variations have different CVF values and different collection areas (i.e. different FWC values). Because of strong pixel blooming effects (due to large differences in FWC) and of the poor statistics (8 pixels for each pixel type), the uncertainty on the CVF extracted with the MV method on the pixel array is very large. For these reasons, only normalized output signals are presented here. To compare pixel variations in terms of absolute output charge values, a larger matrix of pixels should be designed on a second test-chip, with fewer (or no) CVF variations.

Charge orientation efficiency:

The first experimental validation of the LEFM consisted in the measurement of the efficiency in terms of charge orientation toward one of the two TG, as a function of \(V_{LG}\). Charges are generated in the PPD by means of a pulsed LED (\(\lambda = 540 \text{ nm}\)). The pulse height and width are chosen so that the generated charge density is about a few tens of \(e^-/\mu m^2\). During charge integration LG2 and LG1 are biased at \(V_{LG2}\) and \(V_{LG1}\), respectively. In particular, one of the LG potential is varied while the other LG is biased in accumulation mode (\(V_{LG} = -0.4 \text{ V}\)). The timing diagram used for these measurements is shown in Fig. 3.24. Both FD (FD1 and FD2) are reset, the reference is sampled, then both TGs (TG1 and TG2) are activated simultaneously (so that electrons can be synchronously transferred to both FDs), then the signal is sampled. As the experimental set-up only allows to readout one channel at the time, both reference and signal are sampled only at output1. The goal of this

\(^{13}\)These variations correspond to the variations which gave the best results.
Chapter 3. Definition, estimation and modulation of the pinning voltage

Figure 3.22: Schematic diagram of the readout circuit of a 2-tap 1D-pixel array.

Figure 3.23: Layout view of the 2 different studied pixel designs: (a) with and (b) without a charge draining diffusion associated to the LGs (pixels “D” and “ND”, respectively).
3.5. Static and dynamic pinning voltage modulation methods

![Timing diagram](image)

Figure 3.24: Timing diagram for the estimation of charge orientation efficiency.

measurement is to monitor the charge sharing between output\textsubscript{1} and output\textsubscript{2} as a function of $V_{LG}$, giving an estimate of the charge orientation efficiency that can be obtained in a LEFM device.

Fig. 3.25, shows the normalized output signal measured for different PPD widths for a pixel of type 'ND' as a function of $V_{LG1}$ and $V_{LG2}$. As expected, charge orientation efficiency improves as $V_{LG1}$ is increased and a larger potential modulation is observed for narrow PPD widths (as the maximum $\Delta V_{pin}$ is larger). In particular, for $W_{PPD} = 0.5$ $\mu$m, a very good orientation efficiency (up to 90%) can be obtained for a LG biasing voltage of about 2 V.

Figure 3.26 shows a comparison between the normalized output signal measured for different PPD widths as a function of $V_{LG1}$ for a pixels of type "ND" and of type "D" (with LG\textsubscript{2} biased in accumulation mode). As it can be observed, increasing too much $V_{LG1}$ results in a sudden drop of the orientation efficiency. This behavior can be explained by the fact that increasing $V_{LG1}$ results in a decrease of the barrier at the PPD-LG interface. For the “D" pixels, as soon as this barrier becomes low enough, the excess PPD charge is overflows toward the draining diffusion. The LG biasing potential $V_{LGmax}$ at which the measured charge drops, corresponds to the maximum “useful” biasing voltage that can be applied to the device without loosing signal charge. The same considerations can be applied to “ND” pixels, however, as electrons are already accumulated under the LG (since $V_{LG}$ is biased in DC), the lowering of the barrier height does not lead to a visible draining of carriers.\textsuperscript{14} As long as $V_{LG} < V_{LGmax}$, the presence (or not) of the draining diffusion does not affect the charge orientation efficiency.

As can be observed in the figure, $V_{LGmax}$ increases as the PPD width is increased. This

\textsuperscript{14}As a consequence, to have a good estimation of $V_{LGmax}$, it is better to perform this characterization on “ND” pixels.
behavior can be explained by the fact that the potential barrier seen by the electrons depends on the PPD potential. In particular, the smaller $V_{LG_{max}}$ measured in narrow PPDs is due to the smaller pinning voltage. Note also that as $V_{LG_{max}}$ depends on the PPD potential (and therefore on the signal level), the higher the amount of integrated charge, the smaller $V_{LG_{max}}$ and thus the lower the orientation efficiency. Note that these measurements have been performed at low charge levels. If the signal is increased, $V_{LG_{max}}$ is expected to decrease.

**Charge transfer efficiency :**

The second experimental validation of the LEFM consisted in measuring the effect of $V_{LG}$ on the CTI. For this purpose, data has been acquired with the timing diagram in Fig. 3.27. Before the light pulse, both FDs are reset, the reference is sampled on output1 and the PPD is emptied by pulsing TG2 for about 5 $\mu$s. Photo-charges are generated by pulsing the LED on, then TG1 is activated to transfer the collected carriers to FD1. The transfer time (which corresponds to the TG pulse width here) is varied from 10 ns to 1 $\mu$s. $V_{LG2} = -0.4$ V during the whole acquisition. Figure 3.28 and Fig. 3.29 show the CTI measured for different PPD widths on pixels of type “D” and “ND”, respectively. As expected, the larger CTI improvement with $V_{LG}$ corresponds to the smaller PPD width (for both pixel types). In particular, the CTI improves of about a factor 1.5 for $W_{PPD} = 1 \mu$m, whereas almost no enhancement is observed for $W_{PPD} = 4 \mu$m. It can also be observed that the CTI measured for $W_{PPD} = 1 \mu$m is better than the one for $W_{PPD} = 0.5 \mu$m. A possible explanation for this result could be a higher potential barrier at the PPD-TG interface for the 0.5$\mu$m PPD (which is below the minimum PPD width recommended for this technology) due to a narrow transfer channel.
3.5. Static and dynamic pinning voltage modulation methods

![Graph showing normalized output signal as a function of VLG1 for different PPD widths.]

Figure 3.26: Comparison between the normalized output signal measured for different PPD widths as a function of $V_{LG1}$ for a pixels of type “ND” and of type “D”.

![Timing diagram for charge transfer efficiency.]

Figure 3.27: Timing diagram for the estimation of charge transfer efficiency.
Figure 3.28: CTI measured for different PPD widths on pixels of type “ND”.

Figure 3.29: CTI measured for different PPD widths on pixels of type “D”.
3.6 Conclusions

This chapter focused on the definition, modeling and estimation of $V_{\text{pin}}$. Two different physical definitions of $V_{\text{pin}}$ are used in the CIS community: $\Delta \Phi_{\text{max}}$ and $\Delta E_{\text{fmax}}$ between equilibrium and full depletion conditions. $\Delta \Phi_{\text{max}}$ corresponds to the PPD potential floor, whereas it has been shown that $\Delta E_{\text{fmax}}$, which is the PPD channel potential at which the PPD is empty, also corresponds to the minimum TG channel potential $\Phi_{\text{TG}}$ that must be applied to extract all charges from the PPD. In this study, $V_{\text{pin}}$ has been defined as $\Delta \Phi_{\text{max}}$. A simple 1D temperature model of the pinning voltage has also been proposed and validated with experimental measurements. In particular it has been shown that $V_{\text{pin}}$ increases as the temperature is increased. As it will be discussed in chapter 4, these results are fundamental to model FWC variations with temperature.

$V_{\text{pin}}$ is measured both with in-pixel measurements and electrical measurements performed on isolated test-structures (or test-structures arrays). The pros and cons of the different methods addressed in this work are summarized in table 3.1. It has been shown that the floating source method and the rectangle method are not suitable for the estimation of the absolute value of $V_{\text{pin}}$, as arbitrary values can be extracted depending on the experimental conditions. They however allow to observe $V_{\text{pin}}$ relative variations (for example as a function of the PPD width). The absolute value of $V_{\text{pin}}$ can be extracted from PPD-JFET structures with the square root method, however this technique should not be used on short devices as measurements can be affected by DIBL phenomena. The pinning voltage can also be estimated from the $I_{\text{DS}}(V_{\text{SG}})$ characteristic of PPD-JFETS (current method), however it has been shown that $V_{\text{pin}}$ should not be retrieved as the $V_{\text{SG}}$ potential corresponding to a “zero” current condition (or to a percentage of the initial current), but as the $V_{\text{SG}}$ potential at which the characteristic enters the logarithmic region. Reliable values of $V_{\text{pin}}$ can finally be extracted with the in-pixel method, on the condition that the timing diagram and the biasing voltages are chosen respecting the recommendations in [Goi+14b].

Test structure methods have the advantage of being based on simple I-V or C-V measurements, that can be performed by wafer probe. They also allow to easily monitor the effect of process variations and to test many different PPD widths. However, because of the presence of n+ implants on both sides of the PPD channel, JFET measurements do not allow to observe $V_{\text{pin}}$ variations with $L_{\text{PPD}}$. On the other hand, the in-pixel approach gives an estimate of $V_{\text{pin}}$ in a real in-pixel environment (therefore enables observation of the effect of both the PPD width and PPD length) and allows to monitor within the same acquisition, other PPD CIS parameters, such as $\Delta E_{\text{fmax}}$, the Equilibrium Full Well Capacity (EFWC) and the TG channel potential [Goi+14b]. For these reasons the two approaches should be considered complementary.

This chapter also discussed two potential modulation methods that can be implemented in PPD CIS to enhance the charge transfer speed. The geometrical modulation is a static modulation method, which consists in shrinking the minimum PPD size to reduce the PPD pinning potential by means of lateral enhanced vertical depletion. Note that during the design of a high temporal resolution detector, one should take a particular care while estimating the
effect of the PPD shape on charge transfer efficiency. For example a triangular PPD will enhance charge transfer speed even if the PPD dimensions are too small to induce a drift field, as on average, charges will tend to stay in the region where the charge density is lower, i.e. closer to the TG. As a result, wrong conclusions can be drawn from standard CTE measurements. A possible approach to only measure the effect of the electric field is to add a storage gate to the pixel (as suggested in chapter 2), which allows to release the packet of charge at the end of the PPD, whichever the PPD shape. This chapter also presented experimental results on 2-tap lateral electric field modulation (LEFM) pixels designed in a commercially available 0.18 µm technology. It has been shown both by means of TCAD simulations and experimental measurements that LEFM is effective only in narrow PPDs (ideally below 1 µm for the tested technology), as the PPD potential can only be modulated between the geometrically modulated pinning voltage and the pinning voltage corresponding to a zero geometrical modulation (referred here as intrinsic pinning voltage). A good charge orientation efficiency (up to 90%) has been obtained for 1 µm and 2 µm PPD pixels, however the improvement in term of CTI is not very large (less than a factor 2), due to the small maximum electric field that can be generated in the PPD with this method on the tested technology\textsuperscript{15}. Since the implementation of a LEFM pixel involves significant geometrical constraints (and a large reduction of the fill factor, if the pixel includes lateral draining diffusions) and an increase in the dark current due to the lateral gates that are not biased in accumulation mode [MST08], this modulation method is of interest with respect to static solutions only for applications which require a dynamic orientation of carriers. These first experimental results have been obtained on a small 1D array, which presented large CVF and FWC differences between pixel variations. To further investigate LEFM with better statistics, new measurements should be performed on a larger and more uniform pixel array.

\textsuperscript{15}Better results could probably be obtained on a different technology with a larger intrinsic pinning voltage.
### 3.7 Summary of pro and cons of pinning voltage estimation methods

<table>
<thead>
<tr>
<th>Method</th>
<th>Pros</th>
<th>Cons</th>
</tr>
</thead>
<tbody>
<tr>
<td>In-pixel method</td>
<td>• Real in-pixel environment</td>
<td>• Few pixel variations can be implemented on large arrays</td>
</tr>
<tr>
<td></td>
<td>• Allows to observe $V_{\text{pin}}$ variations with both $L_{\text{PPD}}$ and $W_{\text{PPD}}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Meas. of other parameters ($\Delta E_{\text{fmmax}}$, EFWC, TG channel potential)</td>
<td></td>
</tr>
<tr>
<td>SQRT method (JFET)</td>
<td>• Simple I-V measurement</td>
<td>• $L_{\text{PPD}}$ must not be too short to avoid DIBL effects</td>
</tr>
<tr>
<td></td>
<td>• Possibility to test many pixel variations</td>
<td>• Does not reproduce a real in-pixel environment</td>
</tr>
<tr>
<td></td>
<td>• Sqrt characteristic is linear (not ambiguous linear fit)</td>
<td>• Does not allow to observe $V_{\text{pin}}$ variations with $L_{\text{PPD}}$</td>
</tr>
<tr>
<td></td>
<td>• Allows to observe $V_{\text{pin}}$ variations with $W_{\text{PPD}}$</td>
<td></td>
</tr>
<tr>
<td>Current method (JFET)</td>
<td>• Simple I-V measurement</td>
<td>• Not based on the solution of JFET equations</td>
</tr>
<tr>
<td></td>
<td>• Possibility to test many pixel variations</td>
<td>• Does not provide the absolute value of $V_{\text{pin}}$</td>
</tr>
<tr>
<td></td>
<td>• Allows to observe $V_{\text{pin}}$ relative variations with $W_{\text{PPD}}$</td>
<td>• I-V characteristic is not linear (not possible to perform a linear fit to determine the “zero” current point).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Does not allow to observe $V_{\text{pin}}$ variations with $L_{\text{PPD}}$</td>
</tr>
</tbody>
</table>
### Chapter 3. Definition, estimation and modulation of the pinning voltage

<table>
<thead>
<tr>
<th>Method</th>
<th>Pros</th>
<th>Cons</th>
</tr>
</thead>
<tbody>
<tr>
<td>Floating source method (JFET)</td>
<td>• Simple V-V measurement</td>
<td>• Not based on the solution of JFET equations</td>
</tr>
<tr>
<td></td>
<td>• Possibility to test many pixel variations</td>
<td>• Arbitrary $V_{\text{pin}}$ depending on the output current value</td>
</tr>
<tr>
<td></td>
<td>• Allows to observe $V_{\text{pin}}$ relative variations with $W_{\text{PPD}}$</td>
<td>• Does not allow to observe $V_{\text{pin}}$ variations with $L_{\text{PPD}}$</td>
</tr>
<tr>
<td>Rectangle method (JFET)</td>
<td>• Simple V-V measurement</td>
<td>• Not based on the solution of JFET equations</td>
</tr>
<tr>
<td></td>
<td>• Possibility to test many pixel variations</td>
<td>• Arbitrary $V_{\text{pin}}$ depending on the output current value</td>
</tr>
<tr>
<td></td>
<td>• Allows to observe $V_{\text{pin}}$ relative variations with $W_{\text{PPD}}$</td>
<td>• Additional incertitude due to the effect of the TG</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Does not allow to observe $V_{\text{pin}}$ variations with $L_{\text{PPD}}$</td>
</tr>
<tr>
<td>C-V measurements</td>
<td>• Simple C-V measurement</td>
<td>• Arbitrary $V_{\text{pin}}$ depending on the minimum measurable capacitance</td>
</tr>
<tr>
<td></td>
<td>• Allows to observe $V_{\text{pin}}$ relative variations with both $L_{\text{PPD}}$ and $W_{\text{PPD}}$</td>
<td>• Required large test-structures arrays</td>
</tr>
</tbody>
</table>

Table 3.1: Table summarizing the pros & cons of the pinning voltage estimation methods studied in this work.
As discussed in the previous chapters, PPD pixels are based on a transfer of charge from the PPD well toward the readout node (the FD). Because of the finite nature of the PPD well, the maximum signal charge is limited by the maximum amount of charge that can be stored on the PPD capacitance $C_{PPD}$, often referred to as Full Well Capacity (FWC). As discussed in appendix B, in PPD CIS the maximum measurable output charge can either be limited by the saturation of the readout electronics (including the ADC), or by the PPD FWC, depending on $C_{PPD}$, on the charge to voltage conversion factor (CVF) and on the output saturation voltage $V_{out\text{sat}}$. In particular, the maximum output charge is usually limited by the PPD FWC when $FWC < \frac{V_{out\text{sat}}}{CVF}$ (or when a positive $V_{LOTG}$ biasing voltage is applied)\(^1\). Prior to this work, in public litterature the PPD FWC was usually considered as a fixed value, and only few works were published on the dependence of the saturation signal with the operation conditions and with the signal level\(^2\); \cite{PKW05}; \cite{Mey13}.

In this work, we propose to express the FWC as:

$$FWC = \frac{1}{q} \int_{V_{OC}}^{V_{pin}} C_{PPD}(V_{PPD}) \, dV_{PPD}$$  \hspace{1cm} (4.1)

with $q$ the elementary charge. $V_{pin}$ is the pinning voltage (discussed in chapter 3), which is reached after the reset of the photodiode, i.e. after the charge transfer phase in standard PPD CIS operation for a no image lag detector \(^2\). At full well, no more charge can be collected by the PPD and the total current across the photodiode is zero (open circuit condition), therefore, the parameter $V_{OC}$ in Eq. 4.1 (referred here as open-circuit voltage) corresponds to the minimum PPD potential. Whereas $V_{pin}$ only depends on the working temperature $T$ and on technological and geometrical parameters (refer to chapter 3), as discussed in this chapter, $V_{OC}$ varies significantly with $T$, but also depending on other experimental conditions, such as the photon flux (i.e. the signal level) and the TG biasing conditions. Not taking into account these effect can lead to unwanted and unpredictable variations of the dynamic range of the detector (for example if the external conditions change radically during the life-time of the detector, as in space applications). These effects are even more critical in high end

---

\(^1\)Note that the physical phenomena described in this chapter are valid for both saturation mechanisms, but they can be observed in their full extent only if the output signal is limited by the PPD FWC.

\(^2\)If the image sensor presents a non-negligible image lag, the PPD never reaches full depletion, leading to an under-estimation of the FWC and $V_{pin}$.
applications where pulsed light signals are involved (such as LIDAR applications), as the FWC can be highly time dependent.

This chapter presents a study on the modeling of the FWC at equilibrium and how its value can be affected by temperature, light flux and the TG biasing conditions. Based on these initial results, a model of the dynamic behavior of the FWC in response to a change in the illumination conditions (such as in pulsed-light applications) is presented. Unless specified, data have been acquired on a detector designed at ISAE, whose details can be found in table 3.12c (page 71).

4.1 Equilibrium Full Well Capacity

4.1.1 Definition and modeling

After the reset of the photodiode, assuming zero charge lag, the PPD is empty and the PPD potential is equal to the $V_{pin}$. If the PPD is reset and left in the dark with the TG accumulated ($V_{TG} = V_{LOTG} < 0$), the PPD capacitance is discharged only by the dark current ($I_{TOT} = I_{junc}$, with $I_{TOT}$ the current flowing in the PPD capacitance), until the p-n junction reaches an equilibrium condition ($I_{junc} = 0$). The saturation charge obtained in dark conditions and neglecting the TG leakage current is referred to as the Equilibrium Full Well Capacity (EFWC). The open circuit voltage $V_{OC}$ corresponding to the EFWC can be obtained by solving:

$$I_{TOT} = I_{sat} \left( e^{\frac{V_{OC}}{n v_{th}}} - 1 \right) = 0$$  \hspace{1cm} (4.2)

with $n$ the diode non-ideality factor ($1 < n < 2$), $v_{th} = \frac{kT}{q}$ the thermal voltage and $I_{sat}$ the saturation current [TN09]. As in standard p-n junctions, the equilibrium condition expressed in (4.2) holds for $V_{OC} = 0$. The EFWC can be calculated with (4.1) as:

$$\text{EFWC}(T) = \frac{1}{q} \int_0^{V_{pin(T)}} C_{PPD}(V_{PPD}) \, dV_{PPD}$$  \hspace{1cm} (4.3)

In practice, in nominal PPD CIS operating conditions, the EFWC cannot be reached and the FWC measured in the dark with TG accumulated ($\text{FWC}_{dark}$) corresponds to a saturation charge which is always slightly lower than the EFWC. This difference is attributed to the fact that the TG will always have a small leakage current (sub-threshold current), whatever the TG biasing voltage during integration. To simplify the development of the model, the small difference between EFWC and FWC$_{dark}$ is neglected. Charge partition phenomena during the transitions of the TG signal [TM86] (which can result in an artificial variation of the FWC) have also been neglected in this study.

94
4.1. Equilibrium Full Well Capacity

4.1.2 Measurement of the EFWC

Three different approaches can be used to measure the EFWC.

A. The first approach consists in measuring the output voltage in the dark, with TG accumulated, at increasing integration times. Since at room temperature the dark current in a PPD is less than $1 \text{e}^-/\text{s} \mu\text{m}^2$ [Rho+11], long integration times (up to ten thousands of seconds per frame) can be necessary to reach the EFWC. This measurement can be extremely time consuming if one wishes to evaluate the EFWC in different experimental conditions (in particular at low working temperatures). Note also that if the PPD-array presents “hot pixels” or if the PPD array is divided into sub-arrays which present substantially different dark current values, dark blooming phenomena [Bel+15] might affect the transfer function.

B. As discussed in section 4.1.1, the EFWC corresponds to the charge at which the PPD potential is zero ($V_{OC} = 0$). This equilibrium condition can be reached by means of an electrical charge injection such as the one described in section 3.3.2 for the measurement of $V_{pin}$. In particular, the EFWC can be estimated as the output charge corresponding to $V_{inj} = 0$. The main source of uncertainty with this method is the amount of extra charge injected into the PPD because of charge partition phenomena.

C. A third method for measuring the EFWC consists in filling the PPD well by means of a light pulse and measuring the output charge once the PPD has reached equilibrium. As it will be discussed in section 4.5, one must wait several tens of s to ensure that the equilibrium condition is reached, thus the time gain with respect to method A is not as high as one would expect.

To simplify analytical developments, it can be assumed that the PPD capacitance remains constant during charge integration. Under this hypothesis, the FWC can be expressed as:

$$FWC = EFWC - \frac{1}{q} V_{OC} C_{PPD}. \quad (4.4)$$

Note that this is a simplification, which is suitable only to roughly represent the effect of different parameters on the FWC. However $C_{PPD}$ variations must be taken into account when fitting experimental results.

4.1.3 EFWC temperature behavior

Figure 4.2a shows experimental EFWC values as a function of temperature (where the EFWC has been measured with method A, with $V_{LOTG} = -0.4$ V). As can be observed EFWC increases almost linearly with $T$. A Schematic drawing of the PPD I-V characteristic in the dark as function of the PPD voltage $V_{PPD}$ for two different temperatures $T_2 > T_1$ is shown in Fig. 4.2b. The figure also shows the corresponding PPD stored charge $Q_{PPD}$. Since in the dark the PPD is never forward biased, the saturation potential is the same at all working
temperatures ($V_{OC} = 0$ V) and $V_{pin}$ increases with temperature (refer to chapter chapter 3), a higher EFWC is expected for $T = T_2$ (the increase in $V_{pin}$ is represented as a left shift of the $Q_{PPD}$ axis origin $Q_{PPD} = 0$). As can be observed, this EFWC model reproduces well the experimental behavior.

### 4.2 Effect of the photon flux on the Full Well Capacity

If the PPD is exposed to a photon flux $\Phi$, with the TG in accumulation mode ($V_{LOTG} < 0$), the open circuit condition can be expressed as:

$$I_{sat} \left( e^{-\frac{V_{OC}}{n
th}} - 1 \right) = I_{ph}(\Phi)$$

(4.5)

with $I_{ph}(\Phi) = QE \times \Phi$ the photo-current. The corresponding open circuit voltage can be calculated as:

$$V_{OC} = -n
th \ln \left( 1 + \frac{I_{ph}(\Phi)}{I_{sat}} \right)$$

(4.6)

By combining (4.4) and (4.6), the FWC can finally be expressed as

$$FWC(\Phi, T) = EFWC(T) + \frac{1}{q} C_{PPD}\nu_{th}\ln \left[ 1 + \frac{I_{ph}(\Phi)}{I_{sat}(T)} \right]$$

(4.7)

As shown in (4.6), under illumination, the open circuit voltage is negative ($V_{OC} < 0$), which means that FWC$>EFWC$ and that the PPD is forward biased at full-well, resulting in blooming phenomena. As shown by Eq. (4.7) and by the experimental measurements in Fig. 4.3a, the FWC is a logarithmic function of the photon flux [Ben+13]. This phenomenon is schematized in Fig. 4.3b, where the sum of the dark current and the photo-current is plotted for two different photon fluxes (solid and dashed red curves, respectively). As $V_{pin}$ is constant and $V_{OC}$ decreases (becomes more negative) with $\Phi$, the FWC increases with the photon flux.
4.2. Effect of the photon flux on the Full Well Capacity

![Graph showing the measured EFWC as a function of temperature.](image)

**Figure 4.2:** (a) Measured EFWC as a function of temperature. (b) Schematic of the PPD I-V characteristic in the dark as function of the PPD voltage $V_{PPD}$ for two different temperatures $T_2 > T_1$. For the purpose of clarity, schematics are not to scale.
Figure 4.3: (a) Electro-optical transfer function measured for different photon fluxes (and different integration times). The dashed line corresponds to the FWC, which increases logarithmically with the photon flux. (b) Schematic of the PPD I–V characteristic in the dark and under two different illumination levels. For clarity purposes, schematics are not to scale. The FWC curve has been measured on the PPD CIS pixel-array designed at ISAE detailed in table (c).
4.3 Temperature behavior of the FWC under stationary illumination

Equation (4.7) indicates that the FWC under illumination is a strong function of temperature. In particular, there are two different and opposite temperature effects, which are schematized in Fig. 4.4b:

- On one hand, as the temperature is increased, there is an increase in the thermal voltage $v_{th}$ and in $V_{pin}$. These two contributions alone would lead to an increase in the FWC with increasing working temperatures (as in dark conditions).

- On the other hand, there is an exponential increase in the saturation current $I_{sat}$ which results in a decrease in $V_{OC}$ and in a net decrease in the FWC.

Figure 4.4a shows the FWC measured for 3 different photon fluxes $\Phi$ as a function of temperature, with TG in accumulation mode. The dashed line refers to the EFWC modeled as in (4.3). The best fit has been obtained with the same parameters as in Fig. 4.2a. As long as the ratio $I_{sub}(\Phi) >> 1$, the temperature dependence of $I_{sat}(T)$ is the dominant effect and the FWC decreases with temperature. If the temperature is increased, the saturation current becomes comparable to the photocurrent and eventually the FWC becomes equal to the EFWC and starts to increase with temperature. These effects are schematized in Fig. 4.4b. As can be observed, the model reproduces well the behavior observed in experimental data.

4.4 FWC variations as a function of temperature for different TG biasing conditions

The biasing of the TG during integration ($V_{LOTG}$) can strongly differ depending on the application requirements. In [MST08] it is shown that applying a negative $V_{LOTG}$ (TG in accumulation mode) avoids the extension of the PPD depletion region under the TG, strongly reducing the dark current. This first biasing mode is thus recommended for low noise applications. On the other hand, a small positive $V_{LOTG}$ is often applied to implement an anti-blooming function (as excess charges are drained toward the FD instead of being injected into the substrate). As both modes of operation are used in commercial and scientific applications, it is important to understand the effect of temperature and of the photon flux in all biasing conditions.

Figure 4.5a shows a schematic drawing of the effect of $V_{LOTG}$ on the PPD I-V characteristic in the dark. In these operating conditions, two main current contributions must be taken into account: the p-n junction current and the TG sub-threshold current $I_{sub}$. Since full well is reached for $I_{junc} = -I_{sub}$, the open circuit condition corresponds to the crossing of the two curves. As shown in the figure, increasing $V_{LOTG}$ results in an increase of $I_{sub}$ and thus in a
Chapter 4. Static and Dynamic behavior of the Full Well Capacity

Figure 4.4: (a) Full well capacity as a function of temperature measured for 3 different photon fluxes and for the TG in accumulation mode. (b) Schematic of the PPD I-V characteristic under illumination as function of the PPD voltage $V_{\text{PPD}}$ for two different temperatures $T_2 > T_1$. For the purpose of clarity, schematics are not to scale.
4.4. FWC variations as a function of temperature for different TG biasing conditions

Figure 4.5: (a) Schematic of the effect of $V_{LOTG}$ on the PPD I-V characteristic in the dark. For the purpose of clarity, the schematic is not to scale and $-I_{sub}$ is plotted instead of $I_{sub}$. Since full well is reached for $I_{junc} = -I_{sub}$, the open circuit condition corresponds to the crossing of the two curves. For the purpose of clarity, schematics are not to scale. (b) Measured and simulated FWC as a function of $V_{LOTG}$ at different $T$ in dark conditions. The best fit has been obtained with the same parameters as in Fig. 4.2a.
smaller FWC. This effect has been also addressed in [Mey13] and [SBT13]. In particular, in the latter, the contribution of the TG sub-threshold current is taken into account by means of a feedforward thermionic emission of charge across the potential barrier between the PPD and the TG channel during charge integration (TG off). Figure 4.5b shows the FWC measured in the dark plotted as a function of $V_{LOTG}$ for three different measurement temperatures. Three operating regions can be identified:

- For negative $V_{LOTG}$ the FWC corresponds to the EFWC (region A).
- When $V_{LOTG}$ is increased, we observe a transition region (region B) in which the FWC drops moderately with $V_{LOTG}$.
- For even higher $V_{LOTG}$, the FWC drops linearly with $V_{LOTG}$ (region C).

The “knee” voltage, indicated in Fig. 4.5b as $V_{acc}$, corresponds roughly to the $V_{LOTG}$ at which the TG sub-threshold current ($I_{sub}$) [TN09] is comparable to $I_{junc}$. $V_{acc}$ can also be seen as the biasing voltage $V_{LOTG}$ at which the TG exits the accumulation mode. FWC variations can be modeled by introducing in (4.2) the contribution of $I_{sub} = I_{D0}e^{\frac{V_{LOTG}-V_{OC}-V_{T}}{m_{th}(T)}} + I_{sat}(1 - e^{-\frac{V_{OC}}{n_{th}}}) = 0 \tag{4.8}$

where $I_{D0}$ depends on TG geometrical and physical parameters, $m$ is the TG sub-threshold slope ($m > 1$) and $V_{T}$ is the TG threshold voltage (considering body effect). The effect of this sub-threshold current contribution can also explain the phenomena reported in [SBT13].

To highlight the effect of the different parameters, (4.8) can be expressed as a function of $V_{OC}$. In particular, as schematized in Fig. 4.5:

- In region A ($V_{LOTG} < V_{acc}$) $I_{sub}$ is negligible with respect to $I_{junc}$, thus:
  \[ V_{OCA} \approx 0 \tag{4.9} \]

- In region C ($V_{LOTG} > V_{acc}$) $I_{sub} >> I_{sat}$, thus:
  \[ V_{OCC} = V_{LOTG} - V_{T} - n_{th} \ln \left( \frac{I_{sat}}{I_{D0}} \right) \tag{4.10} \]

where to simplify the expression it is assumed that $n, m = 1^3$. Combining (4.9) and (4.10) with (4.4) gives, respectively:

\[ FWC_A(T) = EFWC(T) \tag{4.11} \]

\[ FWC_C(T) = EFWC(T) - \frac{1}{q} C_{PPD} (V_{LOTG} - V_{T}(T)) \tag{4.12} \]

\[ ^3 \text{This simplification is not used in the fitting model, where } m \text{ is calculated as } m = 1 + \frac{1}{q_{\text{ox}} \sqrt{\frac{\epsilon_{Si} q_{Na}}{4 \Phi_B}} \text{ [TN09]} \text{ and } n \text{ is set to } 1.75. \]
4.5. Dynamic behavior of the Full Well Capacity

where the ratio \( \frac{I_{sat}}{I_{D0}} \ll 1 \) has been neglected. Note that, in region C, the PPD can be reversed biased (\( V_{OC} > 0 \)).

In (4.12) only two parameters can vary with temperature: \( V_{pin} \) and \( V_T \). As the increase in the FWC with temperature shown in Fig. 4.6, is more or less constant at all TG biasing conditions, \( V_T \) variations with \( T \) can be neglected here.

The reasoning in dark conditions can be extended to illumination conditions by adding a constant photocurrent to (4.8). Figure 4.6 shows the FWC measured for two different photon fluxes as a function of \( V_{LOTG} \). If \( V_{LOTG} < V_{acc} \), the FWC is the same as in (4.7), whereas when \( V_{LOTG} > V_{acc} \), the FWC drops linearly with \( V_{LOTG} \). As expected from the previous sections, the FWC increases with \( \Phi \) and decreases with \( T \). It can also be observed that, as the temperature is increased from \( T = 343 \) K to \( T = 363 \) K, the FWC decreases more in region A (\( \Delta\text{FWC}_A \approx 2000 \ e^- \)) than in region C (\( \Delta\text{FWC}_C = 1200 \ e^- \)). This can be explained by the fact that the temperature dependence of \( I_{sat} \) and \( I_{D0} \) is not the same (in particular, for the biasing conditions in Fig. 4.6, \( I_{sat} \) is a stronger function of temperature than \( I_{D0} \)).

4.5 Dynamic behavior of the Full Well Capacity

In the previous sections it has been assumed that, at full well, the PPD is at equilibrium (case of EFWC) or in a pseudo equilibrium state where photo-generation within the SCR is compensated by charge diffusion toward the p-doped surrounding regions (\( J_{junc} \)) and eventually by the leakage of the TG (\( I_{sub} \)). However, if the operating conditions are suddenly changed, the time necessary to reach a new pseudo-equilibrium state can be much larger than the time between two acquisitions. This can lead to measurement uncertainty or to a wrong
interpretation of experimental results. In this section, a new analytical model to describe the
dynamic behavior of the FWC in non-stationary light conditions is presented and validated
with the support of experimental data.

Let us consider the response in terms of FWC to a light step at the instant \( t = t_0 \) between
two illumination levels (from \( \Phi_1 \) to \( \Phi_2 \)). It is assumed that, before the step, the PPD is at
pseudo-equilibrium and forward biased, with \( V_{OC} \) as in Eq. 4.6 and \( I_{junc} + I_{sub} + I_{ph}(\Phi_1) = 0 \).
At \( t = t_0^+ \), the photo-current suddenly varies from \( I_{ph}(\Phi_1) \) to \( I_{ph}(\Phi_2) \) and the PPD reaches a
new equilibrium condition. The time dependence of the amount of charge stored in the PPD
can be expressed as:

\[
\frac{\partial \text{FWC}(t)}{\partial t} = -\frac{1}{q} [I_{junc}(t) + I_{sub}(t) - I_{ph}(\Phi_2)]
\] (4.13)

In the following, to simplify the model as much as possible, \( C_{PPD} \) variations with \( V_{OC} \) are
neglected \(^4\). Under this assumption, and if \( \Phi_2 = 0 \), \( V_{OC} \) can be approximated to:

\[
V_{OC}(t) \approx \frac{q}{C_{PPD}} [\text{EFWC} - \text{FWC}(t)]
\] (4.14)

To simplify the analysis, \( I_{sub}(t) \) will also be neglected (for consistency, experimental data
have been obtained with \( V_{LOTG} = -0.5 \) V).

### 4.5.1 FWC behavior after a white-to-black light step

Let us consider a white-to-black light step (\( \Phi_1 > 0 \) and \( \Phi_2 = 0 \)), which corresponds to a PPD
charge drop from \( \text{FWC}(\Phi_1) \) to \( \text{EFWC} \). Since at \( t = t_0 \) the photo-current becomes zero, \( I_{junc} \)
is the only current contributing to the charge of the capacitance. In forward bias conditions,
\( I_{junc} \) can be expressed as the sum of two current contributions \( I_{junc} = A_{PPD} (J_{rec} + J_{diff}) \)
[TN09]:

\[
J_{rec} = \frac{q n_i W_{dep}}{2 \tau_0} \left( e^{-\frac{q V_{OC}}{kT}} - 1 \right)
\] (4.15)

\[
J_{diff} = \frac{q D_n n_i^2}{N_a L_n} \left( e^{-\frac{q V_{OC}}{kT}} - 1 \right)
\] (4.16)

where \( J_{rec} \) is the recombination current density within the SCR, with \( \tau_0 \) the minority carrier
life-time and \( W_{dep} \) the depleted depth and \( J_{diff} \) is the diffusion current density flowing from the
PPD toward the surrounding p-regions, with \( L_n \) and \( D_n \) the diffusion coefficient and diffusion
length, respectively. Figure 4.7 shows the \( J_{rec} \) and \( J_{diff} \) current densities as a function of \( V_{OC} \)
simulated in Matlab. As can be observed, \( J_{diff} \) is the dominant current density contribution
at large forward bias and is responsible for the FWC drop following the light step. At lower
forward voltages, \( J_{rec} \) becomes the main current contribution and is responsible for the final
decay of the FWC toward the EFWC. The figure also shows that as \( V_{OC} \) tends to zero, the

\(^4\)To take into account CPPD variations in forward biasing conditions, the reader can refer to section 2.2.6
in [TN09].

104
4.5. Dynamic behavior of the Full Well Capacity

Figure 4.7: Simulated diffusion and recombination currents densities as a function of $V_{OC}$.

current density drops of more than 5 orders of magnitude. This means that whereas a fast drop in the PPD charge is expected during the first instants following the light step, the time required to reach the EFWC regime can be very long.

The behavior of the FWC as function of time can be obtained from (4.14) as:

$$V_{OC}(t) = V_{OC}(\Phi_1) + \frac{1}{C_{PPD}} \int_0^{T_{int}} A_{PPD} J_{junc}(t) \, dt$$  \hspace{1cm} (4.17)

To observe experimentally the dynamic evolution of the PPD FWC, a light step has been applied by means of a LED placed 15 cm from the detector, which is operated in rolling shutter mode. The pulse intensity is adjusted so that the $Q_{PPD} > EFWC$. The light is first turned ON and 100 images are acquired to ensure that the device has reached pseudo-equilibrium, then the LED is turned off. The sequence is repeated, sweeping the integration time from 34 ms (corresponding to the minimum integration time in this configuration) to 60 s. The image acquired during a light step (LED from on to off) is shown in Fig. 4.8a. The top region (lines 1 to 20) corresponds to the lines which have been read while the LED was still on. In this region the FWC is equal to the FWC measured under steady illumination (pseudo-equilibrium condition); in the bottom region (line 20 to 40), there is a quick drop in the stored charge. The charge drop is due to the fact that charge transfer is performed for each line at increasing delays from the light step (as the device is operated in rolling shutter mode).

Figure 4.8b shows the FWC as a function of the time delay between the light step and the line acquisition. The time resolution is 135 $\mu$s, which corresponds to the time between the acquisition of two successive lines. As the time delay is increased, the FWC tends asymptotically toward a FWC of about 21 ke- which is close to the EFWC that can be extrapolated at room temperature in Fig. 4.2a. Therefore, as discussed in section 4.1, applying a light pulse can be a useful technique to rapidly fill the PPD for the estimation of the EFWC. Note however that an integration time of several tens of seconds must be used to avoid an overestimation of the EFWC. Nevertheless, this method is of great interest at room temperature (and below), where thermal generation can be well below $1 \, e^-/s/\mu m$ and for which integration times of...
several tens of minutes (or hours) are necessary to fill the PPD only with thermally generated charges.

Figure 4.9 shows $V_{OC}$ calculated as (4.14), plotted as a function of time (in logarithmic scale)$^5$. The figure also shows the slope of the curve as a function of time. As can be observed the slope reaches a first plateau at $-0.06 \ V/\text{decade}$ and then a second plateau at $-0.12 \ V/\text{decade}$. As indicated in the figure, these two different time constants can be associated to the two different regimes of $I_{junc}$. As can be observed, the model is able to reproduce the dynamic behavior of the FWC over 6 time delay decades. The small difference at very short delays can be explained by a very fast increase in $C_{PPD}$ at high forward biasing voltages (which is not taken into account in the model).

Figure 4.8: (a) Image acquired while the light is turned from ON to OFF. A sudden drop in the FWC can be observed after line 20, which corresponds to the last line to be readout before the LED is turned off. (b) Measured mean output charge as a function of the time delay between the light step and the line acquisition at $T = 300 \ K$ and $V_{LOTG} = -0.5 \ V$.

4.5.2 FWC behavior after a generic light step

The same reasoning can easily be extended to other light step conditions, by replacing $I_{junc} = A_{PPD}I_{junc}$ by the total current in the PPD. Figure 4.10 shows the simulated temporal evolution of $V_{OC}$ for different $\Phi_1$ and $\Phi_2$ light levels. As can be observed, when $\Phi_2 < \Phi_1$, the PPD potential drop has more or less a similar behavior, whichever $\Phi_2$, since for most of the transient, the photocurrent $I_{ph}(\Phi_2)$ is much smaller than $I_{junc}$. On the contrary, for a positive illumination step ($\Phi_1 < \Phi_2$), the photocurrent $I_{ph}(\Phi_2)$ is much larger than $I_{junc}$, which results at first in a linear increase of $V_{OC}$ (which is proportional to $I_{ph}(\Phi_2)$). As $I_{junc}$ becomes of the same order as $I_{ph}(\Phi_2)$, the transitory becomes slower and slower until

$^5$The best fit has been obtained for $C_{PPD} = 5.4 \ fF$, which is between the maximum ($7.5 \ fF$) and minimum ($4 \ fF$) PPD capacitance extracted in [Goi+14b] for the same pixel geometry at room temperature.
Figure 4.9: Measured and simulated $V_{OC}$ as a function of the delay between the light step and the line acquisition. Two regimes corresponding to two different time constants can be identified by observing the slope of $V_{OC}(t)$. These regimes are attributed to the diffusion of carriers from the PPD SCR to the surrounding p-regions and to charge recombination within the SCR, respectively. (b) Simulated diffusion and recombination currents as a function of $V_{OC}$.

it reaches pseudo-equilibrium. As a general rule, if illumination steps are large enough, the PPD charge transient corresponding to a negative light has a similar behavior, whichever the final illumination level (as its temporal evolution only depends on $I_{junc}$ and $V_{OC}$). On the other hand, the PPD discharge depends significantly on $\Phi_2$ and $\Phi_1$. In particular for a given $\Phi_1$, the initial PPD discharge transient is much faster as $\Phi_2$ is increased.

4.6 Conclusion

The PPD FWC is usually given as a fixed parameter on data sheets and its value is often used to compare different PPD designs. However, it has been shown that if the output signal is not limited by the readout electronics, the FWC strongly depends on the experimental conditions. In particular, as shown in Fig. 4.11, measured FWC can vary up to a factor 3 depending on the signal level, on the working temperature and on $V_{LOTG}$. These important variations can be explained by a simple current compensation reasoning, as the PPD will always tend toward an equilibrium (or pseudo-equilibrium condition) at which the total current charging (or discharging) the PPD capacitance becomes zero. The FWC model can also be applied to more complex pixel structures (such as 5T APS) on the condition that the additional current contributions (such as the sub-threshold current of the anti-blooming transistor) are taken into account. It has also been shown that opposite FWC temperature behaviors are observed in dark and illumination conditions, as both $V_{pin}$ and the dark current depend on the working temperature. In particular, the FWC increases with temperature in dark conditions whereas it drops with temperature under illumination conditions. These results show that FWC values are meaningless if the corresponding experimental conditions are not
Chapter 4. Static and Dynamic behavior of the Full Well Capacity

Figure 4.10: Mean sensor output signal plotted as a function of a normalized integration time (with respect to the charge generation rate) measured for different operating conditions. $\Phi_1 = 4 \times 10^{13}$ ph/s/cm$^2$, $\Phi_2 = 2 \times 10^{14}$ ph/s/cm$^2$. Unless specified, all measurements have been performed at $T = 333$ K and $V_{LOTG} = -0.5$ V. A.U. stands for Arbitrary Units.

Figure 4.11: Mean sensor output signal plotted as a function of a normalized integration time (with respect to the charge generation rate) measured for different operating conditions. $\Phi_1 = 4 \times 10^{13}$ ph/s/cm$^2$, $\Phi_2 = 2 \times 10^{14}$ ph/s/cm$^2$. Unless specified, all measurements have been performed at $T = 333$ K and $V_{LOTG} = -0.5$ V. A.U. stands for Arbitrary Units.
4.6. Conclusion

Based on this study, it is suggested to provide two main figures of merit during device characterization:

- The EFWC, which is the only parameter truly related to the PPD physical parameters (such as $V_{\text{pin}}$).

- The minimum $V_{\text{LOTG}} = V_{\text{acc}}$ biasing voltage which allows implementation of an anti-blooming function.

The dynamic behavior of the FWC has also been studied. In particular it has been shown that the PPD potential does not change instantly when the signal is suddenly changed and that the potential transient can last several tens of seconds before a new equilibrium is reached. This result is of great importance for applications such as Time of Flight applications, where pulsed light illumination is involved. In particular, to avoid measurement uncertainties when using PPD CIS detectors for such high temporal resolution applications, it is important to ensure that the PPD is always reverse biased during the device operation (i.e. that the maximum measured output charge remains below the EFWC). These considerations are also valid for PPD image lag characterization methods, which are often based on pulsed light.

New studies have been published based on this work. In particular, in [Cao+15] the models developed in this thesis have been used as a starting point to develop a more detailed model of the PPD capacitance, in [Goi+14b]; [Cha+14]; [XGT15]; [Inn15] they are used to study other PPD parameters, such as the pinning voltage and the PPD capacitance, whereas in [Goi+14a] they are used as a tool to identify the cause of performance degradation after exposure to radiations. Finally, in [FH14]; [Zuj+15]; [MC+15] the FWC model proposed in this work is used as a reference when addressing the signal dependence of the PPD FWC.
Conclusion and Outlook

This thesis presented a study on key design parameters in Pinned Photodiode CMOS Image Sensors for high temporal resolution applications. The work was focused on what these parameters represent (physical definition), on how they are affected by experimental conditions and how they can/should be measured. Whenever possible, this has been done by developing appropriate analytical models.

A novel PPD pixel topology, referred to as Storage Gate (SG) pixel, has been proposed in this work for the monitoring of charge transfer performances. The measurement principle consists in electrically injecting a packet of charge at the far end of the PPD at increasing delays with respect to the falling edge of the TG signal. These pixels allow comparison of different pixel geometries in terms of CTI at both the same initial charge density and initial amount of carriers. Measurements performed on SG pixels with PPD lengths going from $2\ \mu m$ to $32\ \mu m$ have shown that charge transfer can be much slower than the time predicted by simply solving diffusion equations. These results are attributed to the presence of design traps (such as potential bumps or potential pockets) located at the TG-PPD interface, which significantly slow down the transfer of charge, even for the longest tested PPDs. The most straightforward solution to improve transfer time in barrier limited pixels, is either to increase the TG biasing voltage during charge transfer (which can however lead to charge partition phenomena) or to keep electrons close to the TG during transfer, for example by adding a collection well (region presenting a larger $V_{\text{pin}}$) close to the TG. This approach is a currently adopted solution to artificially reduce the effective PPD length, while maintaining a large active area.

An analytical analysis of charge trapping phenomena under the TG has been carried out. In particular, it has been shown that the probability of electron trapping under the TG during charge transfer is very low. However, based on a similar reasoning, it is suggested that interface states can indeed affect the output signal. In particular, as discussed in [Jan+15], electrons can recombine with holes that have been trapped under the TG during the integration time (which is often of the order of several ms) and that are released as soon as the TG is turned on. Note that such phenomena do not lead to image lag but to non-linearities due to a reduction of the device effective quantum efficiency (which depends on the signal-level).

A second topic addressed in this thesis concerns the definition, the modeling and the estimation of the pinning voltage ($V_{\text{pin}}$) in PPD CIS. As discussed in the second chapter of this work, two different definitions are used in the literature when referring to the pinning voltage. It is sometimes defined as the maximum deviation of the electron quasi-Fermi level ($\Delta E_{\text{fnmax}}$), which is the most commonly used definition in publications, or as the maximum variation of the electrostatic potential ($\Delta\Phi_{\text{max}}$) with respect to equilibrium, which is often used to estimate $V_{\text{pin}}$ from TCAD simulations. It is important to note that because of the thermionic emission of carriers from the TG channel toward the PPD, the condition at which the PPD potential reaches $\Delta\Phi_{\text{max}}$ does not correspond to a full depletion condition. In this
work, \( V_{\text{pin}} \) is nevertheless defined as \( \Delta \Phi_{\text{max}} \), since it represents the PPD potential floor. As emphasized in this work, monitoring \( \Delta E_{\text{fnmax}} \) can also be of great interest as it represents the minimum TG channel potential that must be applied to fully empty the PPD.

The second chapter of this work also addressed the problem of reliable and comparable measurements of the absolute value of \( V_{\text{pin}} \). In the CIS community, \( V_{\text{pin}} \) is both estimated from in-pixel measurements and from electrical measurements performed on isolated test-structure (or test-structure arrays). Among the methods addressed in this work, only the square root method [SD82] and the in-pixel method[TBT12] have proven to be reliable approaches for the estimation of the absolute value of \( V_{\text{pin}} \). It is demonstrated, both with simulations and experimental data, that test structure methods which are based on the simplifying assumption of a on-off behavior of JFETs, such as the floating source methods [Cou09] or the current method [PU09], only allow observation of relative variations of \( V_{\text{pin}} \) (as the absolute measured value depends on the experimental set-up). In-pixel measurements provide an estimation of \( V_{\text{pin}} \) in a real pixel environment and on large pixel arrays (good statistics). They also also to estimate other parameters, such as the PPD capacitance, the EFWC, \( \Delta E_{\text{fnmax}} \) and the TG channel potential during transfer. However, fewer design and geometrical variations can be tested with respect to the test-structure techniques. Therefore, the two approaches should be considered complementary.

Transfer speed can be enhanced (with respect to a simple diffusion regime) by inducing a drift field (i.e. by bending the PPD potential). The maximum theoretical potential drop that can be generated within the PPD is equal to the \( V_{\text{pin}} \) which would be measured in a large photodiode (referred in this work as the intrinsic pinning voltage). As shown in the literature, changing the PPD minimum size leads to a modulation of the PPD potential (geometrical modulation), thus triangular or trapezoidal PPDs can be designed to drift electrons toward the TG. Despite the fact that this method involves strong geometrical constraints, it is fairly simple to implement and have been proved in the litterature to be very effective in speeding up the transfer process. However it is not the most suitable solution for multi-tap PPD pixels, since the generated electric field is static. Note also, that with respect to the (simpler) solution based on the reduction of the effective PPD transfer length by means of a deeper collection well located close to the TG, the geometrical modulation approach is of great interest when the device is not operated in integration mode (or when the integration time is very short, so that carriers do not have time to reach the well before the beginning of charge transfer).

A different approach, proposed in [Han+14], consists in generating a dynamic electric field by changing the bias applied to pairs of lateral gates. This method is referred to as Lateral Electric Field Modulation (LEFM). It has been shown, by means of a test-array designed in a commercially available PPD CIS technology, that LEFM enables a good charge orientation efficiency only for very narrow pixels (below 2 \( \mu \)m), however in dynamic operation, because of the limited electric field that can be generated with this method, the CTI is only slightly improved with respect to standard photodiodes (less than a factor 1.5). Since the LEFM approach involves significant geometrical constraints and a worsening in both the fill-factor and the dark current performances, this method is of interest only when the application specifically requires a dynamic orientation of charges.
An alternative approach to obtain a dynamic electric field in BSI devices while releasing the geometrical constraints, could be to modulate the PPD potential by means of metal electrodes located above the Pre-Metal Dielectric (PMD) or simply by adding poly-silicon gates over the PPD. Note that to modulate the PPD potential from “above” the pinning implant must be first inverted, which means that its potential is un-pinned and therefore the PPD potential can be higher than $V_{\text{pin}}$. The resulting device would be a “temporary pinned” device$^6$. This approach cannot currently be implemented with the available commercial technologies, since the biasing potential required to invert the pinning implant is of several hundreds of Volts (due to the very high doping concentration of the p+ implant). In addition, PPDs implants cannot generally be designed below poly-gates in standard CIS technologies.

This work also showed that the full well capacity (FWC), which is often given as a fixed value in imagers data-sheets, can be strongly dependent from the experimental conditions. A simple analytical model has been developed to predict the behavior of the FWC depending on the working temperature, on the biasing conditions and on the impinging photon flux. It has been shown, that in the dark with the TG in accumulation mode, the PPD charges can increase up to a value which only depends on the PPD capacitance and on $V_{\text{pin}}$. This key FWC level is referred to as Equilibrium Full Well Capacity (EFWC) and has been introduced for the first time in this work. If the TG is accumulated during light integration, the amount of electrons stored in the PPD under illumination can become larger than the EFWC. As emphasized in this work, under illumination, when reaching the full well pseudo-equilibrium (corresponding to an open circuit condition) the PPD can be forward biased. This thesis also showed, with respect to previous works, that the FWC level increases logarithmically with the photon flux even when the TG is accumulated, due to the forward current of the photodiode (previously this behavior was mainly attributed to the TG sub-threshold current). It has been shown in the literature that if the TG is positively biased during integration, excess charge is drained away toward the FD and the FWC drops linearly with $V_{\text{LOTG}}$. Finally, this thesis also showed that different FWC temperature behaviors can be observed depending on the operation conditions. In particular, if the PPD is forward biased (i.e. under illumination), an increase in temperature results in a decrease in the FWC. On the other hand, in the dark, the FWC increases with temperature due to an increase of $V_{\text{pin}}$. These results are very important as they show that FWC values are meaningless if the experimental conditions are not specified and that the only parameter that really characterizes a pixel is its EFWC.

The dynamic behavior of the FWC has also been investigated. It has been shown that if the illumination level is suddenly changed, the PPD does not immediately reach the new corresponding pseudo-equilibrium condition. The smaller the final photon flux, the smaller the forward current of the photodiode and thus the longer the transient to reach pseudo-equilibrium. This means that unless the integration time and the PPD EFWC are sized to ensure that in typical working conditions the PPD charge is below the EFWC, significant errors can affect the output signal if the imaged scene is not still. These considerations can also be extended to image lag characterization methods (which are often based on a pulsed light source), where the pulse width and intensity must be chosen so that the PPD is never forward biased (PPD charge below the EFWC).

$^6$Note that both solutions would lead to a significant increase of the dark current.
To conclude, the models developed in this work can be useful tools to study and optimize PPD CIS pixels. The proposed charge transfer model, associated to measurements on pulsed SG pixels, can help identifying the phenomena limiting charge transfer for a given technology or pixel design. To further improve the model, it would be of great interest to also account for charge trapping phenomena under the TG in the numerical simulation. The FWC model has already been used in the literature as a reference when addressing the effect of the photon flux on the FWC [FH14]; [Zuj+15]; [MC+15] or as a starting point to further investigate (or model) other PPD parameters [Goi+14b]; [Cha+14]; [Cao+15]; [XGT15]; [Inn15]. In [Goi+14a], EFWC variations have been used to investigate the radiation hardness of PPD pixels. Characterization methods from 3T CIS have often been transferred “as they are” to PPD CIS, however as emphasized in this work, new indications and methods should be developed in order to standardize the estimation of figures of merits such as the CVF, the FWC and the pinning voltage. In particular, as discussed in appendix B, much remains to do concerning CVF noise-based methods, such as the mean variance method, which could be re-adapted to take into the specific operation principle of PPDs and take into consideration only the noise contributions which are specific to PPD CIS.


Bibliography


Bibliography


Bibliography


122
<table>
<thead>
<tr>
<th>Reference</th>
<th>Description</th>
</tr>
</thead>
</table>
Since PPD pixels with multiple transfer steps (such as in [YIK10]) were not available, in this work, global shutter readout mode has been implemented by using the FD as the storage node and by acquiring the reference and the signal with two separate images. The corresponding timing diagram is shown in Fig. A.1.

For a large pixel array, this timing diagram implies that both the reference and the signal are stored on the FD for an amount of time, which varies depending on the pixel position, in particular the sampled charge will be held much longer for the pixels of the last line with respect to ones of the first line. If the FD presents a non negligible leakage current, the signal of the last readout pixels can be highly over-estimated.

Figure A.2 shows the leakage current $I_{\text{leakFD}}$ of the FD measured in the dark and under illumination, for different $V_{\text{DDRST}}$ biasing voltages, as a function of the TG off biasing potential $V_{\text{LOTG}}$. The leakage current has been calculated from the variation of the output voltage as a function of time. The tested device is detailed in section 2.3.2.

Similar behaviours are observed in dark conditions and under illumination, except for an
offset in the measured output current due to the parasitic light sensitivity of the FD. As shown in the figure, for slightly positive $V_{\text{LOTG}}$, $I_{\text{leakFD}}$ does not depend on $V_{\text{LOTG}}$. This means that when the TG is not accumulated (and not yet inverted) the current discharging the FD is mainly due to thermally generated carriers (dark current) and eventually to the collection of photo-charges by the FD. It can also be observed that $I_{\text{leakFD}}$ increases as the TG biasing potential becomes more negative and for higher $V_{\text{DDRST}}$ values. As suggested in [Yam+09], the origin of this additional leakage current contribution in accumulation mode (of the order of $10 \text{ fA} - 20 \text{ fA}$ here) is similar to the one observed in 3T APS in [Pai+05b], which is referred to as Gate-Induced-Leak Trap Assisted Tunnelling (GIL-TAT) in [Yam+09], or more commonly as Gate Induced Drain Leakage (GIDL) current [Mar81]; [NVB89]; [TN09]. GIDL is due to the increase in the local electric field in the overlap region between the n+ implant of the FD and the TG (which, as shown by the TCAD simulations in Fig. A.3, can be of the order of $10^6 \text{ V/cm}$ and is an exponential function of $V_x = V_{\text{ch}} - V_{\text{fd}}$ [Yam+09]; [Lou+03], where $V_{\text{ch}}$ is the channel potential on the FD side.

In rolling shutter mode, the RST, SHR, TG and SHS signals are very close to each other (few $\mu s$ between RST and SHS), thus the TG can be biased in accumulation mode to reduce the PPD dark current [MST08] as the effect of GIDL on the output signal can be neglected. However, as shown in this section, this biasing condition should be avoided in charge domain global shutter mode. To reduce the GIDL, it is also recommended to use hard reset instead of soft reset and to minimize the overlap between the FD n+ implant and the TG while designing the pixel.

1The FD is normally screened by means of metal layers, but photocharges generated in the epitaxy can diffuse toward the FD.
Figure A.3: TCAD simulation of the current density and electric field at the FD-TG interface for different $V_{LOTG}$ biasing voltages (with $V_{FD} = 3.3V$).
Estimation of the Charge to Voltage conversion Factor in PPD CIS

The Charge to Voltage conversion Factor (CVF) is defined as the ratio between the variation of the output voltage $\Delta V_{\text{out}}$ and the number $N$ of electrons collected at the FD:

$$CVF = \frac{\Delta V_{\text{out}}}{N_{e^{-}\text{FD}}}$$  \hspace{1cm} (B.1)

where $V_{\text{out}} = G \times V_{\text{FD}}$, with $G$ the gain of the readout chain. The CVF is usually expressed in $\mu V/e^-$ or in ADU/e$^-$. 

The Quantum Efficiency (QE) gives the amount of the total photon flux $\Phi$ on the pixel surface that participates to the pixel photocurrent $I_{\text{ph}}$. If we assume that each absorbed photon generates an electron-hole pair, at that the impinging photons are mono-energetic, then the QE can be expressed as the ratio between the number of impinging photons $N_{\text{ph}}$ and the number $N_{e^{-}\text{PPD}}$ of photo-electrons collected by the photodiode:

$$QE = \frac{I_{\text{ph}}}{\Phi} = \frac{N_{e^{-}\text{PPD}}}{N_{\text{ph}}}$$  \hspace{1cm} (B.2)

A method for the estimation of the QE in 3T APS is presented in [Fow+98].

To simplify the expressions, it will be assumed in the following that $G=1$ and that $\Delta V_{\text{out}} = \Delta V_{\text{FD}} = V$. If we also assume that $N_{e^{-}\text{PPD}} = N_{e^{-}\text{FD}} = N_{e^-}$ (100% CTE), the QE and the CVF determine the overall photon to voltage conversion gain and their product gives the slope of the Electro-Optical Transfer Function (EOTF) $V(N_{\text{ph}})$:

$$\frac{dV(N_{\text{ph}})}{dN_{\text{ph}}} = CVF \times QE$$  \hspace{1cm} (B.3)

It is sufficient to estimate one of the two parameters to derive the other from the EOTF.

If we approximate the FD capacitance to a constant capacitance $C_{\text{FD}}$, the variation of the output voltage can be expressed as:

$$\Delta V = \frac{q \times N}{C_{\text{FD}}}$$  \hspace{1cm} (B.4)
Appendix B. Estimation of the Charge to Voltage conversion Factor in PPD CIS

Which gives:

\[
CVF = \frac{q}{C_{FD}} \quad (B.5)
\]

The precise knowledge of \( C_{FD} \) would allow estimation of the conversion factor. In practice, due to parasitism, the real floating diffusion capacitance cannot be easily estimated and indirect methods are used instead.

Before discussing the different methods used in the CIS community to estimate the CVF in 3T APS and their limitations when applied to PPD CIS, it is important to make a distinction between two different saturation mechanisms:

A) The electronic circuit saturates long before the output charge reaches the FWC of the photodiode: in this case the QE can be considered constant over the whole output voltage range. If we approximate the PPD SCR to the depletion region of an abrupt one-sided p-n junction, the capacitance \( C_{dep} \) of the depletion region can be expressed as a function of the FD potential as \([TN09]\):

\[
C_{dep}(V) = \frac{q\epsilon_{Si}}{W_{dep}(V)} = \frac{q\epsilon_{Si}}{\sqrt{\frac{2\epsilon_{Si}N_A+N_D}{qN_AN_D}}} (V_{bi} - V)
\]

where \( W_{dep}(V) \) is the extension of the depleted region, \( V_{bi} \) the built in voltage, \( \epsilon_{Si} \) the Silicon dielectric constant and \( N_A \) and \( N_D \) the doping levels of the n-type and the p-type regions, respectively. Because of this non linearity the CVF is signal dependent and drops toward saturation.

B) The diode FWC is reached long before the saturation of the electronics: in this case the CVF is constant over the whole output voltage range (since the FD is always in its linear region). On the other hand, the QE drops as the diode approaches its full well, as less and less charges can be collected by the PPD.

In 3T APS the saturation of the maximum output signal is limited by the saturation of the readout chain (saturation mechanism A). In PPD pixels, the saturation mechanism depends on the ratio between \( C_{FD} \) and the PPD capacitance \( C_{PPD} \). If \( C_{PPD} \) is much larger than \( C_{FD} \), the saturation of the output signal is limited by the electronics (saturation mechanism A). However, with pixel-size shrinking, the PPD FWC can be much smaller than the charge required to saturate the readout chain, resulting in the saturation mechanism described in B. The following section discusses three estimation methods that are commonly used in the CIS community to estimate the CVF in 3T APS and their limitations when applied to PPD CIS. More methods for the estimation of the CVF in 3T APS can be found in \( [Boh+08] \).

B.1 The mean variance method

The mean variance method is the most widespread approach for the estimation of the CVF in both CCDs \([Sta+92]\) and CIS \([BF96]\). The method is based on the assumption that the
B.1. The mean variance method

detector response is linear, hence that the number of electrons $N_{e-}$ collected at the FD can be calculated from the mean output signal $V$ as:

$$N_{e-} = QE \times N_{ph} = \frac{V}{CVF}$$  \hspace{1cm} (B.7)

It is also assumed that for good quality detectors, the noise is dominated by photon noise, which follows Poisson statistics:

$$\sigma_{N_{e-}}^2 = N_{e-}$$  \hspace{1cm} (B.8)

Under these simplifying hypotheses, it can be demonstrated [BF96] that the mean output voltage variance $\sigma_V^2$ can be expressed as a function of the mean output signal $V$ and of the CVF as:

$$\sigma_V^2 = V \times CVF$$  \hspace{1cm} (B.9)

As a result, the CVF can be estimated as the slope of the Photon Transfer Curve (PTC), which corresponds to $\sigma_V^2$ plotted as a function of $V$.

Figure B.1a shows the EOTF and PTC measured on a 256 x 256 PPD pixel-array designed at ISAE. The curves have been obtained by using a constant integration time and an increasing photon flux. The array is read both in 3T mode and 4T mode (timing diagrams in Fig. B.1b and B.1c, respectively). As it can be observed, the EOTF is linear at low signal levels for both readout modes and the slope of the PTC (and thus the CVF calculated with the MV method) remains more or less constant. For both readout modes again, the EOTF is less and less linear toward higher signal levels and toward saturation we observe a drop of the PTC.

In 3T readout mode, the linear range mainly depends on the design of the readout electronics and the noise drop is due to the fact that as the saturation point is approached, less and less noise is added by photon statistics (which eventually drops to zero). By comparing the two EOTF curves and the two PTC, three main observations can be made:

- The saturation voltage in 4T mode is below 400mV, where the FD is still in its linear range. It can be inferred that in 4T readout mode the CVF is constant over the whole output range and that the saturation of the EOTF is to be attributed to a drop in the QE.

- In 4T readout mode, even after saturation, the EOTF keeps increasing as the photon flux is increased. As discussed in chapter 4, this behaviour is due to the fact that under illumination, the PPD full well capacity is reached in forward biasing conditions. In particular, it is shown that the open circuit voltage (saturation voltage) depends on the photocurrent and thus on the photon flux.

- In 3T mode, the drop in the PTC roughly corresponds to the output voltage at which the EOTF exits the linear region. In 4T readout mode however, the PTC drops while the EOTF is still in its linear range (250 mV here). Since the CVF is constant and the output signal is not affected by the saturation of the electronics, this second noise drop

\[\text{1}^1\text{Thus as long as the output voltage is far from saturation, the linearity hypothesis of the MV method is valid for both 3T and 4T readout modes}\]
Appendix B. Estimation of the Charge to Voltage conversion Factor in PPD CIS

mechanism could be attributed to a drop in the QE. This phenomenon is not further investigated here and a detailed analysis of the PTC in PPD CIS is left for future studies.

![Graphs showing EOTF and PTC](image)

Figure B.1: EOTF and PTC measured on a 256 × 256 PPD pixel array designed at ISAE in 3T (c) and 4T (d) readout modes. In 3T readout mode, the TG is always accumulated (\(V_{TG} = -0.4\) V). A CVF of about 40 \(\mu V/e^-\) can be estimated for this detector.

Since the CVF is extracted from the PTC slope at low signal levels, where both QE and \(C_{FD}\) variations can be neglected, the MV method is suitable for both 3T APS and PPD CIS (whatever the saturation mechanisms). In both cases, the MV fitting range must be set very carefully, since the PTC slope is not constant even at low signal levels [Jan01]. In particular, choosing a fitting range which is too large leads to an underestimation of the CVF (as the PTC slope drops toward saturation), whereas choosing a fitting range which is too small reduces the accuracy in the estimation of the PTC slope (as the measurement is significantly affected by the readout noise). The MV method has the great advantage of being simple and does not require heavy computations. On the other hand the signal range for which all
B.2. Non Linear Estimation method

hypotheses are valid is limited and depending on the chosen fitting range, very different CVF values can be extracted.

B.2 Non Linear Estimation method

In 2003, to overcome the limited range of validity of the MV method, B. Pain and B. Hancock proposed an alternative algorithm, which is also based on a noise analysis, but removes the hypothesis of linearity of the sensor [BF96]. This method, referred to as Non Linear Estimation (NLE) method, allows calculation of the CVF at all signal levels under the hypothesis of a constant QE. In particular, for 3T APS, it can be demonstrated that the output voltage variance can be expressed as the sum of the contributions of the electronic voltage readout noise, of the electron photon noise and of the electron reset noise as:

\[
\sigma_{\text{Vout}}^2 = \sigma_{\text{Vread}}^2 + \left(\text{QE} \times N_{\text{ph}} + \sigma_{\text{e-RST}}^2\right) \left(\frac{dV(N_{\text{ph}})}{dN_{\text{ph}}} \frac{1}{\text{QE}}\right)^2
\]

(B.10)

where \(\frac{dV(N_{\text{ph}})}{dN_{\text{ph}}} \frac{1}{\text{QE}} = CVF\). The equation can be rewritten as:

\[
Y = b + m_1 x_1 + m_2 x_2
\]

(B.11)

where \(Y = \sigma_{\text{Vout}}^2\), \(x_1 = \left(\frac{dV(N_{\text{ph}})}{dN_{\text{ph}}}\right)^2 \times N_{\text{ph}}\) and \(x_2 = \left(\frac{dV(N_{\text{ph}})}{dN_{\text{ph}}}\right)^2\). The electronic noise, the reset noise and the quantum efficiency can be estimated as the coefficients of the multivariate linear regression that better fits equation (B.11) (\(\sigma_{\nu}^2 = n, \text{QE} = \frac{1}{m_1}\) and \(\sigma_{\text{e-RST}}^2 = m_2 m_1^2\)).

The conversion gain is then derived as:

\[
CVF = \frac{V'(N_{\text{ph}})}{\text{QE}} = V'(N_{\text{ph}}) \times m_1
\]

(B.12)

This method is in fairly good agreement with the MV method for the estimation of the CVF within the EOTF linear range and provides useful additional information on the behavior of the CVF toward saturation in 3T APS. However, the initial hypotheses on which the whole mathematical development is based, do not apply to PPD CIS. On one hand, if the PPD saturates before the electronics, the CVF is almost constant in the whole output range, whereas the QE is signal dependent. Furthermore the noise contributions considered in this method are specific to 3T APS. To apply this approach to PPD CIS, the algorithm and the simplifying hypotheses must be adapted in order to take into account the saturation mechanism and the PPD noise contributions (which means neglecting the reset noise, adding the transfer noise [Fos03] and studying the noise filtering resulting from reduction of the QE toward saturation and from the PPD forward biasing conditions under illumination).
B.3 X-ray method with Fe$^{55}$

A completely different approach to the problem is given by the x-ray method [Jan01]; [HGP04], which is based on our a priori knowledge of the interaction of soft x-rays (up to 10 keV) with Si. In this energy range the absorption is dominated by the photoelectric effect. The average number of electron-hole couples generated in the process is:

$$N_{eh} = \frac{E_{ph}}{\epsilon_{couple}}$$  \hspace{1cm} (B.13)

where $E_{ph}$ is the x-ray photon energy, $\epsilon_{couple}$ is the mean energy required to produce an e-h pair (around 3.65 eV for Si at room temperature). The Fe$^{55}$ is an unstable isotope that decays into Mn, emitting $K_{\alpha}$ (5.899 KeV) or $K_{\beta}$ xrays (6.490 KeV). Following Eq. B.13, the average number of electrons generated in Si will be $N_{e-} \approx 1616$ for $K_{\alpha}$-rays and $N_{e-} \approx 1778$ for $K_{\beta}$-rays. In [Jan01], Janesick estimates the diameter of the generated electron-hole cloud to be less than 1 $\mu$m. If all the generated electrons are successfully collected at the FD, the corresponding change in the output signal is:

$$\Delta V = N_{eh} \times \text{CVF}$$  \hspace{1cm} (B.14)

The conversion factor can thus be calculated as the ratio between the output voltage $V$ and the number of electrons that are generated during the absorption of the x-ray. Since the emission of $K_{\alpha}$ rays is 7 times more probable than the emission of $K_{\beta}$ rays, the first are used to evaluate the CVF and the second to validate it. In a 3T APS, if the ray is absorbed within the depletion region, or at a distance from it which is smaller than the diffusion length, it can be assumed that all the generated electrons are collected at the floating diffusion. The absorption length, defined as the distance where statistically 65% of the impinging photons are absorbed, can be calculated from the attenuation coefficient $\mu_{abs}$ as:

$$L_{abs} = \frac{1}{\mu_{abs} \rho}$$  \hspace{1cm} (B.15)

with $\rho$ the density of the absorption mean. Referring to the NIST data base (http://physics.nist.gov/PhysRefData/Xcom/html/xcom1.html), the absorption coefficient for a photon of 6 keV is around 14.7 cm$^2$/s, while the Si density is 2.33 g/cm$^3$, which results in an absorption length of about $L_{abs} = 30 \mu$m . Given the large absorption length when compared to the width of the depletion region, the probability of having all the electrons collected by one single pixel is quite low. Hence, once the photon is absorbed, electrons can recombine before being collected, or can be collected by neighbor pixels, creating the so called split and partial events. Figure B.3 shows a typical Fe55 x-ray histogram, with a high $K_{\alpha}$ peak, a smaller $K_{\beta}$ peak and the tail due to split and partial events. The high peak toward lower energies is due to non-interactions or re-combinations. More details on the method and a discussion on its limitations in terms of energy resolution can be found in [Jan01].

Like the MV method, the Fe$^{55}$ method allows to calculate the CVF at a single output charge value. If the saturation charge is much larger than 2000 e$^-$, the estimated CVF should
B.3. X-ray method with Fe\textsuperscript{55}

be comparable with the one estimated with the MV method. However if the number of
electrons generated by the x-ray approaches the saturation charge, results should be handled
with particular care, as the CVF drops quickly in this region and small charge collection
variation can results in large CVF value variations.

A first disadvantage of this method consists in the large amount of images (several hundred
thousand) that must be acquired, processed and stored to have good statistics, due to the
very low probability of $K_\alpha$ events. To partially overcome this limitation, it is recommended
to perform a “live event detection”, by setting a detection threshold. For the integration
time, the choice strongly depends on the available memory space and how data are going to
be processed. Using an integration time which is too long, increases the dark noise and the
risk of having more than one event per pixel (which leads to peak blurring). On the other
hand, choosing an integration time which is too short can result in an image output rate
which might not be compatible with live event detection.

An additional difficulty is due to the presence of RTS pixels [GVM11]; [Vir+13], which
introduce false events. Finally, a last limitation of the implementation of this method for
PPD CIS is the effect of charge lag. In particular, measurements performed on a pixel array
designed at ISAE, have shown that there is a good match between the CVF value extracted
with the MV and Fe\textsuperscript{55} methods for pixels presenting low image lag, whereas no peak could
be individuated when pixels presented high image lag. This result can be explained by the
fact that the amount of charge lag is not deterministic, which leads to a strong spread of the
$K_\alpha$ peak. These considerations can be extended to 3T-pixels, which often have smaller CVF
values and for which it might be of interest to use hard reset to minimize the effect of image
lag on the estimated CVF value.

Figure B.2: Illustration of the interaction of a Fe\textsuperscript{55} x-ray with a PPD.
Appendix B. Estimation of the Charge to Voltage conversion Factor in PPD

Figure B.3: Example of pixel histogram acquired at $T = -20^\circ C$ for an integration time of 10s and a detection threshold of 45 mV (applied after the substraction of the dark image).
C.1 Flick’s law derivation from probability calculations

This section presents the derivation of Flick’s diffusion law in 1D from probability calculations.

Let us consider the random walk of a set of carriers. After each time step $\Delta t$, electrons can move with a probability of $p = 1/2$ either of $+\Delta x$ or $-\Delta x$. Given a walkers distribution at a time $t_0$, the number of carriers $n$ located at $x = x_0$ after a time step $\Delta t$ can be expressed as:

$$n(t_0 + \Delta t, x_0) = \frac{1}{2} n(t_0, x_0 - \Delta x) + \frac{1}{2} n(t_0, x_0 + \Delta x) \quad (C.1)$$

The Taylor expansion of the three terms of the expression above are

$$n(t_0 + \Delta t, x_0) = n(t_0, x_0) + \frac{\partial n}{\partial t}(t_0, x_0)\Delta t + \frac{1}{2} \frac{\partial^2 n}{\partial t^2}(t_0, x_0)(\Delta t)^2 + \ldots \quad (C.2)$$

$$\frac{1}{2} n(t_0, x_0 - \Delta x) = \frac{1}{2} n(t_0, x_0) + \frac{1}{2} \frac{\partial n}{\partial t}(t_0, x_0)(-\Delta x) + \frac{1}{4} \frac{\partial^2 n}{\partial t^2}(t_0, x_0)(-\Delta x)^2 + \ldots \quad (C.3)$$

$$\frac{1}{2} n(t_0, x_0 + \Delta x) = \frac{1}{2} n(t_0, x_0) + \frac{1}{2} \frac{\partial n}{\partial t}(t_0, x_0)(\Delta x) + \frac{1}{4} \frac{\partial^2 n}{\partial t^2}(t_0, x_0)(\Delta x)^2 + \ldots \quad (C.4)$$

By combining equations C.1, C.2, C.3, C.4, neglecting terms of order higher than 2 and dividing by $\Delta t$ we obtain:

$$\frac{\partial n}{\partial t}(t_0, x_0) = \frac{(\Delta x)^2}{2\Delta t} \frac{\partial^2 n}{\partial t^2}(t_0, x_0)(\Delta x)^2 \quad (C.5)$$

Assuming that

$$\Delta t \to 0, \Delta x \to 0, \text{ and } \frac{(\Delta x)^2}{2\Delta t} \to D > 0 \quad (C.6)$$

we obtain again the diffusion law:

$$\frac{\partial n}{\partial t}(t_0, x_0) = D \frac{\partial^2 n}{\partial t^2}(t_0, x_0) \quad (C.7)$$
Appendix C. Charge transfer modeling and simulation: theoretical derivations and codes

Figure C.1: Analytical and numerical solution of C.8 compared to the Montecarlo simulation of the random walk of electrons (with $N = 1000e^-, D_n = 13 \text{ cm}^2/\text{s}$). The plotted solution corresponds to $t = 1 \text{ ps}$

C.2 Calibration of the simulation of charge diffusion in the PPD

In order to calibrate the numerical simulation of charge transfer in PPD CIS, at first a 1D diffusion in an endless mean starting from a delta like charge distribution has been simulated. Two different simulations have been implemented:

- Numerical solution of the diffusion equation
- Montecarlo simulation of the random walk of a set of electrons

The outputs have been compared to the analytical solution that can be found in [SN85] (with the omission of the recombination term).

$$u(x,t) = \frac{N'}{\sqrt{4\pi D_n t}} e^{-\frac{x^2}{4D_n t}}$$  \hspace{1cm} (C.8)

where $N'$ is the charge density per unit area, $t$ is the diffusion time and $x$ is distance covered by electrons during the diffusion process. Carrier generation has been neglected.

As shown in figure C.1, both the numerical solution of Flick’s law and the random walk are in good agreement with the analytical solution. Below, the Matlab@code used for the calibration:

1 \hspace{1cm} \% solution of the diffusion equation
2 \hspace{1cm} \% du/dt=D*d^2 u/d x^2

138
C.2. Calibration of the simulation of charge diffusion in the PPD

% with x belong to \([-\infty, +\infty]\) and an initial delta

% like distribution \(u(x,0)\)

% boundary conditions : \(u(-\infty,t)=u(+\infty,t)=0\);

close all; clear all;

% --- definition of physical constants
uth=0.025; %V
\(m_n=2.366\times10^{-31}\); %1/kg
q=1.6\times10^{-19}; %C
vth=2.30\times10^{05}; %m/s
un=500*1e^{-4}; %m^2/V/s
\(\tau_{\text{scat}}=un*m_n/q\); %s scatter time vector
mfpath=tau_scat*vth; %m avarage mean free path
\(D_n=uth.*un\); %m^2/s;
L=1e^{-6};

% --- Define simulation constants
\(t_{\text{max}}=5e^{-12}\); %maximum simulation time
dx= mfpath/2; %spatial step
\(n_x=\text{round}(L/dx)+1\); % number of nodes in x direction
\(\sigma=0.25\); %condition cfl \(\sigma<0.5\)
tstop=1e^{-12};

dt = dx*dx*sigma/D_n; %time step diffusion

nt = round(tmax/dt+1); % number of time steps
\(\%\)coef for the space centered, time forward
\(\%\)numerical diffusion simulation
\(r=D_n*dt/(dx^2)\);
\(r_2 = 1 - 2*r;\)

% --- variable initialization
\(\%\)initial number of charges in each bin with \(u!=0\)
x0_init=1000;
t = 0;
x_hist=[0:dx:nx*dx]; %vecteur for histogram plot
xx=[0:dx:nx*dx]; %x vector for numerical solution
\(x_{an}=xx-xx(\text{round}(nx/2)+2)+dx/2\); %vector for analytical sol.

% ---- initialization for delta like charge density
u= zeros(nx+1,1);
u(round(nx/2)+1:round(nx/2)+2)=x0_init;
u_init=u;
Appendix C. Charge transfer modeling and simulation: theoretical derivations and codes

47 $u_{old} = u$

49 Num_{ch} = \text{sum}(u_{init}) \text{; \%initial number of charges}

51 \% initialization coordinates for the charges
52 c_{x} = \text{zeros}(\text{Num}_{ch},1);
53 c_{x}(1:\text{Num}_{ch}/2) = \text{round}(\text{nx}/2).*dx;
54 c_{x}(\text{Num}_{ch}/2+1:\text{Num}_{ch}) = (\text{round}(\text{nx}/2)+1).*dx;

56 if (0) \% to plot initial conditions
57 figure (2);
59 [h,bc] = \text{hist}(c_{x},x_{hist});
60 \text{plot}(bc.*1e6,h,'g','LineWidth',4)
62 \text{ylim}([0 \text{x0}_{init}]; \text{hold off}
63 \text{title}('Initial/conditions')
65 \text{xlabel}('x(\mu/m)'); \text{ylabel}('Charges');
67 end

69 \% Numerical solution of the diffusion equation
72 m=0;
74 dt = dx*dx*sigma/Dn; \% time step for diffusion
75 \text{while } t<t_{stop}
78 m=m+1
80 \% $t = t + dt$;
82 \text{end}

84 m=0;
86 dt = dx*dx*0.5/Dn; \% time step for random walk
88 t=0
89 \text{while } t<t_{stop}
92 m=m+1
94 \% RW montecarlo simulation
96 \% random direction for all the Num_{ch} charges
C.2. Calibration of the simulation of charge diffusion in the PPD

```matlab
r_num = rand (Num_ch,1);
while (isempty(find(r_num==0.5))==0)
    r_num = rand (Num_ch,1);
end
indplus=find(r_num>0.5);
indminus=find(r_num<0.5);
c_x(indplus)=c_x(indplus)+dx;
c_x(indminus)=c_x(indminus)-dx;
t=m*dt;
dsquare(m)=var(c_x); %distribution variance
end

%Check diffusion coefficient of the numerical solution:
%the function mygaussfit(x,y) returns the fitting parameters for the input function y(x)to the following gaussian function:
%y=A * exp( -(x-mu)^2 / (2*sigma^2) )
[sigma_gauss,mu,A]=mygaussfit(xx,u);
Dn_num_solution=sigma_gauss^2/(2*t)

%plot section
figure;
%exact solution
y_an=Num_ch/sqrt(4*pi*Dn*t)*exp((-(x_an).^2).../(4*Dn*t)).*dx;
%plot exact solution
plot(xx.*1e6,y_an,'r','LineWidth',4); hold on;
%plot solutions of the numerical simulation
plot(xx.*1e6,u,'o','LineWidth',2,'MarkerSize',6);
%compute and plot histogram of charge distribution from RW montecarlo simulation
[h,bc]=hist(c_x,x_hist);
plot(bc.*1e6,h,'gx','LineWidth',2,'MarkerSize',10);
%adjust and save
ylim([0 200]);
xlim([0 nx*dx.*1e6]; hold off;
xlabel('x(\mu m)','FontSize',24); ylabel('Charges','FontSize',24);
legend ('Analytical_solution','Numerical_solution','Random_walk');
set(gca,'FontSize',24);
saveas(gcf,'calibration_simu','eps')
saveas(gcf,'calibration_simu','fig')
```
Appendix C. Charge transfer modeling and simulation: theoretical derivations and codes

C.3 Simulation of the Random walk of charges in a PPD

Below the Matlab® code of the function used for the simulation of the random walk of charges in a PPD.

```matlab
% ==---------------------------------------------------------------
% Simulation of the random walk of N0 charges in a LPPDxWPPD square PPD
% considering:
% A. charge diffusion
% B. self induced drift
% C. drift field (induced by a potential difference dVPPD across the PPD)
% D. a potential barrier at the TG—PPD interface of height PhiB
% Boundary conditions:
% 1. reflecting wall at x=0
% 2. absorbing wall at x=LPPD
% 3. probability pjumb= exp(Phib/uth) for electrons to jump over
% the potential barrier
% ==---------------------------------------------------------------

function [tarrn,N0]=RW(LPPD,N0,DELTA,xdelta,PhiB,dVPPD,SELF)
% LPPD=PPD length
% N0=initial number of electrons
% PhiB_potential barrier
% dVPPD potential drop across the PPD
% SELF =1 to simulate self induced drift
% =0 to neglect self induced drift
% DELTA =1 to simulate a delta—like initial charge distribution
% =0 to simulate uniform charge distribution
% xdelta coordinate of the initial charge delta—distribution
% ==---------------------------------------------------------------

tic
% --- Define physical constants
T=300; % Temperature (K)
mn=2.366E−31; % mass of the electron (1 . kg−1)
kb=1.38e−23; % Boltzmann constant (m2 . kg . s−2 . K−1)
q=1.6E−19; %elementary charge (C)
uth=kb*T/q; %e— thermal voltage (V)
vth=2.30E+05; %e— thermal velocity (m/s)
un=500*1e−4; %electron mobility (m2/V/s)
tau_scat=un*mn/q; % e— scatter time (s)
mfpath=tau_scat*vth; % avarage mean free path (m)
Dn=uth.*un; % e— diffusion coeff. (m2/s)
dx= mfpath/2; % spatial step (m)
CPPD_A=1.2e−15; % area capacitance (F/um^2)
```

142
WPPD=1e−6; % PPD width m

% --- Define simulation parameters
xrefl=0; % coordinate of the reflecting wall (m)
LPPD=2*1e−6 % PPD length
nx=round(LPPD/dx); % number of nodes in x direction
xabs=nx*dx; % coordinate of the absorption wall (m)
xvector=[xrefl:dx:xabs]; % vector of x coordinates

% --- Initiate charge distribution
if DELTA==1
    c_x(1:0)=xdelta;
else
    Ndensity=round(N0/nx);
    N0=Ndensity*nx % print simulated N0
    for i=0:nx−1
        c_x(i*Ndensity+1:i*Ndensity+Ndensity)=i*dx;
    end
end

% --- Calculate drift field
if dVPPD==0
    Edrift=zeros(1,N0);
    Edrift(1) % print drift field
else
    Edrift=dVPPD/LPPD.*ones(1,N0); % external drift field V/m
    Edrift(1)
end

% --- calculate prob of emission across potential barrier
PhiB % print Phib
prob_em=exp(−PhiB/uth)% Probability of emission

% --- calculate capacitance to simulate self induced drift
CPPD=CPPD_A*WPPD*1e12*dx;% capacitance per unit length dx (F/m)

% initiate variables
E=zeros(1,N0);
E(:)=Edrift; % reset E vector
c_x_old=c_x;
tarr=zeros(1,N0); % vector containing electrons arrival time
Narr=0; % reset # transferred e−
Appendix C. Charge transfer modeling and simulation: theoretical derivations and codes

tic
Narrm1=0;
ttemp=zeros(1,N0);
Narr=0;
N=N0;
n=0;

% ---- Begin simulation
while N>0
    Dn=uth.*un.*ones(1,N); % e− diffusion coeff. (m2/s)
    Dself=zeros(1,N);

    if SELF==1
        hist_density=hist(c_x,xvector);
        for i=1:N
            edensity=hist_density(find(xvector==c_x(i)));
            if isempty(edensity)==0
                Dself(i)=un*q*edensity/CPPD;
            end
        end
    end
    dt = dx*dx/2./(Dn + Dself); % time step (s)

    indR=find(c_x<=xrefl); %index e− that reach reflecting wall
    indB=find(c_x>=xabs−dx); %index e− that reach potential barrier
    indRW=setdiff([1: N],unique(union(indR,indB))); %# other e−

    % ---- simulate effect potential barrier
    r_num_barr=rand(length(indB),1);
    i_njump=find(r_num_barr>prob_em);% e− that don't jump over Phib
    i_jump=find(r_num_barr<=prob_em);% e− that jump over Phib
    ind_back=indB(i_njump);
    ind_fwd=indB(i_jump);

    if isempty(ind_back)==0
        %reflection on the barrier
        c_x(ind_back)=c_x(ind_back)−dx.*ones(1,length(ind_back));
    end
    if isempty(ind_fwd)==0
        %transferred charge
        c_x(ind_fwd)=c_x(ind_fwd)+dx.*ones(1,length(ind_fwd));
    end

    % ---- reflection on the wall at x=0
end

tic
C.3. Simulation of the Random walk of charges in a PPD

if isempty(indR)==0
    c_x(indR)=c_x(indR)+dx+dt(indR)*un.*E(indR); %reflexion contre murPPD
end

% --- random walk of other electrons
r_num = rand(1,length(indRW));
while isempty(intersect(r_num,0.5))==0
    r_num = rand (1,length(indRW));
end
i_plus=find(r_num>0.5);
indplus=indRW(i_plus);
c_x(indplus)=c_x(indplus)+dx+dt(indplus)*un.*E(indplus); %step +dx

i_minus=find(r_num<0.5);
indminus=indRW(i_minus);
c_x(indminus)=c_x(indminus)-dx+dt(indminus)*un.*E(indminus); %step -dx
ind_running=find(c_x>=xabs);
for i=1:length(indarr)
    n=n+1;
    tarr(n)=ttemp(i);
end
Narr=Narr+length(indarr);

% print ' arrived electrons
if mod(Narr,100)==1
    if Narr>Narrm1
        Narr
    Narrm1=Narr;
c_x=c_x(ind_running);
ttemp=ttemp(ind_running);
dt=dt(ind_running);
N=N0-Narr;
end
end
toc
The readout circuit is the same for all the devices designed in this work. Below a short description of the main elements.

D.1 Readout Circuit for the 1D pixel arrays

A schematic view of the readout circuit of a 1D pixel array is shown in Fig. D.1. The readout circuit can be divided into four main blocks:

- The in-pixel electronics, which consists of 4 n-MOS transistors
  - $M_1$: Transfer Gate TG (that enables charge transfer from the PPD to the FD)
  - $M_2$: reset transistor (which allows to reset $V_{FD}$ at $VDD_{RST}$ before the acquisition of the reference signal).
  - $M_3$: Source follower (which guarantees a low impedance output)
  - $M_4$: Selection transistor (connects the pixel output to the sampling stage).

where $M_1$, $M_2$, $M_3$ have been sized and designed following the technology design recommendations.

- One n-MOS current source ($M_5$).

- Two sampling circuits (one for the reference and one for the signal), each consisting in a transistor ($M_6$) and a sampling MIM capacitor ($C_{ST}$).

- An output stage for each sampling circuit, which consists in a p-MOS source follower ($M_7$) and a p-MOS current source ($M_8$).

D.2 Simulations

The following sections detail the results of the circuit simulations with the simulator Spectre.
Figure D.1: Schematic diagram of the readout circuit of the 1D pixel array.
D.2. Simulations

D.2.1 Linear range

To estimate the linear range and the operation of the readout electronics, the circuit has been first simulated in DC. Figure D.2 shows the potentials $V_{\text{outN}}$ and $V_{\text{outP}}$ simulated as a function of the FD potential $V_{\text{FD}}$. The readout electronics has been simulated in DC in order to verify its good functioning and to estimate the linearity range output signal. The output voltage of the n stage and of the p stage as a function of the potential applied to the floating diffusion are shown in figure D.2. The gain $\frac{V_{\text{OUTN}}}{V_{\text{FD}}}$ is about $G_n = 0.8$, whereas the overall gain of the readout circuit $\frac{V_{\text{OUTP}}}{V_{\text{FD}}}$ is about $G_{\text{tot}} = 0.58$. From these curves we can also deduce the linear range of the circuit:

- For a non-linearity $< 5\%$:
  - Linear Range of 2.1V
  - Input voltage range between 1 V and 3.2 V
  - Output Voltage Range between 1.85 V and 3.2 V (for a total of 1.35 V)

- For a non-linearity $< 1\%$:
  - Linear Range of 1.6V
  - Input voltage range between 1.2 V and 2.8 V
  - Output Voltage Range between 1.9 V and 2.8 V (for a total of 0.9 V)

Figure D.2: DC simulation of the potentials $V_{\text{outN}}$ and $V_{\text{outP}}$ as a function of the FD potential $V_{\text{FD}}$. 

$$\text{d}V_{\text{OUTP}}/\text{d}V_{\text{FD}} = 0.5684x + 1.2069$$
Appendix D. Details on the readout electronics of the device under test

D.2.2 Bandwidth

To study the bandwidth of the readout circuit, a capacitance of 15 pF has been added at the output (this capacitance should model the capacitance due to the wire-bonding and to the capacitance of the conductive tracks from the package to the input of the instrumentational amplifiers on the PC. Figure D.3 shows the bode diagram for the gains $G_n$ and $G_{tot}$. The overall cut-off frequency is about $f_{cutoff} \approx 7 MHz$.

![Bode diagram showing gain vs. frequency]

Figure D.3: Simulated frequency response of the readout circuit. The cut-off frequency is about 7 MHz

D.3 Decoder

Each tested pixel-array has a dedicated decoder, where the number of bits have been adapted to the size of the array. The decoders only decode pixel addresses, whereas the driving signals of the TG and of the RST transistors are common to all pixels (so that both the high and low levels and the rise and fall fronts can be adjusted depending on the measurement). Here only a 8 bit decoder is described, however the other decoders have been designed with the same philosophy and the same building blocks.

Figure D.4 shows the schematic diagram of the decoder. Two main blocks can be identified: an address decoder (AD_DEC) and an output stage (OUT_DEC). In the address decoder, pixel addresses $X < 0 : 7 >$ are inverted twice to generate the signals $x_b < 0 : 7 >$ and $x_{int} < 0 : 7 >$. These signals and of the enable (EN) signal (which is set =1 to enable the
output of the decoder) are then combined by means of AND (NAND+NOT=AND) 4-inputs logic ports to generated $x_a < 0 : 7 >$, $x_b < 0 : 7 >$ and $x_c < 0 : 3 >$. The size of the transistors used to design the AND ports are shown in Fig. D.5. The transistors of the logic port NAND4_33 have the same size as the transistors of the port NAND3_33.

For a 8 bits decoder, the output stage is divided into 3 stages. The schematic diagram of the building bloc (OUT_DEC_BLOC) used for the 3 stages is shown in Fig. D.5. This block consists in a AND (NAND+NOT) logic function plus a double inversion (NOT+NOT). The inverters used for the later function (INV33BIG) are larger than the inverters of the address decoder. All transistors are 3.3 V logic transistors.
Appendix D. Details on the readout electronics of the device under test

Figure D.4: Schematic diagram of a 8 bit decoder
Figure D.5: Schematic diagram of the building block of the decoder output stage.
Publications and Conferences


Acknowledgment

This thesis would never have been the same without the support of all the people I had the chance to share these three years with.

I first would like to acknowledge all the members of my jury: Albert Thewissen (TU Delft), Tobi Delbruck (ETH Zurich), Xuezhou Cao (Xfab semiconductor) and Thierry Camps (UPS, Toulouse) for taking the time to read the manuscript and for accepting to attend and evaluate my Ph.D defense.

I would like to thank my supervisors at ISAE, Pierre Magnan and Vincent Goiffon, for selecting me for this Ph.D. position and for following my work all along the journey. In particular I would like to thank you Pierre for enrolling such an outstanding jury for the defense and Vincent for taking the time, despite your tight schedule, to share with me both your knowledge and passion for science. I would like to thank Cédric Virmontois (CNES), Olivier Saint-P (Airbus DS) and Michel Brart de Boisanger (Airbus DS) for supporting and supervising my work.

I also would like to thank Aziouz Chabane, Paola Cervantes and Barbara Avon for their support during the development and debugging of the experimental set-up. I would probably still be characterizing my circuits (or at least trying to) without your invaluable help. A kind thought also to Magali Estribeau, for the numerous enriching discussions about charge transfer around a cup of coffee. A special thank for my dear friend Eleanor and my mum for having the courage to read and check my manuscript from top to bottom. I dont know how many people would have been crazy (and nice) enough to do that..

I would like to acknowledge Mr. Assaf Lahav (TowerJazz), for the very interesting exchanges on pinning voltage measurements.

A warm THANK YOU! to my Ph.D. fellows Clémentine, Jean-Baptiste, Jean Marc and Valerian, for their charming company and for the never-ending debates about the philosophy of the p-n junction. Thanks also to all the people from CIMI, MOSE and SSPA for their friendship, the relaxing coffee breaks and for trying to teach me (with poor success) how to play coinche.

I would also like to thank my friends for all the fun and distracting moments around a beer or wandering in the mountains. A special thought also to my family, for always believing in me during these (too) many years of studies and for dragging me, every now and then, on the other side of the planet to help me forget PPDs even existed...

Finally I would like to thank Damiano, for his support, love and (great) patience.
Abstract — Driven by an aggressive market competition, CMOS Image Sensor technology is in continuous evolution. Thanks to the outstanding noise performances of Pinned Photodiode (PPD) CIS, CMOS sensors can now reach a few photons sensitivity, which makes this technology a particularly interesting candidate for high temporal resolution applications. Despite the incredibly large production volume, today, the PPD physics is not yet fully understood, and there is still a lack of golden standards for the characterization of PPD performances. This thesis focuses on the definition, analytical modeling, simulation and estimation of PPD key design parameters, with a particular focus on charge mechanisms, on the pinning voltage and on the full well capacity. The models developed in this work can help both manufacturers and users understanding the design trade-offs and the dependence of these parameters from the experimental conditions, in order to optimize the sensor design, to correctly characterize the image sensor, and to adjust the operation conditions to reach optimum performances.

Keywords: Pinned Photodiode, CMOS Image Sensors, transfer time, pinning voltage, Full Well Capacity, high temporal resolution, pulse storage gate pixel

Résumé — Poussée par une forte demande et un marché très compétitif, la technologie PPD CIS est en évolution permanente. Du fait de leurs très bonnes performances en terme de bruit, les capteurs d’image CMOS à base de Photodiode Pincée (PPD CIS) peuvent désormais atteindre une sensibilité de l’ordre de quelques photons, ce qui rend cette technologie particulièrement intéressante pour les applications d’imagerie à haute résolution temporelle. Aujourd’hui, la physique des photodiodes pincées n’est pas encore comprise dans son intégralité et il y a un manque important d’uniformisation des méthodes de caractérisation de ces détecteurs. Ces travaux s’intéressent à la définition, à la modélisation analytique, à la simulation et à l’estimation de paramètres clés des PPD CIS, tels que le temps de transfert, la tension de pincement et la full well capacity (FWC). Comme il a été mis en évidence par cette thèse, il est de première importance de comprendre l’effet des conditions expérimentales sur les performances de ces capteurs. Ceci aussi bien pour l’optimisation de ces paramètres lors de la conception du capteur, que lors de la phase de caractérisations de celui-ci, et enfin pour choisir correctement les conditions de mesures lors de la mise en œuvre du dispositif.

Mots clés : Photodiode pincée, Capteurs d’image CMOS, transfert de charge, tension de pincement, Full Well Capacity, haute résolution temporelle, pixel à grille de stockage pulsée.

ISAE-SUPAERO, Université de Toulouse, Image Sensor Research Team, 10 avenue E. Belin, F-31055, Toulouse, France
En vue de l’obtention du

DOCTORAT DE L’UNIVERSITÉ DE TOULOUSE

Délivré par :
Institut Supérieur de l’Aéronautique et de l’Espace

Présentée et soutenue par :
Alice PELAMATTI
le mardi 17 novembre 2015

Titre :
Estimation et modélisation de paramètres clés des capteurs d’image CMOS à photodiode pincée pour applications à haute résolution temporelle

Estimation and modeling of key design parameters of pinned photodiode CMOS image sensors for high temporal resolution applications

École doctorale et discipline ou spécialité :
ED GEET : Micro et Nanosystèmes

Unité de recherche :
Équipe d’accueil ISAE-ONERA OILMPE

Directeur/trice(s) de Thèse :
M. Pierre MAGNAN (Directeur de thèse)
M. Vincent GOIFFON (Co-directeur de thèse)

Jury :
M. Thierry CAMPS - Président du jury
M. Pierre MAGNAN - Directeur de thèse
M. Vincent GOIFFON - Co-Directeur de thèse
M. Albert THEUWISSEN - Rapporteur
M. Tobi DELBRUCK - Rapporteur
Mme Xuezhou CAO
Introduction

Les images numériques font désormais partie de notre vie quotidienne. Grâce à un développement technologique extrêmement rapide dans le domaine des capteurs d’image CMOS (CIS), des imageurs très performants, dont l’utilisation était confinée aux appareils photo haut de gamme ou professionnels durant l’ère "CCD" (Charge Coupled Device), se trouvent aujourd’hui sur les téléphones intelligents et les tablettes. De plus en plus de fonctions peuvent être intégrées in-pixel (on parle désormais de pixels "intelligents") et, chaque année, les fabricants repoussent un peu plus loin les limites des capteurs en termes de performances de bruit, de vitesse, d’efficacité de détection, de résolution etc. Chaque saut technologique ouvre la porte à de nouvelles applications commerciales et scientifiques.

L’imagerie spatiale est un domaine particulièrement exigeant car les détecteurs doivent satisfaire aux exigences de la mission tout en garantissant une faible consommation d’énergie, une résistance à l’environnement radiatif, une fiabilité à long terme et, surtout, contrairement aux appareils photo "terrestres", où l’optique peut être adaptée pour répondre aux exigences du détecteur, les imageurs spatiaux doivent souvent respecter les contraintes optiques de la charge utile. Au cours de cette dernière décennie, l’accent a été mis sur les missions spatiales basées sur des détecteurs à haute résolution temporelle, (tels que les détecteurs LIDAR) pour la météorologie [MFT08], les applications altimétriques ou plus généralement d’imagerie 3D, pour le guidage, la navigation et le contrôle des modules d’atterrissage planétaire [CC08] (par exemple pour choisir un site d’atterrissage sûr), pour la mise en orbite planétaire [Kol+15], ou encore pour l’estimation de l’attitude et de la géométrie de débris spatiaux. Les caractéristiques des détecteurs sont spécifiques à chaque mission, toutefois, en règle générale, le principal défi est l’échantillonnage très rapide d’un signal lumineux pendant une fenêtre de temps limitée.

Dans les capteurs d’images standard, la fréquence d’acquisition est souvent limitée par le débit maximal de sortie des données, i.e. par le temps nécessaire pour accéder à la matrice de pixels, effectuer la conversion analogique-numérique et acquérir les données provenant du circuit intégré [ED+09]. Afin d’améliorer la fréquence d’échantillonnage, une première solution consiste à parallélibser la lecture au moyen de sorties multiples, toutefois le nombre maximum de sorties est souvent limité par la complexité accrue du banc d’acquisition et par le bilan de puissance. Une approche alternative à l’acquisition d’images en mode "continu" consiste à séparer la phase d’acquisition des phases de lecture et de conversion analogique-numérique. Ceci peut être réalisé en stockant des échantillons temporels "in-situ" au cours de la fenêtre d’acquisition par le biais de mémoires analogiques (situées dans le pixel ou dans une zone séparée du circuit intégré) et en lisant les données dans un deuxième temps. Ce mode d’acquisition est souvent dénommé ‘en rafale’ ("burst") en opposition au "mode continu". Les premiers imageurs burst avec stockage "in situ" que l’on trouve dans la littérature sont basés sont des capteurs CCD [Kos+96] ; [EMT99]. Une analyse synthétique des progrès dans cette direction est fournie par Etoh et al. dans [Eto+11] . Ces capteurs peuvent atteindre des fréquences image exceptionnelles, souvent au prix d’une consommation très élevée (et d’un
échauffement important du capteur). Pour la plupart des applications scientifiques et commerciales, la tendance est de reproduire les fonctionnalités des capteurs CCD en utilisant la technologie CIS, qui est souvent plus accessible, offre de meilleurs performances en termes de consommation de puissance [Fos93] et contrairement à la technologie CCD, est en constante évolution et devrait être encore disponible au cours des prochaines années. Quelques années après l’invention du premier capteur CCD à prise de vue en rafale, nous trouvons en effet les premières implémentations de capteurs CIS avec stockage des images in-situ [Kle+04]; [ED+11]. La fréquence d’échantillonnage de ces détecteurs n’est pas encore comparable aux derniers capteurs CCD burst (qui visent désormais 10 G images par seconde [Eto+13]), toutefois le développement récent de la technologie 3D [Son] peut donner un gros avantage aux capteurs CMOS en termes de capacité de stockage [Bon+13b].

La fréquence d’échantillonnage maximale pouvant être atteinte avec un capteur d’images dépend fortement des performances de bruit et d’efficacité de détection et du gain du capteur. En effet, un temps d’échantillonnage très court implique un signal très faible, et donc, afin de garantir un bon rapport signal à bruit, il est nécessaire que le détecteur ait un très faible bruit de lecture (ou bien que le signal d’entrée soit très élevé). Les capteurs d’images CMOS à Photodiode Pincée (PPD CIS) présentent intrinsèquement de meilleures performances en termes de bruit que les capteurs standards à pixels actifs (3T APS) et sont donc d’excellents candidats pour les détecteurs à haute résolution temporelle. Un exemple de capteur PPD CIS burst ayant démontré des capacités de vitesse jusqu’à 10 M images par seconde est présenté dans [Toc+12]. Ce dispositif comprend six circuits de sortie parallèles associés à six amplificateurs de sortie et est divisé en deux zones, l’une contenant la matrice de pixels en 2D, et l’autre les matrices de 140 mémoires analogues par pixel. Une approche alternative (ou complémentaire) aux multiples sites de stockage par pixel consiste à s’afranchir des contraintes de vitesse sur l’électronique in-pixel en augmentant le nombre de sorties associées à chaque photodiode (pixels "multi-tap"). Comme les pixels à PPD sont basés sur un transfert de charge (et non pas sur une partition des charges), des pixels multi-tap peuvent être facilement implémentés dans les PPD CIS. Il s’agit, en effet, d’une solution actuellement adoptée pour les pixels "démodulateurs" (lock-in pixels) pour les mesures de temps de vol (Time of Flight, ToF) [Lan+00]; [BLS06]; [Sto+11]; [Kim12]; [Sto+11]; [Bon+13a]; [Han+15].

Une fois que toutes ces solutions permettant l’amélioration de la fréquence image ont été implémentées, la limite ultime en termes de fréquence d’échantillonnage des PPD CIS est due au temps nécessaire pour transférer les électrons depuis la zone de collection (la PPD) vers le nœud de lecture. Ce temps de transfert dépend des mécanismes de transport qui interviennent au cours du transfert de charge, de la géométrie du pixel et des réglages fins du procédé technologique utilisé, afin d’optimiser le profil du potentiel tout au long du chemin de transfert. La réduction du temps de transfert implique souvent un compromis entre les différents paramètres de conception et entre ces derniers et les contraintes spécifiques de la mission/application ; ainsi, lors du développement d’un détecteur PPD CIS à haute résolution temporelle, il est primordial de bien comprendre la signification physique de chacun des paramètres et leur impact les uns sur les autres.

1. La sécurité d’approvisionnement est un aspect particulièrement critique pour les applications spatiales, car il peut passer de 10 ans entre le prototype de l’instrument et son lancement.
Cette thèse porte sur la définition, la modélisation analytique, la simulation et l'estimation des paramètres clé de conception d’un capteur PPD CIS pour applications à haute résolution temporelle. Le chapitre 2 de cette thèse étudie le temps de transfert, qui détermine la limite ultime en termes de résolution temporelle dans les capteurs PPD CIS. En particulier, le transfert de charge, simulé par le biais d’un modèle Montecarlo, est implémenté en Matlab, prenant en compte différents phénomènes de transport des charges tels que la diffusion thermique, la dérive et l’émission thermoïonique au dessus de la barrière de potentiel qui se trouve à l’interface entre la grille de transfert (TG) et la PPD. L’effet sur la vitesse de transfert du champ électrique latéral induit par la TG, du champ auto-induit et du piégeage de charge sous la TG est aussi étudié dans ce chapitre. Les résultats des simulations sont comparés à des simulations TCAD et à des mesures expérimentales obtenues sur des pixels à grille de stockage pulsée qui permettent de reproduire le pire scénario en termes de temps de transfert, c’est à dire lorsque le paquet de charge est photo-généré à l’extrémité de la PPD.

La tension de pincement est une deuxième figure de mérite clé des PPD CIS qui est très souvent utilisée comme référence pour l’optimisation des niveaux de dopage sous la TG et des tensions de polarisation et d’alimentation (afin de maximiser la vitesse de transfert de charge). La définition, la modélisation et l’estimation de ce paramètre sont abordées dans le chapitre 3 du manuscrit. Au sein de la communauté CIS, la tension de pincement est estimée à travers différentes méthodes, fondées sur des principes physiques très différents et qui ne fournissent pas toujours le même paramètre physique et/ou ne sont pas fondées sur de solides équations de dispositifs à semi-conducteur. La première partie du troisième chapitre de cette thèse présente une comparaison des principales méthodes d’estimation et propose une discussion sur la définition et la signification physique de la tension de pincement. En particulier, il est démontré par le biais de démonstrations analytiques, de simulations TCAD et de mesures expérimentales, que la définition théorique couramment acceptée de ce paramètre ne correspond pas au paramètre physique qui est mesuré avec les méthodes existantes. Il étudie également l’effet de la température sur la tension de pincement.

Pour améliorer la vitesse de transfert par rapport aux simples phénomènes diffusifs, des solutions permettant de générer des champs de dérive [Tub+09]; [Tak+10]; [Sto+11]; [Han+14], ont été implémentées dans la littérature. La chute de tension maximale (et donc le champ électrique maximal) qui peut être générée aux bornes de la PPD est égale à la tension de pincement. La deuxième partie du chapitre 3 est consacrée à la discussion, à la simulation et à la validation expérimentale de deux méthodes proposées dans la littérature permettant de moduler, respectivement, de façon statique [Tak+10] et dynamique [Han+14], le potentiel dans la PPD et donc de générer un champ de dérive pour améliorer la fréquence d’échantillonnage tout en garantissant une bonne efficacité de transfert de charge.

En conditions de faible éclairement, le signal de sortie est principalement affecté par le rapport signal à bruit du dispositif et par l’efficacité de transfert de charge. En conditions de fort éclairement (donc de fort signal), les performances du capteur sont souvent évaluée en termes de nombre maximum d’électrons pouvant être collectés par la PPD, i.e. la Full-well capacity (FWC). Le chapitre 4 est dédié au développement d’un modèle analytique permettant de prédire la FWC en fonction de la température, des tensions de polarisation et des condi-
tions d'éclairement. La première partie du chapitre introduit le concept de FWC à l'équilibre (EFWC), qui correspond à la FWC mesurée dans le noir et avec la TG en mode accumulé et qui est la seule valeur de FWC qui dépend uniquement de la géométrie et des profils de dopage de la PPD. Ces travaux montrent que la FWC est un paramètre auquel il est important de se référer lorsque l'on choisit le niveau d'éclairement ou lorsque l'on souhaite étudier l'effet des conditions expérimentales (ou encore d'une campagne d'irradiation) sur la FWC. Cette thèse étudie également le comportement dynamique de la FWC en conditions d'éclairement non-stationnaire. En particulier, il est montré que si le flux lumineux est soudainement modifié, la PPD se charge/décharge afin de tendre vers une nouvelle condition d'équilibre. Le transitoire dépend fortement des conditions initiales et finales d'éclairement et peut avoir une durée de plusieurs minutes. Ces phénomènes peuvent induire des erreurs de mesure importantes pour les applications à haute résolution temporelle, telles que les mesures de temps de vol, qui sont souvent basées sur une source lumineuse pulsée ou, de façon plus générale, visent à imager des scènes qui varient très rapidement. Pour cela il est montré que pour ce type d'applications, le flux de photons incident doit toujours être choisi suffisamment faible pour maintenir la charge de la PPD en dessous de l'EFWC.

Les modèles développés au cours de ces travaux de thèse peuvent être un outil très utile aux fabricants pour pouvoir prédire comment les différentes conditions expérimentales affectent les performances du détecteur, notamment en cas d'applications haute résolution temporelle, afin de tenir compte de ces effets lors de la phase de conception. Les résultats de cette étude sont aussi importants en ce qui concerne les phases de caractérisation, notamment en termes de choix de la méthode de caractérisation (par exemple pour la mesure du CVF, de la FWC et de la tension de pincement). Enfin, comme mis en évidence par ces travaux, il est important de définir au plus vite des standards pour l’estimation des figures de mérite des PPD CIS afin de fournir aux utilisateurs des paramètres bien définis et comparables.
Résumé des travaux de thèse

1 Capteurs d’image CMOS à Photodiode Pincée

1.1 Des premier photodétecteurs aux capteurs CMOS

En 1965 G. Weckler étudie le premier photodétecteur en mode intégration basé sur une jonction p-n [Wec65] ; [Wec67]. Ce dispositif était basé sur l’observation expérimentale que le potentiel aux bornes d’une jonction p-n polarisée en inverse et laissée flottante (par le biais d’un interrupteur) décroit à une vitesse dépendant linéairement du flux lumineux. La variation de potentiel peut être exprimée en fonction de la capacité de la jonction p-n (C_d), de la surface du détecteur (A_d) et de la densité du courant photonique (y J_ph) :

\[ \frac{dV}{dt} \approx \frac{J_{ph} A_d}{C_d} \] (1)

où le courant photonique I_ph = J_p A_d est dû à la génération de paires d’électrons-trou suite à l’absorption de photons ayant une énergie E_ph supérieure à la bande interdite du semi-conducteur [Sze85]. En polarisation inverse, les électrons photogénérés dans la zone de charge d’espace (ZCE) (ou qui atteignent la ZCE par diffusion thermique) sont balayés par le champ électrique, entraînant une diminution du potentiel inverse de la photodiode.

L’énergie d’un photon peut être exprimée en fonction de sa longueur d’onde \( \lambda \) comme [Sze85] :

\[ E_{ph} = \frac{hc}{\lambda} \] (2)

où \( h \) est la constante de Planck’s et \( c \) est la vitesse de la lumière. Le nombre d’électrons par nombre de photons incidents collecté est appelé efficacité quantique (QE) :

\[ QE(\lambda) = \frac{J_{ph}}{q\Phi_{ph}(\lambda)} \] (3)

où \( \Phi_{ph}(\lambda) \) est le flux de photons incident par unité de surface et \( q \) la charge élémentaire. La QE est fortement affectée par les caractéristiques de réflexion optique (interne et externe), par la profondeur d’absorption des photons et par la capacité de collecter les charges photogénérées. Pour cela, il s’agit d’un paramètre fortement dépendant de \( \lambda \) [Sze85]. De façon plus générale, I_ph peut être exprimé comme

\[ I_{ph} = A_d \int_{\lambda} \Phi(\lambda)QE(\lambda)d\lambda \] (4)

L’origine de l’imagerie dynamique est souvent attribuée à l’invention des CCDs (Charge Coupled Device) par Willard Boyle and George E. Smith dans les laboratoires AT&T Bell en...
Résumé des travaux de thèse

1969 [BS70], pour laquelle ils ont reçu le Prix Nobel de physique en 2009. En 1968, P. Noble étudie la première matrice de pixels MOS [Nob68], et pose les premières bases qui amèneront, par la suite, au développement des capteurs CMOS à pixel actif (APS) [Fos93], souvent appelés capteurs à 3 transistors (3T APS). Grâce aux très bonnes performances des CCDs [The95]; [Jan01] par rapport aux capteurs CMOS, la plupart des imageurs scientifiques et commerciaux ont été basés sur la technologie CCD jusqu’aux années 1990, quand les imageurs CMOS (CIS) ont lentement pris le dessus, poussés par un développement de plus en plus massif de produits électroniques pour applications commerciales. En 1995, Lee et al.[Lee+95] développent les premier CIS à base de photodiodes pincées (PPDs) [Ter+82]; [Bur+84]. Cette technologie est souvent appelée PPD CIS, ou encore APS 4-Transistors (4T). Grâce aux excellentes performances en bruit des PPD CIS, au développement de la technologie en éclairement arrière (BSI) [Pai+05]; [Iwa+06]; [Rho+09], à des noeuds technologiques de plus en plus petits [Ov1] et à la récente introduction des technologies 3D [Sou]; [Suk+13]; [Gra14], les CIS sont désormais concurrentielles en termes de performances avec les CCD, aussi bien du point de vue du bruit, que de la QE et de la vitesse [Moc+15], avec tous les avantages intrinsèques de la technologie CMOS (coûts plus contenus et possibilité d’intégrer des fonctions complexes dans les pixels). Ces détecteurs sont désormais la technologie la plus répandue pour les imageurs commerciaux, mais trouvent aussi de nombreuses applications scientifiques, telles que les applications de temps de vol (ToF) ou pour la microscopie en fluorescence [YK06]; [YIK09]; [MC11]; [Li+12] ou le ranging [Tub+09]; [Tak+10]; [Han+14]. Pour plus de détails sur l’évolution des CIS et sur les principales figures de mérite, le lecteur peut faire référence à la section 1.2 de cette thèse ou à la revue d’Eric Fossum [FH14].

1.2 Principe de fonctionnement des capteurs PPD CIS

Quand on parle d’APS, on fait référence à une matrice de pixels intégrant un élément photosensible (la photodiode) et un ou plusieurs transistors. Le principe de fonctionnement d’un pixel CIS standard (3T) est détaillé dans la section 1.3 de ces travaux. Un dessin schématique d’un pixel PPD pixel est reporté dans la Fig. 1 : la photodiode (PPD) est associée à une grille de transfert (TG), qui permet d’isoler la PPD du nœud de lecture (diffusion flottante FD) pendant la phase d’intégration de la lumière (TG off) et de transférer les électrons vers la FD (TG on), où le signal est converti du domaine de charge au domaine de tension et lu en sortie.

La PPD est une photodiode enterrée, formée par une double jonction p+np. L’implant p+ de surface (implant de pincement) permet de réduire fortement le courant d’obscurité de ces détecteurs par rapport aux APS 3T, car il isole la ZCE des centres de génération-recombinaison situés à l’interface Si – SiO2. Les caissons P (P-well) permettent à leur tour d’isoler la ZCE de l’oxyde des tranchées d’isolation (STI). Les profils de dopage utilisés pour générer la PPD (Np PIN, Nd PPD et Nn , respectivement pour l’implant de pincement, pour l’implant n et pour l’épitaxie) sont optimisés de sorte que la jonction p-n supérieure puisse être approximée à une jonction mono-latérale et que la ZCE de la jonction inférieure contribue faiblement à la déplétion de la zone n (afin de maximiser la capacité de stockage de la PPD).

Du fait de cette structure stratifiée, le potentiel de la PPD VPPD est confiné entre une
1. Capteurs d’image CMOS à Photodiode Pincée

dans sa valeur maximale (appelée tension de pincement) et le potentiel de surface (typiquement la masse). Par conséquent, si la PPD est soudainement connectée à un puits de potentiel plus profond (avec \( V_{\text{well}} > V_{\text{pin}} \)), les charges stockées dans la PPD sont drainées vers le puits de potentiel et \( V_{\text{PPD}} \) augmente jusqu’à atteindre \( V_{\text{PPD}} = V_{\text{pin}} \). Grâce à ce plafond de potentiel, il est possible d’implémenter un vrai transfert de charge dans ce type de dispositif (alors que les pixels 3T permettent uniquement d’implémenter un partage de charge entre capacités).

La TG est un transistor dont la source et le drain sont, respectivement, la PPD et la FD. Des implants spécifiques à chaque technologie peuvent être présents sous la TG pour isoler la PPD de la FD (implant d’anti punch-through, APT), pour moduler spatialement la tension de seuil du transistor afin de minimiser l’injection de charge de la FD vers la PPD [BBK12] ou encore pour optimiser le profil de potentiel le long du chemin de transfert (pour ne pas créer de barrière/poche de potentiel à l’interface PPPD-TG [Jan01]).

La structure FD associée au transistor de reset (RS), au transistor suiveur (SF) et au transistor de sélection de colonne (SEL) rappelle fortement la structure d’un APS standard. Toutefois, la FD n’est pas utilisée pour collecter les charges, mais uniquement pour convertir le signal en une tension de sortie. Des transistors additionnels sont parfois inclus dans le pixel pour implémenter des fonctions d’anti-éblouissement ou d’obturateur global (global shutter).

\[ \text{Figure 1 – représentation schématique d’un pixel PPD.} \]

Un exemple de chronogramme de lecture d’un pixel à 4 transistors est reporté sur la Fig. 2. Au terme du temps d’intégration, la FD est réinitialisée en activant le transistor RS, puis la référence \( V_{\text{ref}} \) est échantillonnée. La TG est pulsée en mode passant pour transférer la charge stockée dans la PPD \( (Q_{\text{PPD}}) \) vers la FD, puis à nouveau en mode bloqué. Le signal \( V_{\text{sig}} \) est donc échantillonné et une nouvelle phase d’intégration commence. Le signal de sortie
Q_{PPD} est mesuré comme :

\[ Q_{PPD} = \frac{V_{ref} - V_{sig}}{CVF} \] (5)

On peut identifier deux différences principales par rapport à un pixel 3T :

- Le facteur de conversion de charge à tension (CVF) dépend uniquement de la FD et pas de la surface du pixel. Une étude sur la mesure du CVF dans les PPD CIS est présentée dans l’annexe B de ces travaux.

- La présence de la TG permet d’implémenter un double échantillonnage corrélé (CDS), (ce qui permet de s’affranchir du bruit KTC).

Il est possible de faire fonctionner le détecteur en mode global shutter [Mey13]; [WM15]; [Liu+15]; [Lau+07]; [YIK10]; [Sak+12] en modifiant le chronogramme de lecture (et/ou en ajoutant des transistors supplémentaires). Pour plus de détails, se reporter à la section 1.4 du manuscrit.

1.3 Conclusion

Grâce à leur très bon rapport signal à bruit (SNR) et à la possibilité d’implémenter un vrai transfert de charge, la technologie PPD CIS est une très bonne candidate pour les détecteurs pour applications à haute résolution temporelle. Ces dernières demandent, en effet, un échantillonnage très rapide d’un signal lumineux en entrée et donc de pouvoir mesurer des signaux extrêmement faibles (du fait du temps d’intégration très court). Lors de la conception d’un détecteur PPD CIS pour applications à haute résolution temporelle, il faut très souvent faire des compromis entre des problématiques optiques, de rapidité, de bruit (tout en tenant compte de l’amplitude typique des signaux en jeu). Par exemple, une grande surface de PPD améliore le SNR au détriment de la fréquence d’échantillonnage (une étude sur l’effet de la géométrie du pixel sur les limites en rapidité des PPD CIS est présentée dans le chapitre 2 de cette thèse). La tension de pincement, qui fait l’objet du chapitre 3 de ces travaux, est une autre figure de mérite qui doit être ajustée avec attention en fonction de la tension d’alimentation et des caractéristiques de la TG, afin de trouver un bon compromis entre la
1. Capteurs d’image CMOS à Photodiode Pincée

FWC (Full Well Capacity, i.e. la charge maximum pouvant être collectée par la PPD) et l’efficacité de transfert de charge. Le troisième paramètre clé, traité dans le chapitre 4 de ces travaux, est la FWC. Cette figure de mérite affecte très fortement les performances du détecteur en termes de plage de sensibilité (IDR, dynamic range) et de vitesse (à fort signal). En particulier, cette thèse a mis en évidence que la FWC dépend fortement des conditions expérimentales. Comme suggéré par ces travaux, la valeur de FWC mesurée à l’équilibre (EFWC) peut être utilisée comme référence afin d’étudier le comportement en saturation de la PPD. En particulier, ils montrent que pour les application à haute résolution temporelle, la taille de la PPD doit être dimensionnée de sorte à maintenir la charge dans la PPD en dessous de l’EFWC afin de s’affranchir des erreurs pouvant être engendrées par le comportement dynamique de la charge de saturation en condition d’éclairement non-stationnaire.
Résumé des travaux de thèse

2 Modélisation, estimation et mesure du transfert de charge

La limite ultime des PPD CIS en termes de fréquence d’échantillonnage dépend du temps nécessaire pour transférer les charges de la PPD vers le nœud de lecture. Certaines applications scientifiques, telles que les applications spatiales, demandent des pixels de grande taille (par exemple pour des contraintes de type optique [Kra+13]). Pour cela il est important d’étudier l’effet de la longueur du chemin de transfert des électrons (et donc la longueur de la PPD) sur l’efficacité de transfert, afin de trouver un compromis optimum entre les contraintes géométriques de l’instrument et les performances finales du détecteur. Le chapitre 2 de cette thèse étudie les différents mécanismes de transport de charge dans les PPD CIS et comment ces paramètres sont affectés par la géométrie du pixel. En particulier, le transfert de charge est simulé par le biais de simulations Montecarlo du mouvement aléatoire des électrons (random walk). Ces résultats sont comparés à des simulations TCAD et à des mesures expérimentales obtenues sur des pixels dédiés présentant une grille de stockage utilisée en mode pulsé.

2.1 Définitions

Le transfert de charge peut être caractérisé en termes de temps de transfert de charge ou d’efficacité de transfert de charge (CTE). La définition la plus intuitive serait "le temps nécessaire à transférer tous les électrons de la PPD vers la FD". La diffusion des électrons est un phénomène fortement aléatoire, on peut donc uniquement parler de temps de transfert moyen. Pour cela, on étudie plus fréquemment le comportement du détecteur en termes de CTE :

\[ \text{CTE} = \frac{Q_{\text{out}}}{Q_{\text{PPD}}} \]  

(6)

où CTI (inefficacité de transfert) (avec \( \text{CTI} = 1 - \text{CTE} \)), qui permet de mesurer la charge moyenne transférée (ou non-transférée par la CTI) normalisée par rapport à la charge initiale stockée dans la PPD avant le transfert. Une CTE inférieure peut donner lieu (selon le mode d’opération du capteur) à une rémanence de charge et donc à l’apparition d’images "fantômes" dans des conditions d’éclairement non-stationnaires. Ces phénomènes sont souvent indiqués sous le nom de "image lag". Dans ces travaux, le terme temps de transfert fait référence au temps moyen nécessaire pour atteindre un niveau donné de CTI.

2.2 Mécanismes de transport de charge dans les PPD CIS

Les mécanismes de transport de charge dans les détecteurs CCD ont été largement étudiés dans la littérature [CKR72]; [Bar75]; [MMM73]; [Ban+91]; [Jan01]. Les trois mécanismes principaux sont : la diffusion thermique, l’effet du champ latéral de la TG et du champ auto-induit [CKR72]. Si les porteurs rencontrent une "barrière" ou une "poche" de potentiel le long du chemin de transfert ("pièges de conception" dans [Jan01]), le transfert de charge dépend aussi de l’émission thermoïonique des électrons à travers la barrière de potentiel. La section 2.2 de ce travail étudie comment ces différents mécanismes peuvent être appliqués aux
2. Modélisation, estimation et mesure du transfert de charge

PPD CIS. La discussion s’appuie sur un modèle Montecarlo de transfert de charge développé en Matlab® et sur des simulations TCAD. La section 2.2.8. présente, de plus, une étude des phénomènes de piégeage et misonéisme de porteurs sous la TG.

2.3 Cartographie du temps de transfert

Idéalement il serait souhaitable de pouvoir faire une cartographie du temps de transfert en fonction de la position initiale d’un porteur. Simulons tout d’abord le cas le pire : le transfert d’un électron situé à l’opposé de la PPD par rapport à la TG. L’expérience est répétée 1000 fois pour différentes longueurs de PPD : 1µm, 2µm, 8µm and 16µm. Dans les premières simulations, seule la diffusion des porteurs est prise en compte. Une description détaillée des conditions aux bornes qui permettent de simuler le confinement des charges dans la PPD est reportée dans la section 2.2.11 de cet ouvrage. Les histogrammes des temps de transfert correspondent sont reportés dans la Fig. 4a. Comme on peut l’observer, le temps de transfert peut varier de presque deux ordres de grandeur pour différentes répétitions de l’expérience. Il est important de bien garder en tête ce comportement statistique (qui ajoute un bruit de transfert supplémentaire par rapport aux contributions étudiées dans [Fos03]), notamment si l’on souhaite atteindre une résolution de quelques photons.

Les courbes de CTI issues des histogrammes de la Fig. 2.5a de cette thèse sont présentées Fig. 4b. On peut observer que l’augmentation de la longueur de la photodiode entraîne un décalage de la courbe de CTI. De plus, comme montré Fig. 5, le temps de transfert (défini ici comme le temps moyen pour atteindre une CTI de 0.001) augmente avec le carré de la longueur de la PPD (ce dernier résultat est cohérent avec les équations de diffusion).

2.4 Comparaison entre simulations numérique et simulations TCAD.

Les résultats des simulations numériques ont été comparés au transfert simulé en TCAD, dont les courbes de CTI sont montrées Fig. 2.9 de cet ouvrage. Avant le début du transfert, la PPD est à l’équilibre (dans le noir avec TG en mode accumulé), donc les charges sont distribuées uniformément dans la photodiode). Comme on peut l’observer, le temps de transfert
Résumé des travaux de thèse

Figure 4 – Courbes de CTI correspondantes à la simulation Montecarlo du transfert de 1000 électrons pour différentes longueurs de PPD.

Figure 5 – Temps de transfert correspondant à une CTI de 0.001 en Fig. 4b en fonction de la longueur de la PPD.
2. Modélisation, estimation et mesure du transfert de charge

correspondant à une CTI 0.001 est comparable à celui simulé en Matlab pour la photodiode avec \( L_{PPD} = 8 \ \mu m \), cependant le transfert est bien plus rapide si l’on réduit la longueur de la PPD. Cette différence est attribuée au fait que la simulation TCAD tient compte de l’effet du champ latéral de la TG (ce qui n’est pas le cas pour les simulations numériques présentées), qui devient de moins en moins négligeable plus la photodiode est courte.

2.5 Pièges de conception

Afin d’étudier l’effet de la barrière de potentiel à l’interface PPD-TG due à la présence de piège de conception (design trap), deux structures différentes (montrées Fig. 2.10 de la thèse) ont été simulées en TCAD. Les deux structures diffèrent uniquement au niveau de l’interface entre la PPD et la TG (la structure B est identique à celle simulée Fig. 2.9 de cet ouvrage alors que les implants de la structure A ont été ajustés pour que le canal de la PPD ne remonte pas/ou peu vers la TG). La Fig. 2.11 de cet ouvrage montre les courbes de CTI simulées pour ces deux structures (PPD de 4 \( \mu m \)) pour différentes tensions de polarisation appliquée à la TG pendant le transfert (\( V_{HTG} \)). Le front montant de la TG dure 100 ps, ce qui explique les différentes pentes observées sur les courbes pendant les premiers instants du transfert. Comme on peut le voir, les variations de \( V_{HTG} \) affectent fortement le temps de transfert pour la structure A, et ne modifie pas ou peu le temps de transfert pour la structure B.

Ce comportement peut être expliqué par la présence d’une barrière de potentiel [Fos03] dans la structure A (absente dans la structure B) dont la hauteur (\( \Phi_b \)) est modulée en fonction du potentiel de canal de la TG. A cause de cette barrière, les électrons ne rejoignent pas instantanément la FD une fois atteinte l’interface PPD-TG, mais ont une certaine probabilité \( p_{\text{jump}} \) de passer au delà de la barrière par émission thermoïonique qui dépend de l’énergie de l’électron et de \( \Phi_b \) [Fos03] :

\[
p_{\text{jump}} = \exp\left(-\Phi_b/u_{th}\right)
\]

Le cas échéant, les électrons "rebondissent" sur la barrière et continuent à diffuser dans la PPD. La hauteur \( \Phi_b \) dépend de plusieurs paramètres :

- Elle est affectée par les niveaux de dopage sous la TG. En particulier, si le profil de dopage le long du chemin de transfert n’est pas bien échelonné, cela donne lieu à des barrières/poches de potentiel (par exemple la hauteur de la barrière est plus grande dans la structure A que dans la structure B).
- Plus \( V_{HTG} \), plus \( \Phi_b \) est petite [Jan+14]
- Le potentiel de la PPD varie en fonction de la charge stockée. Donc d’une part \( \Phi_b \) augmente entre le début et la fin du transfert, d’autre part \( \Phi_b \) dépend du niveau du signal

Sur la base de ces considérations, pour une topologie de pixel donnée, un utilisateur peut vérifier si le transfert dans le pixel est limité par la présence d’une barrière de potentiel en jouant sur \( V_{HTG} \) et sur le niveau de charge. En particulier, plus le niveau de charge et \( V_{HTG} \) sont élevés, meilleur sera la CTE. Cependant, trop augmenter \( V_{HTG} \) peut donner lieu à des phénomènes de partition de charge [Goi+14b], qui entraîneraient à leur tour une diminution du CTI. Il faut donc trouver un bon compromis. Entre autres, comme indiqué dans le chapitre
de cette thèse, pour des forts niveaux de signal, la mesure peut être fortement affectée par le comportement dynamique en saturation du pixel.

L’effet de la barrière de potentiel a été précédemment étudié dans la littérature en s’appuyant aussi bien sur un modèle Monte Carlo [Fos03], sur une approche statistique [FL07], sur une approche itérative [HYT15] et sur de simulations TCAD [Zho+11]. Ce phénomène est aussi étudié sur la base de simulations numériques dans [Jan+14], mais le modèle utilisé n’est pas détaillé. Dans ces travaux, l’effet des pièges de conception est étudié en intégrant au modèle Monte Carlo une probabilité finie pour les électrons de passer la barrière une fois atteinte l’interface avec la TG. Par rapport à l’approche choisie dans [Fos03] et [FL07], basée sur l’hypothèse que les charges sont toujours “prêtes à ”sauter” la barrière, dans le modèle développé dans cette thèse, aucun champ électrique ne maintient le nuage de charge près de la TG. Par conséquent, les électrons qui ”rebondissent” contre la barrière continuent de diffuser dans la photodiode. De plus, contrairement à [Fos03] et [HYT15], où la variation temporelle de la barrière de potentiel est prise en compte, dans l’hypothèse retenue ici, la barrière reste constante pendant toute la phase de transfert. Cette approche comporte une surestimation de l’inefficacité de transfert dans les premiers instants du transfert de charge, toutefois lors du transfert des derniers électrons, si l’on prend comme hypothèse que la capacité est constante, la variation du potentiel de la PPD est très faible, donc les variations de Φ_b sont négligeables. Comme montré fig. 6, la présence d’une barrière de potentiel peut bien expliquer une dégradation du temps de transfert de plusieurs ordres de grandeur. L’effet du niveau de charge sur la CTE a été simulé en TCAD. Les résultats sont présentés et discutés dans la section 2.5 de cet ouvrage.

Le modèle développé dans ces travaux peut aussi prendre en compte la dérive des charges due à une chute de tension aux bornes de la PPD, au champ auto-induit ou encore au champ latéral de la TG. Ces phénomènes sont détaillés, respectivement dans les sections 2.2.3, 2.2.4 et 2.2.5 de cette thèse. Les phénomènes de piégeage de charge sous la TG sont traités uniquement de façon analytique dans la section 2.2.8 de cet ouvrage. Un résumé des effets sur le temps de transfert des différents mécanismes étudiés est présenté dans le tableau 1. Pour chaque mécanisme, est indiqué quel paramètre de conception/opérationnel il est possible d’ajuster afin de modifier les performances du détecteur en termes de CTE, quels sont les effets de ces variations et, quand c’est possible, quelles mesures ont été faites pour valider ces résultats.

2.6 Mesures expérimentales

Cette section présente les mesures expérimentales du temps de transfert pour des longueurs de PPD allant jusqu’à 32 µm. Les mesures ont été obtenues sur des pixels dédiés qui consistent en un pixel PPD standard (4T) avec une grille de stockage (SG) additionnelle à l’opposé du pixel. Ces dispositifs permettent de reproduire expérimentalement le pire des cas de transfert, pour lequel le nuage d’électrons est photo-généré à l’opposé de la TG. Dans ces travaux, seuls des pixels rectangulaires ont été testés. Toutefois cette méthode se prête très bien à la comparaison et à la caractérisation de topologies de pixels plus exotiques.
2. Modélisation, estimation et mesure du transfert de charge

Figure 6 – Courbes de CTI simulées (simulation Montecarlo) pour une PPD de 2 µm de longueur en prenant en compte la présence d’une barrière de potentiel de hauteur constante $\Phi_b$ à l’interface PPD-TG.

<table>
<thead>
<tr>
<th>Mécanisme</th>
<th>Paramètres</th>
<th>Comportement attendu</th>
<th>Dans ces travaux</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diffusion</td>
<td>$L_{PPD}$</td>
<td>$t_{transf} \propto L_{PPD}^2$</td>
<td>Mes. pour $L_{PPD} = 2\mu m, 4\mu m, 8\mu m, 16\mu m$</td>
</tr>
<tr>
<td>Dérive</td>
<td>$L_{PPD}$</td>
<td>$t_{transf} \propto L_{PPD}$ pour un $\Delta V_{PPD}$ fixé</td>
<td>Simulation</td>
</tr>
<tr>
<td></td>
<td>$\Delta V_{PPD}$</td>
<td>$t_{transf} \propto \Delta V_{PPD}$ pour une $L_{PPD}$ fixé</td>
<td>Simulation</td>
</tr>
<tr>
<td>Émission thermoïonique</td>
<td>$V_{HTG}$</td>
<td>$t_{transf} &gt;&gt;$ quand $V_{HTG} &gt;&gt;$</td>
<td>Mes. for $V_{HTG} = 2.9$V to 3.7V</td>
</tr>
<tr>
<td></td>
<td>$Q_{PPD}$</td>
<td>$t_{transf} &lt;&lt;$ quand $Q_{PPD} &gt;&gt;$</td>
<td>Mes. pour 2 niveaux $Q_{PPD}$</td>
</tr>
<tr>
<td>Champ latéral</td>
<td>$V_{HTG}$</td>
<td>$t_{transf} &lt;&lt;$ quand $V_{TG} &gt;&gt;$</td>
<td>Non mesuré</td>
</tr>
<tr>
<td>Auto-répulsion</td>
<td>$Q_{PPD}$</td>
<td>$&gt;&gt;$ la vitesse de transfert initiale</td>
<td>Développement analytique</td>
</tr>
<tr>
<td>des $e^-$ avec $h^+$</td>
<td>$L_{TG}$</td>
<td>$Q_{out} &lt;&lt;$ quand $L_{TG} &gt;&gt;$</td>
<td>Développement analytique</td>
</tr>
</tbody>
</table>

Table 1 – Tableau résumant les mécanismes affectant les transferts dans les détecteurs PPD CIS.
Afin de mesurer correctement le temps de transfert, il faut tout d’abord identifier les conditions expérimentales pour lesquelles le signal de sortie est affecté par la CTE du dispositif. Une analyse détaillée dans ce sens est présentée dans la section 2.3.1 de ces travaux.

2.6.1 Véhicule de test et principe de mesure

Une matrice 1D de $1 \times 56$ pixels a été conçue dans une technologie commerciale PPD CIS 0.18 µm. La matrice se compose de sept sous-matrices de $1 \times 8$ pixels PPD avec SG. Une vue en coupe d’un pixel SG est montrée Fig. 7. Plus de détails sur la géométrie des pixels testés et sur le banc de mesure sont reportés dans la section 2.3.2 de cette thèse.

Le chronogramme utilisé pour les mesures est montré Fig. 8. Ce chronogramme permet d’injecter électriquement des charges stockées sous la SG au début de la PPD (donc à l’opposé de la TG) à un délai variable par rapport au front descendant du signal TG. Cette approche permet donc de comparer la CTE en injectant toujours la même quantité de charge, au même endroit, quelque soit la géométrie de la diode, pour des temps de transfert de quelques ns. Pour une description détaillée du chronogramme, faire référence à la section 2.3.3 du manuscrit.

La CTI pour un délai donné $\Delta t$ est calculé comme :

$$CTI = 1 - \frac{V_{out}(\Delta t)}{V_{out\max}}$$

avec $V_{out\max}$ la tension de sortie mesurée pour $\Delta t = \Delta t_{\max}$ (avec $\Delta t_{\max} = 90 \mu s$ le délai
2. Modélisation, estimation et mesure du transfert de charge

2.6.2 Résultats expérimentaux

La figure 9 montre la CTI mesurée pour différentes longueurs de PPD et tensions de polarisation $V_{HTG}$. Comme prédit par les simulations, on observe une augmentation du temps de transfert avec le carré de la longueur de la PPD et un effet significatif du potentiel de canal de la TG sur la courbe de CTI. Ces résultats, associés à l’observation expérimentale (Fig. 2.28 de la thèse) de l’effet du niveau de charge sur le temps de transfert, permettent de conclure que pour la technologie testée, l’émission thermoïonique au-delà de la barrière de potentiel due à des pièges de conception est le facteur limitant pour la technologie testée dans ces travaux.

2.7 Conclusion

Le chapitre 2 de ces travaux adresse la problématique des mécanismes limitant la vitesse de transfert de charge dans les détecteurs PPD CIS. L’étude et la compréhension de ces mé-
canismes physiques est particulièrement importante lors de la conception de détecteurs pour applications haute résolution temporelle, car le temps de transfert (i.e. le temps nécessaire pour transférer le paquet de charge de la PPD à la FD en garantissant une CTI donnée) correspond à la limite ultime en termes de période d’échantillonnage. Le transfert de charge a été étudié à travers un modèle Montecarlo simulant le mouvement aléatoire (random walk) des électrons dans la PPD. Ce modèle prend en compte les mécanismes de diffusion, de dérive et d’émission thermoionique. Les simulations ont été comparées à des simulations TCAD 2D et à des mesures expérimentales sur des pixels dédiés. En comparant l’effet de la variation de certains paramètres, tels que la tension de polarisation de la TG pendant le transfert et le niveau de signal, il a été montré que pour la technologie testée, le temps de transfert est principalement limité par l’émission thermoionique des charges au dessus de la barrière de potentiel à l’interface PPD-TG. Cette même approche peut être utilisée pour identifier les phénomènes limitant le transfert dans d’autres technologies ou pour d’autres topologies de pixels. Sur la base de cette étude, il est possible d’améliorer le transfert en augmentant \( V_{\text{HTG}} \) (tout en tenant compte des contraintes liées aux phénomènes de partition de charge), ou bien en maintenant les électrons le plus près possible de la TG le plus longtemps possible pendant le transfert (de telle sorte qu’ils puissent toujours être émis au dessus de la barrière). Ceci peut être obtenu soit en introduisant un champ de dérive dans la PPD (donc en appliquant une différence de potentiel aux bornes de la photodiode), soit en ajoutant un puits de potentiel près de la TG (par exemple en utilisant deux implants de pincement différents de sorte que la zone près de la TG ait un potentiel de pincement plus grand).
3 Définition, estimation et modulation de la tension de pincement

Les performances en termes de résolution temporelle des capteurs PPD CIS sont fortement affectées par la technologie utilisée et la géométrie du pixel. Afin d’optimiser le transfert, la tension de polarisation et la tension de seuil de la TG doivent être ajustées en fonction de la tension d’alimentation du pixel et du potentiel maximum de la PPD, i.e. de la tension de pincement ($V_{\text{pin}}$). La valeur optimale de $V_{\text{pin}}$ dépend fortement de l’application finale visée. Par exemple, une PPD avec un faible $V_{\text{pin}}$ permet souvent d’obtenir de meilleurs performances en termes de CTE. D’autre part, comme indiqué au chapitre 4 de cette thèse, un plus grand $V_{\text{pin}}$ permet d’augmenter la FWC à l’équilibre (EFWC) et donc d’avoir une plus grande plage de fonctionnement.

La tension de pincement ayant un très fort impact sur les performances finales du détecteur, il est important de pouvoir en mesurer de façon fiable la valeur absolue afin de surveiller les lignes de production et observer les effets des variations de process/géométrie et des conditions expérimentales. Le chapitre 3 de cette thèse est dédié à l’étude de la définition physique et de la modélisation de la tension de pincement (notamment de son comportement en fonction de la température) et des méthodes de mesures de $V_{\text{pin}}$ utilisées dans la communauté CIS. La deuxième partie du chapitre est dédiée à l’étude de deux méthodes, présentées dans la littérature, permettant de moduler le potentiel de la PPD afin de générer un champ de dérive pour accélérer le transfert des électrons. Le principe de fonctionnement de chacune des méthodes est étudié sur la base de simulations TCAD et de mesures expérimentales.

3.1 Définition et modélisation de la tension de pincement

Il existe deux définitions différentes de la tension de pincement dans la littérature :

- Dans [KF05], $V_{\text{pin}}$ est défini comme la déviation maximum $\Delta E_{\text{fnmax}}$ du quasi-niveau de Fermi des électrons [Gro67] entre l’équilibre (la PPD est à son taux de remplissage maximum dans le noir et $V_{\text{PPD}} = 0$V) et le dépoulement complet de la PPD de porteur minoritaire.

- Lors de l’évaluation de $V_{\text{pin}}$ sur la base de simulations TCAD, la tension de pincement est définie comme la variation maximum du potentiel électrostatique $\Delta \Phi_{\text{max}}$ de la PPD entre l’équilibre et le dépoulement complet [FH14] ; [Mic+11]

Comme indiqué Fig.10 ces deux paramètres correspondent à des grandeurs physiques très différentes, qui comme démontré par cette thèse, peuvent différer de plusieurs centaines de mV. Dans ces travaux, $V_{\text{pin}}$ est défini comme $\Delta \Phi_{\text{max}}$, qui représente le plafond de potentiel de la PPD et dépend uniquement du profil de dopage et de la géométrie de la photodiode. Comme démontré dans la section 3.1 de ces travaux, $\Delta E_{\text{fnmax}}$ correspond au potentiel de canal de TG minimum permettant de transférer la totalité de la charge stockée dans la PPD (qui dépend, entre autres, des caractéristiques de la TG et de l’interface de celle-ci avec la PPD).
Résumé des travaux de thèse

Figure 10 – Schéma d’un pixel PPD à l’équilibre (a) et suite au transfert de charge (b). Les schémas en potentiel le long de la coupe A-A’ sont reportés, respectivement dans les figures (c) et (d). Les diagrammes de bandes le long de la coupe B-B’ dans des conditions d’équilibre et de déplétion totale sont reportés Fig. (e) and (f).
3. Définition, estimation et modulation de la tension de pincement

La tension de pincement peut être modélisée en faisant les hypothèses simplificatrices suivantes :
- La déplétion latérale de la PPD est négligeable et n’affecte donc pas la tension nécessaire à développer verticalement la PPD. Cette hypothèse est vérifiée quand la largeur et la longueur de la PPD sont supérieures à quelques µm. 
- Le profil de dopage de la PPD est réalisé de sorte que la zone dépeuplée de la PPD puisse être approximée à celle d’une simple jonction p-n unilatérale [TN09], correspondant à la jonction p+/n.

Sous ces hypothèses on peut donc utiliser un simple modèle 1D pour estimer $V_{\text{pin}}$ :

$$V_{\text{pin}} = \frac{qN_{\text{PPD}}d_{\text{PPD}}^2}{2\epsilon_{\text{Si}}} - V_{\text{bi}}$$  \hspace{1cm} (9)

avec $q$ la charge élémentaire, $d_{\text{PPD}}$ la profondeur de l’implant n de la PPD, $\epsilon_{\text{Si}}$ permittivité du Si et $V_{\text{bi}}$ le potentiel induit de la jonction p+/n [TN09]. Afin de prendre en compte l’effet de la géométrie et des profils réels de potentiel, il serait nécessaire de développer un modèle beaucoup plus complexe. Des modèles plus détaillés sont proposé dans [Cao+14] et [PU09], toutefois une approche TCAD serait probablement plus indiquée étant donné la complexité du problème.

3.2 Mesure de la tension de pincement

Des mesures de la tension de pincement sont souvent utilisées dans l’industrie pour contrôler les lignes de production et développer/optimiser les technologies PPD CIS. N’existant pas de **standard** pour ce type de mesure, chacun utilise des méthodes développées en interne, qui sont souvent basées sur des principes physiques très différents les uns par rapport aux autres. Une étude comparative des méthodes utilisées pour la mesure de $V_{\text{pin}}$ est présentée dans la section 3.3 de cette thèse. Ces méthodes peuvent être rassemblées en deux catégories :

1. Méthodes basées sur des structures de test ou des matrices de structures de test. Celles-ci peuvent, à leur tour, être divisées en deux catégories :
   - Méthodes basées sur des structures de type JFET (Junction Field Effect Transistor) [SD82] ; [PU09] ; [Con09] ; [Hyn81], où $V_{\text{pin}}$ est estimée comme la tension de “pinch-off” $V_p$ [Nea11] de structures JFET réalisées avec des implants PPD.
   - Méthodes basées sur des mesures capacitatives [LRF11].

2. Méthodes basées sur des mesures in-pixel [TBT12] ; [Goi+14b] ; [XGT15] ; [Cha+14], où $V_{\text{pin}}$ est mesurée directement sur des matrices de pixels PPD. i

En particulier, ce document démontre que plusieurs méthodes utilisées dans l’industrie ne permettent pas d’estimer la valeur absolue de la tension de pincement, mais uniquement d’observer des variations relatives de cette dernière. Il montre également qu’au moins deux méthodes, l’une basée sur des structures de test de type JFET (méthode de la racine dans la section 3.3.1.1) et la mesure mesure in-pixel (section 3.3.2), permettent de mesurer la valeur absolue de $V_{\text{pin}}$. 

21
3.3 Comportement de la tension de pincement en fonction de la température

L’effet de la température sur la tension de pincement peut être modélisé en ré-écrivant l’équation 9 de sorte à mettre en évidence la dépendance de la température de chacun des paramètres. Dans le premier terme de l’équation \( \left( \frac{qN_{PPD}d_{PPD}}{2\epsilon_{Si}} \right) \) tous les paramètres sont des constantes qui dépendent uniquement de la technologie ou de la géométrie, le comportement en température de \( V_{pin} \) peut donc être simplement approximé au comportement de \( V_{bi} \) :

\[
V_{bi}(T) = \frac{kT}{q} \ln \left( \frac{N_a N_{PPD}}{n_i^2(T)} \right)
\]

où \( n_i(T) \) peut être modélisé comme proposé dans [Mis+93]. Comme montré en Fig. 11, ce modèle, bien que simple, reproduit bien l’effet de la température sur la tension de pincement.

![Figure 11 – Tension de pincement mesuré en fonction de la température (méthode in-pixel) comparée au modèle proposé dans ces travaux.](image)

3.4 Modulation statique et dynamique de la tension de pincement

Dans les grands pixels, le potentiel de la PPD est approximativement constant dans toute la PPD (à l’exception du champ latéral à proximité de la TG lors du transfert et des bords de la PPD). Par conséquent, le transfert de charge repose principalement sur la diffusion thermique des charges. Comme indiqué dans le chapitre 2 de cet ouvrage, le temps nécessaire pour transférer les charges dans des pixels de plusieurs \( \mu \text{m} \) peut être de l’ordre de plusieurs dizaines de \( \mu \text{s} \) dans un régime purement diffusif. Ces temps extrêmement longs (par rapport à la résolution temporelle souhaitée pour des applications grande vitesse) peuvent être expliqués par la non-directionnalité des phénomènes diffusif et de l’effet des pièges de conception. Afin
3. Définition, estimation et modulation de la tension de pincement

D’améliorer le transfert, le potentiel de la PPD peut être modulé spatialement, de telle sorte à générer un champ électrique pour accélérer les charges vers le nœud de lecture.

Différentes solutions ont été proposées dans la littérature pour induire un champ électrique dans les pixels PPD [SPS10]; [Li+12]; [Miy+14]; [Tub+09]. Ces méthodes peuvent être divisées en deux catégories : méthodes statiques et méthodes dynamiques, basées respectivement sur la génération d’un champ électrique statique ou variable dans le temps. Les méthodes statiques sont adaptées à des pixels avec un seul nœud de lecture, dans lesquels il est suffisant d’accélérer les charges toujours dans la même direction. Dans le cas de pixels présentant plusieurs noeuds de lecture, tels que les pixels démodulateurs (lock-in pixels) [Lan+00]; [BLS06]; [Sto+11]; [Kim12]; [Sto+11]; [Bon+13a]; [Han+14], il peut être beaucoup plus avantageux d’implémenter un champ électrique dynamique.

3.4.1 Modulation Géométrique

La section 3.5.1 du manuscrit présente un étude sur la modulation géométrique de la tension de pincement [Tak+10]. L’application de cette méthode aux pixels PPD a été étudiée dans [Tak+10], où il est montré qu’un modèle 1D de la tension de pincement amène à une surestimation du potentiel dans la PPD pour des pixels dont au moins une des dimensions est de quelques μm. Cette modulation de $V_{\text{pin}}$ peut être expliquée par une modulation latérale de la zone dépeuplée verticale dans la PPD, qui est accentuée lorsque les deux dimensions de la PPD (largeur et longueur) sont toutes deux petites. Pour prendre en compte ces effets, il est possible de résoudre l’équation de Poisson en 3D. Toutefois les simulations TCAD représentent une solution simple pour estimer l’effet de la géométrie de la photodiode sur le profil de potentiel.

TCAD simulations : La Fig. 12 montre la tension de pincement simulée en fonction de la largeur de la PPD sur une photodiode partiellement pincée de longueur $L_{\text{PPD}} = 5 \mu m$. Comme on peut l’observer, des variations de tension de pincement de l’ordre de 100 mV-150 mV peuvent être obtenues, en variant les dimensions de la PPD pour une tension de pincement intrinsèque de 700 mV.

Mesures expérimentales : L’effet de la taille de la PPD sur la tension de pincement a été mesuré sur des structures de test de type JFET et par le biais de mesures in-pixel. Les mesures expérimentales sont montrées Fig. 13. Comme prédit par les simulations TCAD, la tension de pincement varie fortement en fonction des dimensions de la photodiode jusqu’à quelques μms de largeur. Ces mesures montrent aussi une bonne correspondance entre les valeurs de $V_{\text{pin}}$ estimées avec la méthode in-pixel et la méthode de la racine. Les autres méthodes étudiées, telles que la méthode du courant (Cu.) et la méthode de la source flottante (source. float) permettent uniquement d’observer des variations relatives de la tension de pincement en fonction de la largeur du pixel.
Figure 12 – $V_{pin}$ simulée sur une photodiode partiellement pincée de longueur $L_{PPD} = 5 \mu m$ et largeur variable.

Figure 13 – $V_{pin}$ en fonction de la largeur de canal des structures PPD-JFET $W_{JFET}$ (ou de la dimension minimum de la PPD $W_{PPD}$) estimées avec la méthode in pixel [TBT12], avec la méthode de la source flottante [Cou09], avec la méthode du courant [PU09] et avec la méthode de la racine [SD82]. La longueur de canal des structures PPD-JFET est de $L_{JFET} = 20 \mu m$. Tous les dispositifs testés dans ces travaux ont été conçus à l’ISAE. Une partie des mesures a été effectuée par A. De-Ipanema Moreira dans le cadre d’un projet étudiant en deuxième année à l’ISAE.
3. Définition, estimation et modulation de la tension de pincement

3.4.2 Lateral Electric Field Modulation (LEFM)

Une méthode de modulation dynamique du potentiel a été proposée par Kawahito et al. en 2013 [Kaw+13]. Cette méthode, appelée Lateral Electric Field Modulation (LEFM) est basée sur le contrôle du potentiel local dans la PPD par le biais de paires d’électrodes latérales. Un capteur basé sur la méthode LEFM a été conçu récemment par ces mêmes auteurs dans une technologie PPD CIS A 0.11 µm dédiée [Han+14]. La section 3.5.3 de cet ouvrage est dédiée à l’étude de la méthode LEFM, sur la base de simulations TCAD et de mesures expérimentales sur un détecteur bi-ports conçu dans le cadre de ces travaux de thèse dans une technologie PPD CIS 0.18 µm commerciale.

Principe de fonctionnement : La méthode LEFM se base sur la modulation du potentiel local de la PPD $V_{PPD}$ par le biais de champs latéraux induits par des paires de grilles latérales (LG). En particulier, en utilisant plusieurs paires de grilles, dont la polarisation est modifiée dans le temps, on obtient une modulation dynamique du profil de potentiel dans la PPD.

La Fig. 14 montre une vue en coupe d’une PPD associée à une paire de grilles latérales (situées des deux côtés de la PPD). Afin de visualiser le dispositif en 3 dimensions, il faut s’imaginer que la TG se trouve dans l’axe perpendiculaire à la page. Le dessin schématique du dispositif représente aussi une paire de diffusions n+ associées aux LG, qui sont polarisées à une tension $V_D$.

L’implant de pincement p+ est fortement dopé, par conséquent ce dernier reste toujours pincé au potentiel du substrat et le potentiel dans la PPD ne peut jamais dépasser le potentiel de pincement intrinsèque ($V_{pinI}$) qui serait mesuré dans un grand pixel (sans aucune modulation géométrique), quel que soit le potentiel $V_{LG}$ appliqué (si l’on reste dans des plages de tension typique). Ceci signifie que pour moduler le potentiel dans la PPD, il faut tout d’abord le réduire (et donc réduire $V_{pin}$) par le biais d’une modulation géométrique. En quelques mots, la méthode LEFM peut être appliquée uniquement sur des pixels étroits, et consiste dans une "compensation" de la modulation géométrique de la tension de pincement. Si l’on indique par $V_{pinLO}$ la tension de pincement d’un pixel étroit avant d’appliquer la méthode LEFM, la modulation maximum de potentiel pouvant être générée dans la PPD est de :

$$\Delta V_{PPD} = V_{pinHI} - V_{pinLO}$$

De ce fait, plus l’on souhaite obtenir de grands $\Delta V_{PPD}$ (et donc augmenter le champ électrique) plus il est nécessaire d’utiliser une technologie avec une grande tension de pincement intrinsèque et de concevoir une PPD étroite.

Simulations TCAD : Afin d’identifier les avantages et les inconvénients de la méthodes LEFM, cette dernière a été étudiée sur la base de simulations TCAD et de mesures expérimentales.

3. Comme montré dans la suite de ces travaux, ces diffusions ne sont pas indispensables au bon fonctionnement de la méthode, mais permettent de drainer les charges générées ou stockées sous les LG.
Figure 14 – Vue en coupe d’une structure LEFM. Diagramme de potentiel dans la structure en fonction de la tension de polarisation appliquée à la paire de grilles latérales. $V_{LG}$. 

Résumé des travaux de thèse
3. Définition, estimation et modulation de la tension de pincement

La Fig. 15 présente les résultats d’une simulations TCAD 2D de la structure montrée Fig. 14. En particulier la figure montre le potentiel maximum dans la PPD en fonction de la tension de polarisation des LG pour différentes largeurs de PPD. Comme montré par l’analyse précédente du mécanisme de fonctionnement, la modulation du potentiel est d’autant plus importante, que les pixels sont étroits.

**Figure 15** – Potentiel maximum dans la PPD simulé en fonction de $V_{LG}$ pour différentes largeurs de PPD. La structure simulée est montrée Fig. 14.

**Circuits de test :** Un circuit de test, dont les caractéristiques sont détaillées dans la section 3.5.4.3 de cet ouvrage a été réalisé avec les objectifs suivants :

1. Vérifier le principe de fonctionnement de la méthode LEFM sur un détecteur bi-ports réalisé avec une technologie PPD CIS 0.18 μm.

2. Étudier l’effet de la géométrie du pixel sur l’efficacité de modulation du potentiel, notamment en termes d’orientation des charges et d’efficacité de transfert.

Les topologies de pixels testées se divisent en deux catégories : pixels avec diffusions n+ associées aux LG (**pixels de type D**) et sans diffusion (**pixels de type ND**). La vue de dessus de ces deux topologies de pixels est montrée Fig. 16. Pour chacune des topologies, 4 largeurs différentes de pixels ont été testées (0.5 μm, 1.0 μm, 2.0 μm and 4.0 μm).

**Efficacité d’orientation des charges :** La première validation expérimentale a consisté à mesurer l’efficacité d’orientation des charges vers une des deux TG (donc vers un des deux ports de sortie). Le chronogramme utilisé est détaillé Fig. 17. Pour plus de détails nous renvoyons à la section 3.5.4.4 de cet ouvrage. L’objectif de cette mesure est de quantifier le partage des charges entre les deux ports de sortie en fonction de la tension de polarisation des LG $V_{LG}$.

La Fig. 18, montre le signal de sortie mesuré pour différentes largeurs de PPD sur des
(a) PIXEL "D"

(b) PIXEL "ND"

Figure 16 – Vue de haut des deux topologies de pixels étudiés : (a) avec et (b) sans diffusion n+ associées aux grilles latérales LG (respectivement pixels “D” et “ND”).

Figure 17 – Chronogramme utilisé pour la mesure de l’efficacité d’orientation des charges.
3. Définition, estimation et modulation de la tension de pincement

pixels de type “ND” en fonction de $V_{LG1}$ et $V_{LG2}$. Comme on peut l’observer, l’efficacité d’orientation s’améliore si l’on augmente $V_{LG1}$, il y a donc une modulation du potentiel local dans la proximité des grilles LG1. De plus, l’orientation des charges est d’autant plus efficace que les pixels sont étroits. En particulier, une efficacité d’orientation jusqu’à 90% est observée pour les pixels avec $W_{PPD} = 0.5\, \mu m$ en polarisant les grilles latérales à des tensions de l’ordre de 2 V. Les résultats obtenus sur les pixels de type “D” sont présentés Fig. 3.26 de cet ouvrage.

**Efficacité de transfert de charge :** La deuxième validation expérimentale de la méthode LEFM a consisté à mesurer l’effet de $V_{LG}$ sur le CTI. Le chronogramme utilisé est montré Fig. 19. Le temps de transfert (qui correspond dans cette mesure au temps d’ouverture de la TG) est varié de 10 ns à 1 $\mu s$. $V_{LG2} = -0.4\, \text{V}$ au cours de toute l’acquisition. Les résultats des mesures effectuées sur des pixels de type “ND” sont montrés Fig. ???. Les mesures obtenues sur les pixels de type “D” sont montrés dans la section 3.5.4.4 de cet ouvrage. Comme on peut l’observer, l’efficacité de transfert s’améliore si l’on augmente $V_{LG1}$ ; et ceci d’autant plus que les pixels sont étroits.

3.5 Conclusion

Le chapitre 3 de ces travaux de thèse a été dédié à la définition, modélisation et estimation de $V_{pin}$. Deux différentes définitions de $V_{pin}$ sont utilisées aujourd’hui dans la communauté CIS : $\Delta \Phi_{\text{max}}$ et $\Delta E_{\text{fimax}}$. $\Delta \Phi_{\text{max}}$ correspond au potentiel électrostatique maximum de la PPD (donc au “fond” du puits de potentiel de la PPD), lorsque $\Delta E_{\text{fimax}}$, correspond au potentiel de canal de TG minimum pour garantir un transfert optimum des charges. Dans ces travaux, $V_{pin}$ a été défini comme $\Delta \Phi_{\text{max}}$. 
Figur 19 – Chronogramme pour la mesure de l’efficacité de transfert.

Figur 20 – CTI mesuré pour deux tensions $V_{LG1}$ sur des pixels de type “ND”.
3. Définition, estimation et modulation de la tension de pincement

Un modèle 1D du comportement en température de $V_{\text{pin}}$ a été proposé et validé expérimentalement. En particulier il a été montré que $V_{\text{pin}}$ augmente avec la température.

$V_{\text{pin}}$ est mesuré aussi bien sur la base de mesures in-pixels que de mesures électriques obtenues sur des structures isolées (ou des matrices de structures). Les avantages et les inconvénients des différentes méthodes sont résumées dans le tableau dans la section 3.7 de cet ouvrage.

Deux méthodes de modulation de la tension de pincement dans les PPD CIS, permettant de générer un champ électrique dans la PPD (et donc d’améliorer la vitesse de transfert) ont aussi été étudiées dans le chapitre 3 de ces travaux. La modulation géométrique consiste en une modulation spatiale de la largeur de la PPD, qui permet de réduire localement la tension de pincement. Cette méthode a l’avantage d’être simple, mais permet uniquement de générer un champ électrique statique. Une autre approche consiste à utiliser la méthode LEFM, pour laquelle le potentiel à proximité de grilles latérales peut être modulé dans le temps en fonction des tensions de polarisation appliquées. Il a été montré, par le biais de simulations TCAD et de mesures expérimentales, que cette méthode est efficace uniquement lorsque la PPD est suffisamment étroite pour observer une modulation géométrique de la tension de pincement. Les dispositifs testés ont montré une bonne efficacité d’orientation des charges (de l’ordre de 90%) pour des pixels de largeur 1 µm et 2 µm, cependant, l’amélioration en termes de CTI reste contenue (moins d’un facteur 2), du fait du faible champ électrique pouvant être généré avec la méthode LEFM.
Conclusions et Perspectives

Cette thèse présente une étude des paramètres clé de conception des capteurs d’image CMOS à photodiode pincée pour des applications de haute résolution temporelle. Ces travaux abordent, tout particulièrement, la façon dont ces paramètres sont affectés par les conditions expérimentales et comment ils peuvent/devraient être mesurés. Quand cela a été possible, l’étude a été associée au développement d’un modèle analytique spécifique.

Une nouvelle structure de pixels, basée sur une grille de stockage (SG) pulsée a été conçue pour mesurer le temps de transfert dans les PPD. Le principe de mesure consiste à injecter électriquement un paquet de charges à l’extrémité de la PPD à des délais croissants par rapport au front descendant du signal de commande de la TG. Ces pixels permettent de comparer, de la façon la plus "objective" possible, les performances en termes d’efficacité de transfert pour différentes géométries et tailles de pixels. Les mesures obtenues sur des pixels de type SG avec des longueurs de PPD allant de 2µm à 32µm ont mis en évidence que le temps de transfert est beaucoup plus long (quelques ordres de grandeurs) par rapport à ce qui est estimé en résolvant simplement les équations de diffusion. Cette différence peut être expliquée par la présence d’une barrière de potentiel (ou poche de potentiel) au niveau de l’interface TG-PPD, pouvant fortement ralentir le transfert des derniers électrons. Deux solutions simples qui permettent donc d’améliorer le transfert consistent, d’une part à augmenter la tension de polarisation de la TG pendant le transfert (la tension maximum utile est toutefois limitée par les phénomènes de partition de charge), et d’autre part à garder les électrons près de la TG le plus longtemps possible pendant le transfert. Pour cela, il peut être intéressant d’ajouter une zone de collection (ayant un plus grand \( V_{pin} \)) près de la TG. Cette solution a déjà été adoptée dans la littérature pour réduire la distance effective de diffusion des électrons, tout en gardant une grande surface de collection de charge.

Un développement analytique a permis de montrer que la probabilité de piégeage d’électrons sous la TG pendant le transfert de la charge est extrêmement faible. Cependant, il est montré, à travers un raisonnement analytique similaire, que les états d’interface peuvent effectivement affecter le signal de sortie. En particulier comme suggéré dans [Jan+15], les électrons peuvent se recombiner avec les trous ayant été piégés pendant le temps d’intégration (qui est souvent de l’ordre de plusieurs ms) et qui sont libérés dès que la TG devient passante. Il est important de remarquer que ce dernier phénomène ne conduit pas à une rémanence de charge mais plutôt à une non-linéarité du signal de sortie (due à une réduction de l’efficacité quantique effective du dispositif qui est fortement dépendante du niveau de charge).

Ces travaux ont porté aussi sur la définition, la modélisation et la mesure de la tension de pincement (\( V_{pin} \)). Deux différentes définitions sont utilisées aujourd’hui pour faire référence à \( V_{pin} \). Ce paramètre est parfois défini comme la variation maximum du niveau de quasi-Fermi des électrons (\( \Delta E_{F_{\text{max}}} \)), qui est la définition la plus utilisée dans les publications scientifiques, ou bien comme la variation maximum du potentiel électrostatique (\( \Delta \Phi_{\text{max}} \)), qui est souvent utilisée pour estimer \( V_{pin} \) à partir de simulations TCAD. Il est important de remarquer que,
Conclusions et Perspectives

du fait de l’émission thermoïonique des électrons depuis le canal de la TG vers la PPD, quand le potentiel de la PPD atteint $\Delta \Phi_{\text{max}}$, la PPD n’est pas encore complètement dépeuplée. Toutefois, dans ces travaux, il a été choisi de définir $V_{\text{pin}}$ comme $\Delta \Phi_{\text{max}}$, car ce paramètre est fortement lié aux propriétés de la PPD. Comme il a été mis en évidence par ces travaux, mesurer les variations de $\Delta E_{\text{fmax}}$ peut aussi apporter des informations importantes, car ce dernier donne une estimation du potentiel minimum qu’il faut appliquer dans le canal de la TG pour vider complètement la PPD.

Au sein de la communauté CIS, $V_{\text{pin}}$ est estimé expérimentalement ou bien à travers des mesures électriques sur des structures de test (ou des matrices de structures de test) ou sur la base de mesures intra-pixel. Parmi les méthodes étudiées dans ces travaux, il a été montré que seulement la mesure de la racine $\sqrt{SD82}$ et les mesures in-pixels [TBT12] permettent de mesurer la valeur absolue de $V_{\text{pin}}$. Il a été démontré également, sur la base de simulations et de mesures expérimentales, que les méthodes de mesure de $V_{\text{pin}}$, qui reposent sur un comportement on/off des JFETs, telles que la méthode de la source flottante [Cou09] ou la méthode du courant [PU09], permettent uniquement de mesurer des variations relatives de $V_{\text{pin}}$ (car la valeur absolue mesurée dépend des conditions expérimentales). Les mesures intra-pixel donnent une estimation de $V_{\text{pin}}$ dans un environnement identique à celui de fonctionnement et permettent d’avoir une bonne statistique (moyenne sur un grand nombre de pixels). Ces mesures permettent entre autres d’estimer d’autres paramètres, tel que l’EFWC, $\Delta E_{\text{fmax}}$ et le potentiel de canal de la TG, toutefois en matrice il est difficile de tester autant de topologies de pixels que pour des mesures basées sur des structures de test. Pour cette raison les deux approches devraient être considérées complémentaires.

La vitesse de transfert de charge peut être améliorée (par rapport à un régime de diffusion simple), en introduisant un champ de dérive dans la PPD (par exemple en penchant le potentiel de la PPD). La chute de potentiel théorique maximale pouvant être générée dans la PPD est égale à la tension de pincement mesurée dans de grandes photodiodes ($V_{\text{pin}}$ intrinsèque de la technologie). Comme cela a déjà été démontré dans la littérature, une modification de la taille minimum de la PPD, conduit à une modulation du potentiel de la PPD (modulation géométrique), et donc les PPD triangulaires ou trapézoïdales peuvent être conçues pour accélérer les électrons vers la TG. Malgré les fortes contraintes géométriques, cette technique de modulation est efficace et simple à mettre en œuvre. Par rapport à une solution basée sur un puits de potentiel près de la TG (qui n’impose pas ou peu de contraintes géométriques), la modulation géométrique a l’avantage de pouvoir être utilisée pour des applications où le temps d’intégration est extrêmement court (donc pour lesquelles les charges n’ont pas le temps de diffuser jusqu’à la zone de collection avant le début de la phase de transfert).

Une autre solution pour améliorer le transfert, qui a été proposée dans [Han+14], consiste à générer un champ électrique dynamique par le biais de paires de grilles latérales. Cette méthode est appelée LEFM (Lateral Electrical Field Modulation). Il a été démontré au moyen de mesures effectuées sur une petite matrice de pixels que cette méthode permet d’obtenir une orientation efficace des électrons pour des pixels très étroits (moins de 2 $\mu$m), toutefois, en mode dynamique, du fait du faible champ électrique qui peut être généré avec cette méthode, l’amélioration en termes d’efficacité de transfert est assez contenue par rapport à une photo-
diode standard (moins d’un facteur 1.5). La méthode LEFM introduit de fortes contraintes géométriques, une diminution de la surface active et une augmentation du courant d’obscurité; il est donc intéressant de l’appliquer uniquement pour les applications demandant explicitement une orientation dynamique de charges.

Une approche alternative pour obtenir un champ électrique dynamique dans les dispositifs BSI tout en se dégageant des contraintes géométriques, serait de moduler le potentiel de la PPD à l’aide d’électrodes métalliques placées au-dessus du PMD (Pre-Metal Dielectric) ou tout simplement en ajoutant des portes en polysilicium au dessus de la PPD. Précisons que pour moduler le potentiel de la PPD depuis la surface, l’implant p+ doit tout d’abord être inversé, ce qui signifie que son potentiel (potentiel de surface) n’est pas pincé. Le potentiel de la PPD peut donc être augmenté au-dessus du \( V_{\text{pin}} \). Ce type de dispositif serait donc un dispositif "temporairement pincé". Cependant, ces deux méthodes ne peuvent pas être implémentées avec les technologies commerciales disponibles, étant donné que le potentiel de polarisation nécessaire pour inverser l’implant de surface est de plusieurs centaines de Volts. En outre, les technologies standards ne permettent généralement pas de générer les implants de la PPD en dessous d’une grille en polysilicium.

Ces travaux montrent également que la full well capacity (FWC), qui est souvent donnée comme une valeur fixe dans les fiches techniques des imageurs, dépend fortement des conditions expérimentales. En particulier, un modèle analytique a été développé pour prédire le comportement de la FWC en fonction de la température de travail, des conditions de polarisation et du flux de photons incidents. Ils montrent également que dans l’obscurité avec la TG en mode accumulé, la charge stockée dépend uniquement de la capacité de la PPD et de \( V_{\text{pin}} \). Ce paramètre clé a été introduit pour la première fois par ces travaux de thèse et est appelé FWC à l’équilibre (EFWC). Si la TG est accumulée pendant la phase d’intégration, la charge stockée dans la PPD peut dépasser l’EFWC. Comme il a été mis en évidence par ces travaux, dans ces conditions expérimentales, la PPD est polarisée en direct lorsqu’elle atteint sa FWC. Cette thèse a aussi montré, par rapport aux publications précédentes, que la valeur de la FWC augmente logarithmiquement en fonction du flux incident même si la TG est en mode accumulé, du fait du courant direct de la photodiode (dans la littérature, la dépendance de la FWC du flux était uniquement attribuée au courant sous-seuil de la TG). Ces travaux montrent de plus que si une faible tension positive est appliquée à la TG pendant l’intégration, la charge en excès est drainée vers le nœud de lecture (FD) et on observe une diminution linéaire de la FWC avec \( V_{\text{LOTG}} \). Enfin, ces travaux ont mis en évidence des comportements différents de la FWC avec la température en fonction des conditions d’éclairement. Si la PPD est polarisée en direct (donc en éclairement), une augmentation de la température entraîne une diminution de la FWC, alors que dans l’obscurité, la FWC augmente avec la température en raison de l’augmentation de \( V_{\text{pin}} \). Ces résultats sont très importants car ils montrent que les valeurs de FWC sont dénuées de sens si les conditions expérimentales ne sont pas spécifiées, et que le seul paramètre qui caractérise réellement un pixel est son EFWC.

Ces travaux étudient également le comportement dynamique de la FWC. Ils montrent que si le niveau d’éclairement est brusquement modifié, la PPD tendra vers une nouvelle condition de pseudo-équilibre. Plus le niveau final d’électrons est faible, plus le courant circulant dans
la jonction pn est petit et donc plus le transitoire pour atteindre la conditions de pseudo-équilibre sera long. Cela signifie qu’à moins que le temps d’intégration et la EFWC de la PPD ne soient dimensionnés pour assurer que, dans des conditions d’utilisation nominales, la charge de la PPD soit en dessous de la EFWC, des erreurs significatives peuvent affecter la tension de sortie si le niveau d’éclairement dans la scène imagée change rapidement. Ces considérations peuvent être étendues aux méthodes de mesure de lag (rémanence), qui sont souvent basées sur une source lumineuse pulsée, pour lesquelles la largeur et l’intensité de l’impulsion doivent être choisies de sorte que la PPD ne soit jamais polarisée en direct (donc que la charge reste inférieure à l’EFWC).

Pour conclure, les méthodes développées dans cette thèse peuvent s’avérer un outil intéressant afin d’optimiser les imageurs PPD CIS. Le modèle de transfert de charge, associé à des mesures sur des pixels de type SG, peuvent aider à identifier les phénomènes physiques limitant le transfert pour une technologie ou une topologie de pixel données. Afin d’améliorer le modèle, il serait intéressant de prendre en compte dans les simulations numériques, les phénomènes de piégeage de charge sous la TG. Le modèle de FWC a déjà fait l’objet de références dans la littérature relatives à l’effet du flux lumineux sur la valeur de la FWC [FH14]; [Zuj+15]; [MC+15] ou encore comme point de départ lors de l’étude d’autres paramètres des PPD CIS [Goi+14b]; [Cha+14]; [Cao+15]; [XGT15]; [Inn15]. Dans [Goi+14a], les variations d’EFWC ont été utilisées pour étudier les effets des radiations sur les capteurs d’image. Les méthodes de caractérisation des APS 3T ont souvent été appliquées "telles-elles" aux PPD CI, toutefois, comme le montrent ces travaux, il serait utile de développer de nouvelles méthodes et de donner des indications afin d’uniformiser la mesure de figures de mérites telles que le CVF, la FWC et $V_{\text{pin}}$. En particulier, il reste encore beaucoup à faire en matière de méthodes de mesure du CVF, afin que celles-ci soient adaptées aux contributions de bruit spécifiques des détecteurs PPD CIS.
Bibliographie


Bibliographie


Bibliographie


Bibliographie


Publications et Conférences


Abstract — Driven by an aggressive market competition, CMOS Image Sensor technology is in continuous evolution. Thanks to the outstanding noise performances of Pinned Photodiode (PPD) CIS, CMOS sensors can now reach a few photons sensitivity, which makes this technology a particularly interesting candidate for high temporal resolution applications. Despite the incredibly large production volume, today, the PPD physics is not yet fully understood, and there is still a lack of golden standards for the characterization of PPD performances. This thesis focuses on the definition, analytical modeling, simulation and estimation of PPD key design parameters, with a particular focus on charge mechanisms, on the pinning voltage and on the full well capacity. The models developed in this work can help both manufacturers and users understanding the design trade-offs and the dependence of these parameters from the experimental conditions, in order to optimize the sensor design, to correctly characterize the image sensor, and to adjust the operation conditions to reach optimum performances.

Keywords : Pinned Photodiode, CMOS Image Sensors, transfer time, pinning voltage, Full Well Capacity, high temporal resolution, pulse storage gate pixel

Résumé — Poussée par une forte demande et un marché très compétitif, la technologie PPD CIS est en évolution permanente. Du fait de leurs très bonnes performances en terme de bruit, les capteurs d’image CMOS à base de Photodiode Pincée (PPD CIS) peuvent désormais atteindre une sensibilité de l’ordre de quelques photons, ce qui rend cette technologie particulièrement intéressante pour les applications d’imagerie à haute résolution temporelle. Aujourd’hui, la physique des photodiodes pincées n’est pas encore comprise dans son intégralité et il y a un manque important d’uniformisation des méthodes de caractérisation de ces détecteurs. Ces travaux s’intéressent à la définition, à la modélisation analytique, à la simulation et à l’estimation de paramètres clés des PPD CIS, tels que le temps de transfert, la tension de pincement et la full well capacity (FWC). Comme il a été mis en évidence par cette thèse, il est de première importance de comprendre l’effet des conditions expérimentales sur les performances de ces capteurs. Ceci aussi bien pour l’optimisation de ces paramètres lors de la conception du capteur, que lors de la phase de caractérisations de celui-ci, et enfin pour choisir correctement les conditions de mesures lors de la mise en œuvre du dispositif.

Mots clés : Photodiode pincée, Capteurs d’image CMOS, transfert de charge, tension de pincement, Full Well Capacity, haute résolution temporelle, pixel à grille de stockage pulsée.

ISAE-SUPAERO, Université de Toulouse, Image Sensor Research Team, 10 avenue E. Belin, F-31055, Toulouse, France